

A Four-Transistor Capacitive Feedback Reset Active Pixel and its Reset Noise Reduction Capability

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Abstract

A new CMOS active pixel with reset noise reduction capability using capacitive feedback reset (CFR) is proposed. The CFR pixel with capacitive feedback consists of a photodiode, four MOS transistors, a feedback capacitor and a buffer capacitor. It can be fabricated in standard CMOS process, thus yielding a low noise pixel without additional process steps. It has been confirmed with a fabricated pixel structure that the reset noise is reduced to 0.39 times the reset noise level of the conventional photodiode active pixel configuration.

I. Introduction

The Several improvements are needed for CMOS active pixel sensors (APS's) to reproduce as good image quality with high sensitivity as the charge couple device (CCD) image sensors provide. One of fundamental issues of CMOS APS is reset noise reduction. In most of conventional CMOS active pixels fabricated using general purpose CMOS technologies, reset noise is generated when the photodiode voltage is initialized through a reset switch. The reset noise voltage v_n is given by

$$v_n = \sqrt{kT/C} \quad (1)$$

where k is the Boltzmann's constant, T the absolute temperature and C the photodiode capacitance[1]. The number of noise electrons caused by the reset after the correlated double sampling (CDS) is expected to be 40 electrons, supposing the photodiode capacitance of 5 fF. This value is a few times larger than the noise floor of the CCD image sensors ($10 \sim 20 e^-$), thus resulting in a few times lower sensitivity. Although the reset noise voltage can be reduced to $\sqrt{kT/2C}$ with the reset transistor operating in a saturation region [2], the noise is still larger than CCD imagers.

A pinned photodiode APS is being investigated to suppress the kTC noise as well as to reduce the dark current [3-5]. However, there is a concern about incomplete charge transfer with low supply voltage, as CMOS device continues to scale with reduced supply voltage.

On the other hand, several readout circuits have been proposed for infrared focal-plane arrays. Among them, there is the capacitor feedback transimpedance amplifier (CTIA)[6,7]. Although the reset noise is generated at a

reset of CTIA, the fact that the photodiode voltage is fixed at a reference voltage is applicable to the reset noise reduction (by means of a circuit topology). Recently, Fowler, *et al.* proposed a pixel in which a feedback circuit was formed for reset noise suppression and demonstrated the reset noise was reduced to $\sqrt{kT/18C}$ [8]. However, it is difficult to reduce pixel size, since their proposed pixel requires 5 n-MOSFETs and one p-MOSFET in each pixel.

In this paper, a low noise 4-transistor CMOS active pixel using capacitive feedback reset (CFR) operation is proposed. Since the pixel has reset noise reduction capability without requiring a special process technology, such as pin photodiode, it is feasible to built low noise, low power supply and low cost CMOS imagers.

II. Pixel Design

a. Circuit Configuration

The circuit configuration of the pixel together with bias circuits on each column is shown in Fig. 1. The unit pixel consists of a photodiode, four MOS transistors, a feedback capacitor C_2 and a buffer capacitor C_3 . A capacitor C_1 is the photodiode capacitor and a capacitor C_4 represents a parasitic capacitance between the photodiode and the drain of M_{RD} .

Fig. 2 shows a pulse timing diagram. Waveforms of the inverter output $V_{inv, out}$, the source follower output V_{out} and the photodiode voltage V_{PIX} are also shown. During the readout/reset period, the row select pulse ϕ_{SEL} is turned ON with the pulse ϕ_{VDSW} being OFF, so that the transistors M_{RD} and M_{NB} form a source follower through the select transistor M_{SEL} . Buffered photodiode voltage V_{out} , which is a function of accumulated signal charge, V_{PIX} , is thus read out as the first signal.

Then, during the hard clamp reset period, pulses ϕ_{VDSW} , ϕ_{RS1} , ϕ_{RS2} turn ON. The source of M_{SEL} is biased at V_{SS} and the transistors M_{RD} and M_{PB} form an inverter. The photodiode voltage V_{PIX} is reset or hard-clamped at the balance voltage V_{RS}^* of the inverter circuit in which the input and the output terminals are shorted by M_{RS1} . The V_{RS}^* can be adjusted by changing the bias voltage V_{BP} . When ϕ_{RS1} turns OFF, reset noise appears on V_{PIX} . However, since the pulse ϕ_{RS2} is still ON, V_{PIX} is immediately forced back to the V_{RS}^* , due to capacitive

feedback through C_2 and C_4 . This period corresponds to the capacitive feedback reset (CFR). Then, when the pulse ϕ_{RS2} is turned OFF, the reset noise appears on V_{PIX} but it is smaller than the reset noise appeared after the hard clamp as analyzed below.

After the reset period, the pulse ϕ_{VDSW} turns OFF and V_{PIX} after the reset is readout as the second signal with the source follower configuration. A light dependent signal voltage V_{sig} can be obtained using CDS, where the second signal V_{out2} after the reset is subtracted from the first signal V_{out1} before the reset.

b. Noise Analysis

When the hard clamp is released by turning the pulse ϕ_{RS1} OFF, the reset noise appears on V_{PIX} and is given by

$$\langle v_{n1}^2 \rangle = G^2 \cdot kT / (C_1 + C_2) \quad (2)$$

where $\langle v_{n1}^2 \rangle$ is a noise power caused by hard clamp operation and G is the voltage gain of the output follower. Since the pulse ϕ_{RS2} is still kept ON, the photodiode voltage is forced back to V_{RS} . Thus, $\langle v_{n1}^2 \rangle$ is completely suppressed, supposing the open loop gain of the amplifier is infinite. However due to parasitic capacitance C_4 , the noise is bounce back to V_{PIX} as $\langle v_{n1}^{*2} \rangle$ when operation mode is changed to the source follower from the inverter configuration.

$$\langle v_{n1}^{*2} \rangle = \left(\frac{C_4}{C_T} \cdot \frac{C_1}{C_2 + C_4} \right)^2 \langle v_{n1}^2 \rangle \quad (3)$$

$$C_T = C_1 + C_2 C_3 / (C_2 + C_3) + C_4 \quad (4)$$

After the capacitive feedback is settled, the pulse ϕ_{RS2} is turned OFF. The reset noise associated with this switching appears and is delivered to the photodiode node through the feedback capacitor C_2 . The resulting reset noise on the photodiode is represented as

$$\langle v_{n2}^2 \rangle = G^2 kT \cdot \left(\frac{C_2}{C_1 + C_2} \right)^2 \cdot \left(C_3 + \frac{C_1 \cdot C_2}{C_1 + C_2} \right)^{-1} \quad (5)$$

Noise of the inverter circuit consisting of M_{RD} and M_{BP} yields voltage fluctuation at V_{PIX} in CFR operation.

The inverter amplifier noise was presented in noise analysis of CTIA pixel [6,9] and the noise $\langle v_{nINV} \rangle$ is given by (6).

$$\langle v_{nINV} \rangle = \frac{G}{C_T} \sqrt{\frac{kT(C_2 + C_4)(C_1 + C_2 + C_4)}{C_L + C_1(C_2 + C_4)/(C_1 + C_2 + C_4)}} \quad (6)$$

Where C_L is the load capacitor connecting to the vertical drain bus.

Here noise suppression ratio R_{SUP} is introduced to express its noise reduction efficiency. R_{SUP} is defined as the ratio of total reset noise to $\langle v_{nFBOFF} \rangle$, which is the reset noise without CFR operation, and is considered to be a reset

noise associated with the total integration capacitance C_T described in (4);

$$R_{sup} = \sqrt{\left(\langle v_{n1}^{*2} \rangle + \langle v_{n2}^2 \rangle + \langle v_{nINV}^2 \rangle \right) / \langle v_{nFBOFF}^2 \rangle} \quad (7)$$

As an ideal case, if $C_4=0$ and inverter amplifier noise are neglected, R_{SUP} can be expressed as

$$R_{sup} \approx \sqrt{\left(1 + \frac{\alpha \cdot \beta}{\alpha + \beta} \right) \cdot \left(\frac{\alpha}{1 + \alpha} \right)^2 / \left(\beta + \frac{\alpha}{1 + \alpha} \right)} \quad (8)$$

where, $\alpha = C_2/C_1$ and $\beta = C_3/C_1$. Since R_{SUP} is expressed by only capacitance ratios, when the pixel size is scaled, the value of R_{SUP} is held constant, providing the same capacitance ratios are used.

The calculated results of (8) as a function of α and β are shown in Fig. 3. The smaller value of R_{SUP} corresponds to greater reset noise suppression efficiency. Smaller α results in greater noise suppression efficiency since the transmission efficiency of the reset noise after CFR to the photodiode node is reduced. On the other hand, smaller β decreases the noise suppression efficiency since the reset noise after CFR appeared on the common node of C_2 and C_3 increases. It is thus desirable to design α as small as possible and β as large as possible. Designing the small value of α is limited by operational range of the inverter amplifier and also requires considerations on the effect of parasitic capacitance. The maximum value of β should be determined by required fill factor, since larger β requires larger silicon area in a pixel.

III. Characterization

A test pixel structure with unit pixel size of $40 \mu\text{m} \times 40 \mu\text{m}$ has been designed and fabricated in single poly, triple metal $2 \mu\text{m}$ CMOS process. Capacitors are formed by MOS capacitors and the third level metal is used only for the light shield. Representative design parameters are $C_1=105 \text{ fF}$, $C_2=20 \text{ fF}$, $C_3=40 \text{ fF}$, $C_4=4.2 \text{ fF}$ and $C_L=1.0 \text{ pF}$. The expected reset noise suppression ratio estimated by (7) is 0.31.

In this particular design, fill factor was designed to be 11% for experimental purposes. However, it has been confirmed with trial layouts that the fill factor of more than 20 % can be obtained for a $6 \mu\text{m} \times 6 \mu\text{m}$ pixel with a $0.35 \mu\text{m}$ design rule.

a. Photo-Conversion Characteristics and Temporal Noise

Fig. 4 (a) and Fig. 4 (b) correspond to ones without CFR and with CFR, respectively. The exposure was controlled by the integration time. The pulse timing for ϕ_{RS2} to disable CFR is illustrated with a dashed line in Fig. 2.

The vertical axis represents the source follower output after CDS operation. An interval between two data sampling was set at $200 \mu\text{sec}$. The temporal noise, both $\langle v_{illuminated} \rangle$ and $\langle v_{dark} \rangle$, represent the standard deviation of 500 samples under illuminated condition and dark condition, respectively. Frequency bandwidth of the

measurement system is limited to 100kHz by a low pass filter. Pixel follower gain was measured to be 0.78 and V_{RS}^* was set at 1.8V.

The noise floor with CFR is $105 \mu V_{rms}$, while the one without CFR is $220 \mu V_{rms}$. The accumulation capacitance C_T was estimated to be 156fF by the photon shot noise behavior and it can yield reset noise of $180 \mu V_{rms}$ with the correlated double sampling (CDS). The noise floor of $105 \mu V_{rms}$ with CFR is much smaller than the estimated kTC reset noise value of $180 \mu V_{rms}$.

b. Reset Noise Suppression Ratio

Fig. 5 shows measured R_{SUP} , which was obtained dividing reset noise with CFR by that without CFR. Source follower noise were measured and subtracted in extraction of the reset noise. The horizontal axis of Fig. 5 indicates the reset voltage of the pixel electrode V_{RS}^* which is controlled by V_{PB} . R_{SUP} barely depends on V_{RS}^* over the measured range of 1.3 to 1.8V

Averaged value of R_{SUP} was 0.39. It is slightly larger than the design target value of 0.31. The value of 0.39 interprets that the reset noise power is reduced to 1/7.

IV. Discussion

A fundamental issue is the achievable noise floor when the pixel size is scaled to less than $6 \mu m$. Estimated residual reset noise, source follower noise and the total noise are plotted in Fig. 6, supposing that C_{PIX} is scaled in proportion to $(FS)^{1.5}$ and $C_1:C_2:C_3=5:1:2$ which is the same ratio in the test structure. From past experiments, it is seen that the trend of the photodiode capacitance per unit area is much slower than that of the source/drain capacitance in order to obtain appropriate quantum efficiency. The thermal noise of the inverter and the source follower are assumed to be constant in the calculation. The pixel size of less than $5 \mu m$ and the read noise of less than $20 e^-$ are feasible with $0.25 \mu m$ design rule and the C_{PIX} is estimated to be 6.9 fF. Supposing signal voltage swing of 0.6V at V_{PIX} , the full well capacity of the $5 \mu m$ pixel is $21 e^-$ thus the pixel dynamic range reaches at 62 dB. The performance of the $5 \mu m$ pixel is comparable to relatively low-end CCD image sensors.

V. Conclusion

The approach employing a circuit design technique to reduce noise is different from the one seen in the CCD image sensors. It will reduce an overhead of process development for the CMOS image sensors as well as fabrication cost, since the noise floor can be reduced to that of the CCD image sensors without employing a special process such as a pinned photodiode fabrication process.

Several trial layouts suggest that the pixel size becomes $17 \sim 20$ times the feature size (design rule) while maintaining more than 20% fill factor. Thus, a use of on-chip micro lens is readily applicable.

References

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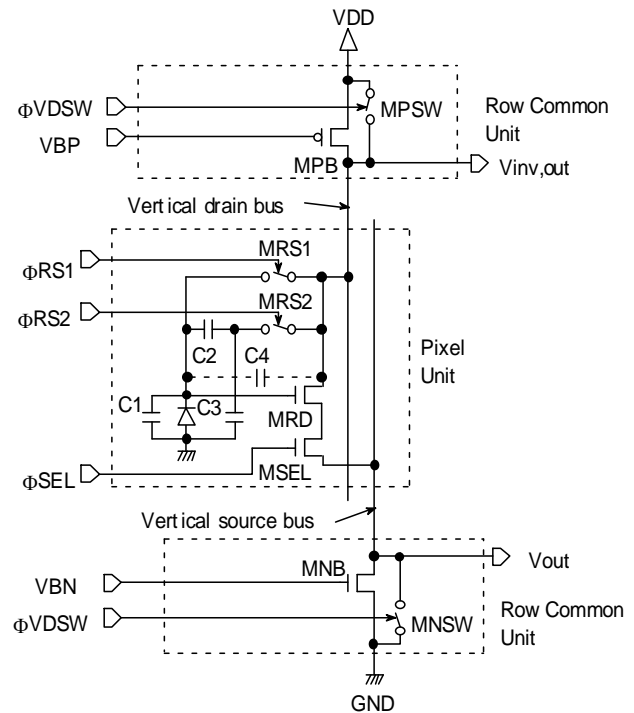


Fig. 1

Circuit configuration of a 4 transistor CFR pixel and related peripheral circuits in a test structure.

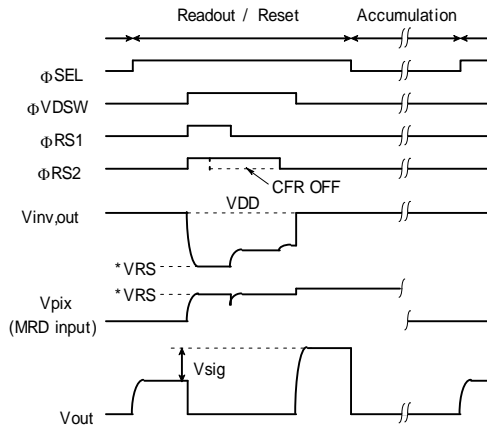


Fig. 2

Timing diagram for the 4 transistor CFR pixel.

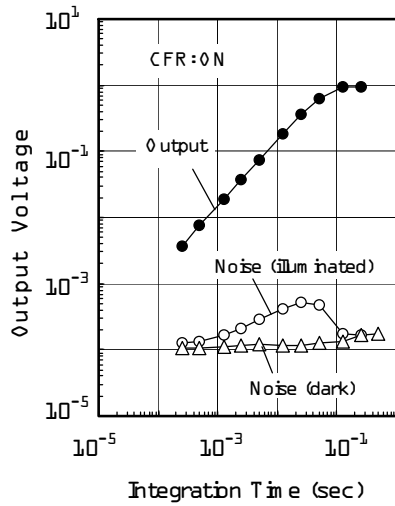


Fig. 4(a) With CFR operation

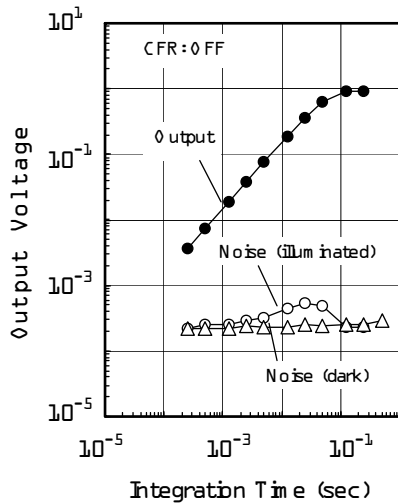


Fig. 4(b) Without CFR operation

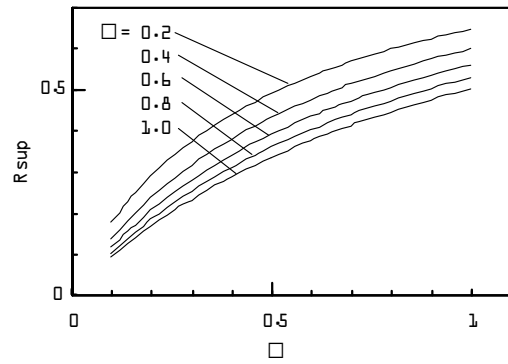


Fig. 3

Calculated reset noise suppression ratio R_{SUP} .

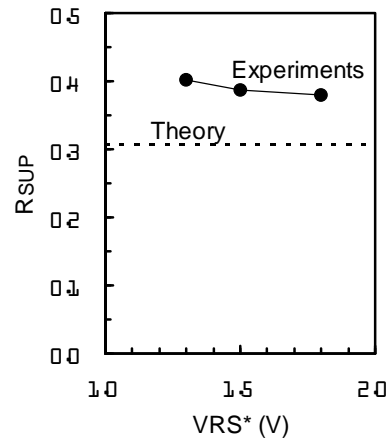


Fig. 5

Experimental results of R_{SUP} .

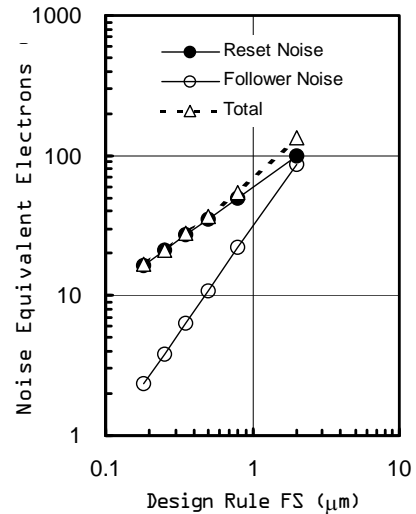


Fig. 6

Estimated noise of the 4 transistor CFR pixel as a function of design rule.