

# Characterization of Pixel Response Time and Image Lag in CMOS Sensors

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## Abstract

Pinned photodiodes used in pixels are capable of being fully depleted, and thus have reduced image lag. Practically, a number of design factors can produce lag in such a pinned photodiode if not taken into account. This paper explores the factors using a simple model. Results of the application of the model to pixels are also shown.

## I. Introduction

Image lag in image sensors is characterized by the presence of information from previous frame(s). An example of this is shown in Fig. 1, where the sensor has been moved between frames: ghost images of the letters are seen. The high-contrast situation shown in Fig. 1 is typical of the worst case for lag. The lag shown in Fig. 1 is for the dark-to-bright transition (the regions of the sensor that image the dark letters do not regain the signal level corresponding to full illumination until several frames have been read out). The analogous bright-to-dark transition lag has been attributed to incomplete extraction of charge from the photodiode during the photodiode reset cycle.

The “pinned” photodiode does not in principle produce image lag. As implemented in Motorola (Fig. 2), it consists of a p-n-p stack with the top p region internally connected to the bottom p (substrate). As the voltage on the n region is increased, the depletion regions from both top & bottom junctions approach one another. When the depletion edges meet, the n region is fully depleted of mobile charges and no further depletion is possible. This ensures that the diode always reaches the same potential when reset (eliminating reset noise) and that no charge can remain in the diode to be subsequently read out. In practice, however, lag can exist in pinned-photodiode pixels, as discussed below.

## II. Lag in the Pinned Diode

One reason for residual charge in the pinned diode is the very large resistance of a fully-

depleted n region. The pinned diode can be modeled as a lumped element non-linear RC delay network (Fig. 3a), with the resistance of each element being a strong function of the voltage (Fig. 3b). In large photodiodes the series resistance of the stages closer to the output can increase the time required to deplete the stages farther away from the output. If the resultant delay is greater than the width of the pulse applied to the transfer gate M2 (Fig. 4 shows a schematic of the 4-transistor pixel used), then charge is left behind in the diode; obviously, the same applies to the reset pulse, when both M1 and M2 are turned on.

This situation has been simulated using the extracted photodiode voltage dependent resistance (Fig. 5). Significant delay is observed with only 4 stages. This simulation models a 4  $\mu\text{m}$  long diode; the time required to deplete 99% of the diode charge can be several  $\mu\text{s}$ . If a large diode is required for low-light applications, then the layout must be optimized to keep the transfer time within acceptable limits.

Even for relatively small pixels, charge can be left behind if the voltage required to deplete section  $i$  is less than that required for sections  $j > i$  (refer to Fig. 3a). In such a case the resistance  $R_i$  rises more rapidly than  $R_j$ , delaying the extraction of charge from  $j$ . If the difference in depletion voltages is large enough, then a certain amount of charge is always left behind in  $j$ -constituting a “fat zero”. This situation is shown in Fig. 6. Some charge does get extracted from the fat zero through thermionic emission over the energy barrier created by  $I$  (Fig. 7). The rate of emission, therefore, decays exponentially with time; and the charge thus extracted is greater for a larger fat zero.

Depending on the times the transfer gate (M2) is on during the reset and transfer cycles ( $t_r$  and  $t_t$ , respectively), the following effects can occur:

- a) If  $t_r > t_t$ , the photodiode over-depletes of electrons. In this case, part of the signal charge is used to restore the fat zero. This results in less signal charge being

transferred; therefore, the transfer characteristic exhibits non-linearity (lower sensitivity) at low light levels. It also produces lag in the dark-to-bright transition.

- b) If  $t_t > t_r$  and RC delay (or fat zero) prevents full depletion during reset, resulting in signal electrons from one frame appearing during succeeding frames; this results in lag during the bright-to-dark transition.

### III. Testing and Measurements

Several pixel designs have been tested using a pulsed-LED source; the LED on and off transients were much less than the readout time of the sensor. The sensor was operated in snapshot mode, where all pixels were reset simultaneously and charge integration also occurred simultaneously.

Fig. 8 shows the effect of over-depleting the fat zero: the lower curve shows increased low-light non-linearity. This also results in dark-to-bright lag (Fig. 9). The effect of the fat zero on bright-to-dark lag is shown in Fig. 10; optimization of the pixel is seen to eliminate this effect.

#### Conclusions:

A mathematical model for image lag in pinned photodiodes has been developed. The results are shown to explain observed lag in both dark-to-bright and bright-to-dark transitions. Understanding these effects has enabled improved pixel designs that minimize them.



Figure 1: An example of image lag in dark-to-bright transition. Two successive frames are shown; the ghost image of the letter N is seen in both frames.

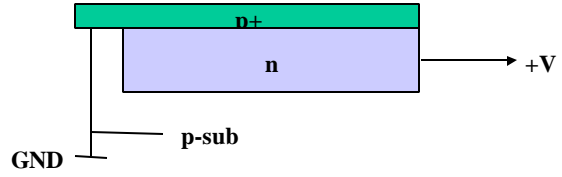


Figure 2: Representation of the pinned diode structure.

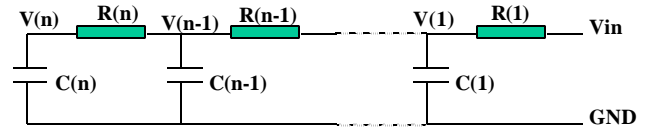


Figure 3(a): Equivalent representation of pinned photodiode.

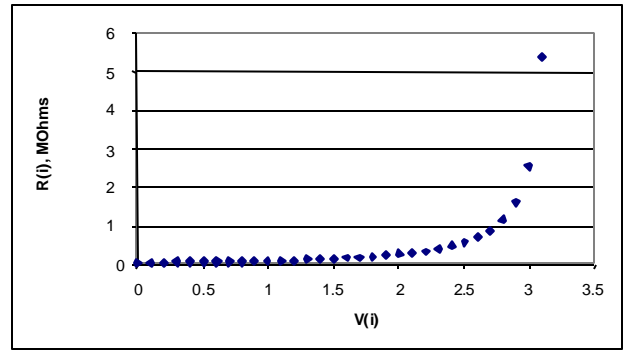


Figure 3(b): Resistance as a function of voltage of a pinned-diode element.

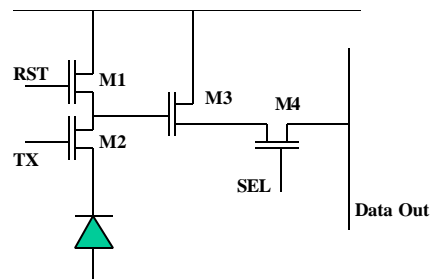


Figure 4: Schematic of the 4-transistor pixel.

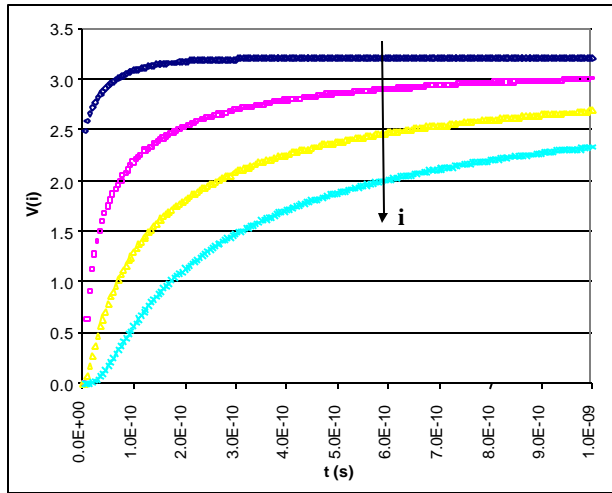


Figure 5: Step-input response of the pinned diode, shown for 4 elements. The length of each element is about 1  $\mu\text{m}$

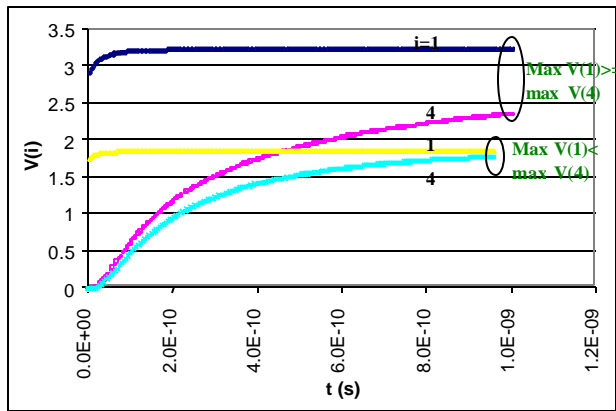


Figure 6 : Step response of pinned photodiode (elements 1 & 4), when the maximum achievable voltage is limited by section 1 (bottom curves) and when it is not (top curves).

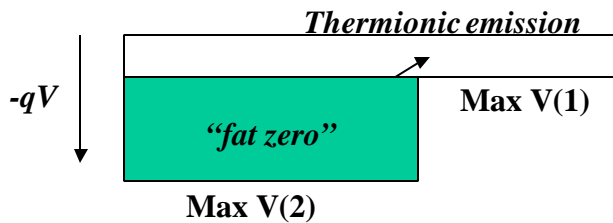


Figure 7: Voltage limiting by stage 1 (to Max. V(1)) creates a “fat zero”, some of which can be extracted through thermionic emission over the energy barrier.

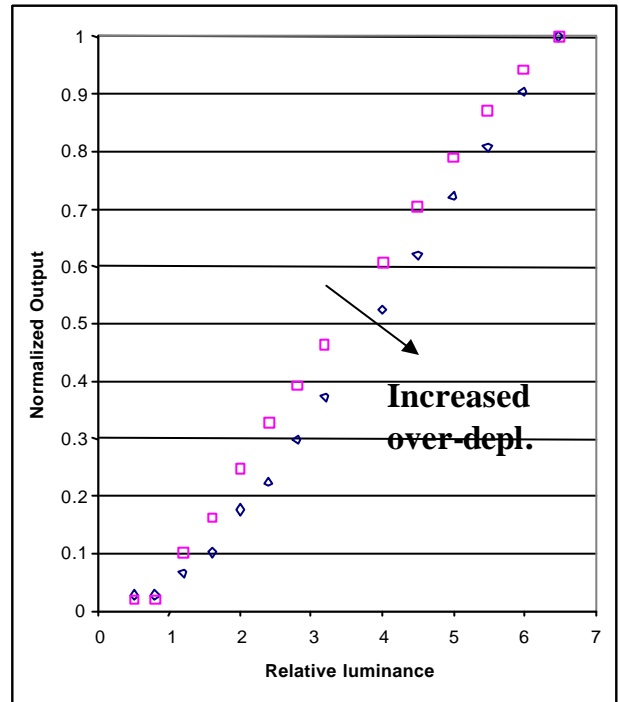


Figure 8 : Over-depleting the fat zero creates low-light non-linearity in the pixel output (lower curve).

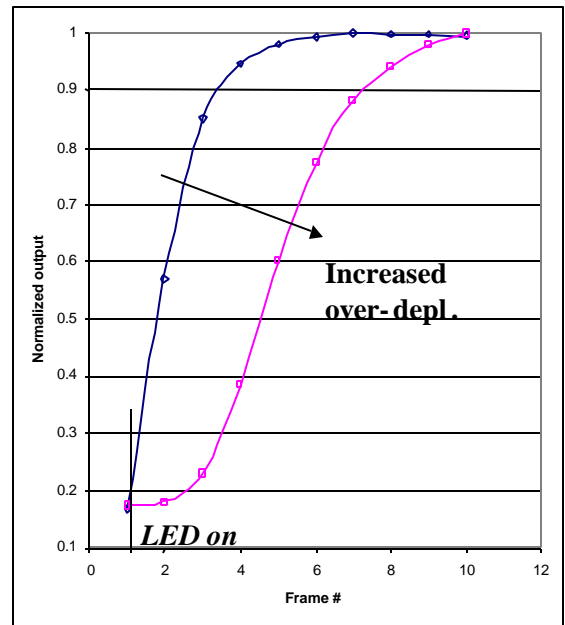


Figure 9: Dark-to-bright transition lag due to over-depletion of fat zero.

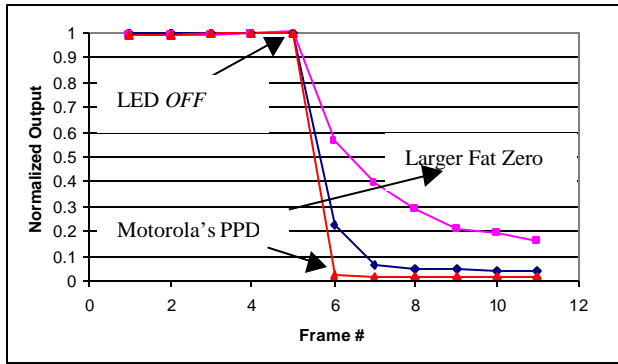


Figure 10 : Bright-to-dark transition lag as a function of the size of the fat zero.