Low dark current CCD register driven through the barrier

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Abstract

In the device described here, the dark-current generated at the Si-SiO_2 interface is completely absorbed into the driving electrodes. And because four phase drive pulses can be used, the device can handle, with high transfer efficiency, several times as much charge as can be handled by a two phase device using hole pinning.

1. Introduction

One of the problems with the conventional CCD register is the large dark-current generated at theSi-SiO_2 interface. Virtual phase CCD's[1] have been used to reduce the dark current to half that in the conventional CCD, and it can be further reduced by keeping all the transfer electrodes in the hole pinning mode[2], except at the instant that charge is transferred. When this is done, however, it is difficult to handle a large amount of charge, because two phase drive pulses must be used. In this paper, we therefore describe a new kind of CCD shift register that has a small dark-current and can handle a large amount of charge. We also show the results obtained when the operation of this register was simulated using the three dimensional numerical simulator "SPECTRA"[3]

2. Dark-current and channel potential

Figure 1 shows the structure of a unit transfer cell. The cell is an inverted version of the conventional photo-diode with vertical over flow drain. Each transfer electrode (top N layer) is separated from the others by a layer of SiO_2. The leakage current between electrodes is negligible, when difference between the potential on the electrodes and the potential on the SiO2 edge is large enough, and leakage currents from an electrode to the channel is almost zero when the potential barrier between the electrode and the channel is high enough. These conditions can be obtained easily by adjusting the impurity concentration of the barrier. For the three cells structure biased as shown in Fig. 2, the simulated leakage current between electrode and between the electrode and the channel were a hundred times smaller than 10^{-20}A which is the current flowing into the channel from p-type substrate. The leakage currents are negligibly small from power consumption view point and dark-current view point. Figure 2 shows electron current vectors in the X=0 plane when light is incident on the Z=0 plane. It is apparent from direction of the vectors that current generated at the Si-SiO_2 interface flows into the driving electrodes. This means the dark-current in this CCD register will be small. Figures 3 (a) and 3(b) shows the minimum barrier potential and the maximum channel potential along the Y direction (the charge transfer direction). It is clear from these figures that the CCD can be driven by the conventional four phases drive pulses.

3. Charge-handling capacity and transfer efficiency

Figure 4(a) shows the transfer inefficiency when electrons set under three electrodes are collected into two electrodes by reducing the voltage of one electrode 7V to 2V in 4ns linearly. We can see that a transfer inefficiency of 10^{-11} is obtained at 5.5 ns transfer time, for signal electrons of 5.16e+4. This amount of charge is three times larger than the charge in the two phase hole pinning device[2] The larger charge handling capability is due to the facts that

(1) The charge storage area is large.
(2) Transferable electrons are decided by drive pulse swing.

Figures 4(b) shows transfer inefficiency when a built-in field is made under a transfer electrode. Comparing Figs. 4(a) and (b), we can see that the transfer inefficiency for 4 ns transfer time is decreased by more than three orders when built in field is made.

The proposed register can thus take the place of the conventional register in the interline scheme CCD sensor. It is also suitable for use in a back-illumination frame transfer CCD sensor with unti-blooming, but not in a front illumination one because light sensitivity become low.

4. Consideration on anti-blooming

As is apparent from Fig.1, the register inherently resist blooming. Figures 5(a) and 5(b) show electron current flow and the maximum channel potential at the X=0 plane under very strong illumination (1.0e-2 watt/cm^2 at the Z=0 plane, λ=550 nm). In these figures, the photo-current flowing into the channel is equal to the overflow current into the electrode. Then, all photo-generated charge seems to flow towards electrode in Fig.5 (a). We can see from Fig.5 (b) that the channel potential difference is larger than 0.7 V. This is high enough to suppers leakage between charge packets to a negligible value, because excess charge is quickly absorbed into electrodes when charge spreads into dark portion.. Then no blooming occurs.

In case of strong illumination, shown in Fig. 5, the number of stored charge under highly biased electrodes reaches 1.006e+5. Some part of this charge is absorbed by electrode during charge transfer. But when the charge is reduced to 5.16e+4, mentioned above the over flow into electrodes becomes negligible.

When the register is designed only as a charge transfer device by increasing barrier concentration slightly, signal charges greater than 8.5e+4 can be handled by same driving pulses. When driving voltages are increased, several times avalanche multiplication occurs for photo-generated charges.

5. Conclusion

We proposed a new CCD register with inherent anti-blooming function to reduce dark-current and to increase charge capacity. The performance of the register was analyzed using three dimensional numerical simulator. This anti-blooming register will be able to handle a large amount of charge with very low dark current.

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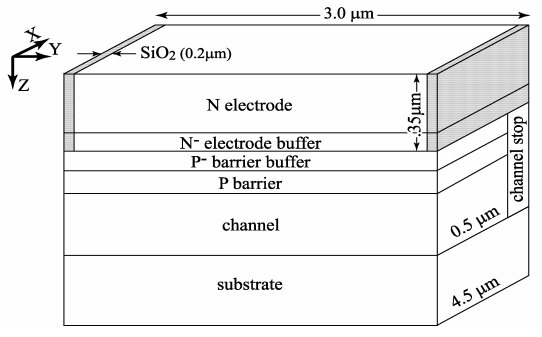

Fig.1 The unit cell structure

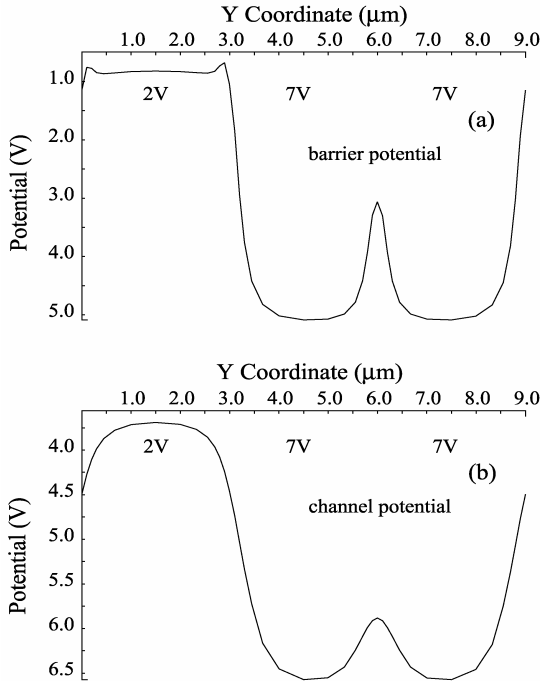

Fig.2 The barrier potential (a) and the channel potential (b) along Y direction

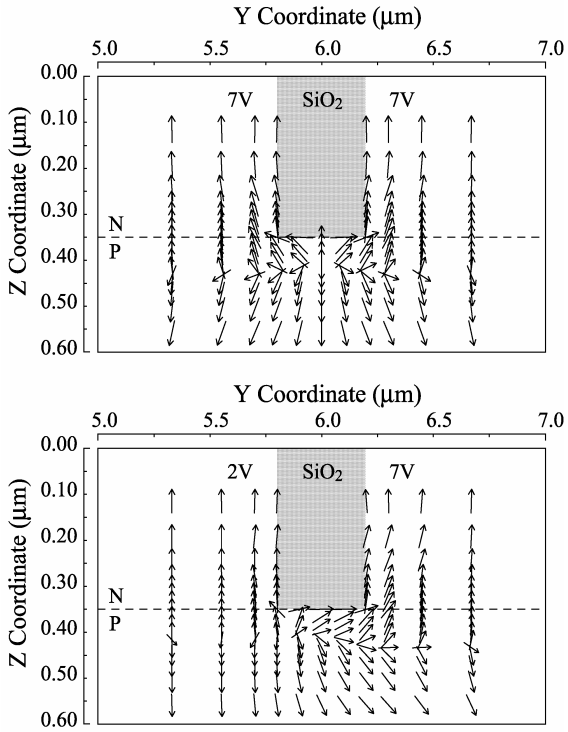

Fig. 3 Electron flow around SiO_2

Electrons generated under SiO_2 flow equally into two driving electrodes in the top figure. And electrons flow from lowery biased electrode to highly biased electrode in the bottom figure.

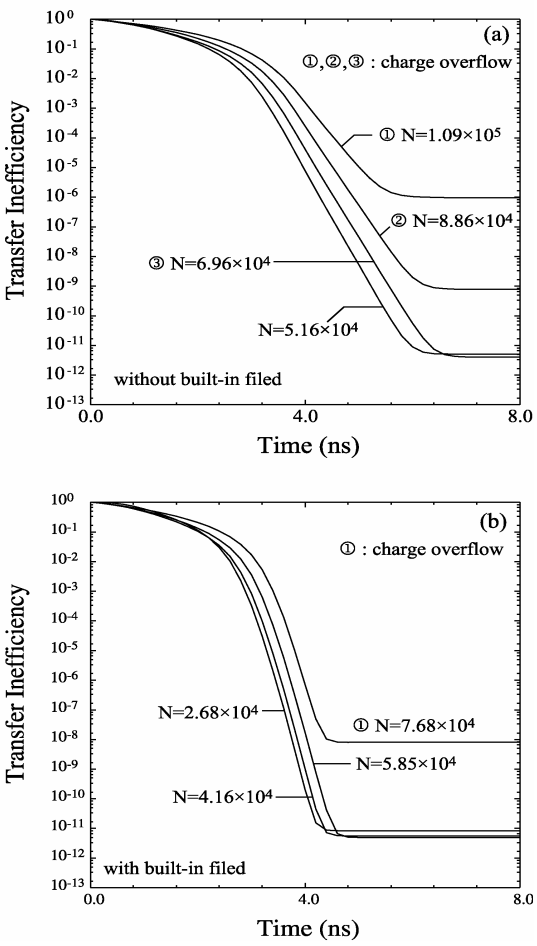

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Fig. 4 Transfer inefficiency

In Fig.4 (a), no built in field is made under an electrode. In Fig. 4 (b), the built-in field is formed under an electrode by additional barrier doping.

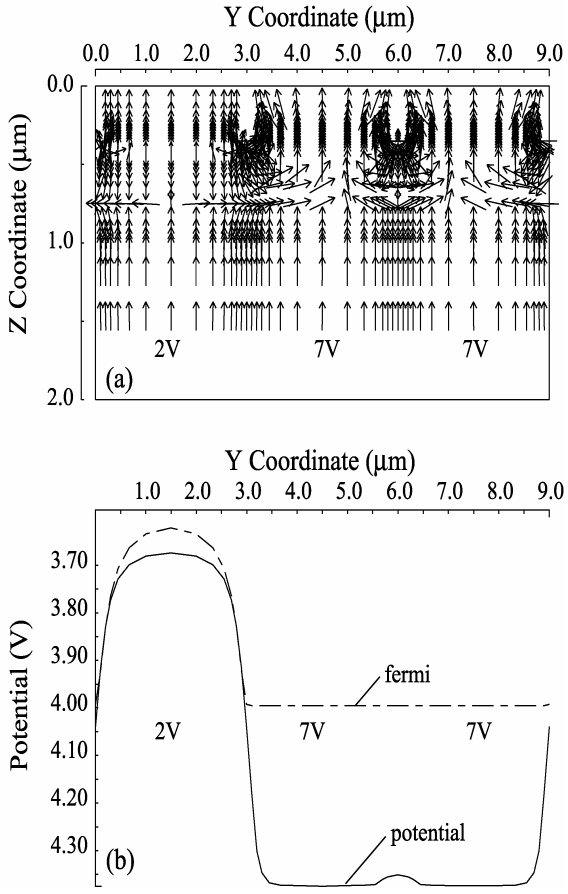

Fig. 5 Electron flow (a) and potential profile (b) along Y direction under very strong illumination. In Fig. 5(a), all photo-generated charge flows towards electrode. In Fig. 5(b), The potential difference (0.7V) is high enough to separate charge packets

References

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3) H. Mutoh: "3D optical and electrical analysis," IEEE Transaction of Electron Devices, ED-44, 1604-1610 (1997).

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