Dual Mode Active Pixel Sensor with Focal Plane Edge Detection

Muahel Tabet and Richard Hornsey

Department of Electrical & Computer Engineering, University of Waterloo, Ontario, Canada N2L 3G1

Tel. (519) 888-4097; Fax. (519) 746-3077; email rhornsey@venus.uwaterloo.ca

ABSTRACT

We report a straightforward, yet robust, VLSI implementation of sampled-data visual edge detection. Our technique adopts the well-known correlated double sampling (CDS) circuit to perform spatial differentiation of the captured image for edges detection functions. Because this circuit is significantly reduces the fixed pattern noise (FPN), it is usually an integral part of most integration-mode CMOS image sensors. Therefore, no additional area is required to include the proposed edge detection functionality in the image sensor. The imager array was implemented using active pixel sensor (APS) technology with dual mode of operation: a logarithmic (continuous) mode with wide optical dynamic range and a linear (integrating) mode with higher image quality. Real-time edge detection has been demonstrated for the both modes of operation. Our technique can be easily extended to perform temporal differentiation, providing a simple method for motion detection. The prototype chip was fabricated using standard 0.5μm CMOS process with an 64 x 64 array. Each pixel has a pitch of 30 μm, with fill factor of ~ 60%. The system operational voltage is 3.3V. Results indicate that the proposed architecture is visible for applications such as adaptive scanning and industrial inspection, where integrated functionalities are advantageous.

I. INTRODUCTION

In recent years, CMOS image sensors have gained significant ground over charge-coupled devices (CCD) [1]-[5], [7] in many applications, especially where integrated functionalities are advantageous, such as in security, biometrics, and industrial applications. The main advantages of CMOS image sensors are their high level of integration [1], random accessibility [2], [6], and low-voltage low-power operation [1], [2], [3]. Accordingly, they offer system-on-chip capability allowing on-chip image processing with low production cost [1], [3], [7]. This has been of great impact in the development of smart vision chips which in addition to their main task as image sensors, they perform real-time image-processing by including parallel analog signal processing circuitry on-chip [2], [8].

Most of designs reported, however, include the on-chip image-processing functionalities at the expense of area, which can limit the spatial resolution achievable. In this paper, we overcame this issue by using the sample-and–hold (S&H) circuits of CDS circuit blocks to perform the required functionality without adding any additional area.

Section II, describes the architecture proposed edge detection system, followed by its theory operation in section III. Measurement results for both logarithmic- and linear-mode of operation are presented in section IV. Finally, results are discussed and concluding remarks are made.

II. ARCHITECTURE OVERVIEW

The functional diagram of the proposed CMOS image sensor with focal plane edge detection is shown in Fig. 1. The edge detection operation starts by activating one row at a time using row address decoder. Output signals from the pixels in the selected row are simultaneously transferred (via each column bus) to CDS S&H circuits (two of them per column) from where they are read out by activating one column at a time using the column address decoder [1]. The difference between the two read-out signals will result in the required edge information. This edge detection operation is similar to that of a normal of integrating-image sensor with CDS circuit. The difference here is that the operation has been modified from double sampling of one pixel in order to remove non-uniformities to the subtraction of adjacent pixels to achieve spatial differentiation. The key parameter here is the timing of the control signals. With appropriate timing, we can combine high-resolution image capture with edge detection functionality on the same chip. Moreover, with a slight modification in the sequence of events in the temporal differentiation from the sample-reset-sample (the usual pattern) to sample-sample-reset, a simple method for motion detection can be easily implemented

III. EDGE DETECTION OPERATION

In this section, we describe the theory of operation of the proposed edge detection function. The Correlated double sampling (CDS) circuits, which are located per column, consist of two sample-and-hold (S&H) circuits as shown in Fig. 2 [8]. In this paradigm, when a row '*n*' is selected using row select signal "ROW", and the S&H switch is turned on by SH_1, each pixel's response in that row is sampled and stored in S&H capacitor C_{j1} located in each column j. All pixels in the selected row are then reset. Similarly, when the successive row '*n+1*' is selected, all pixels' responses in that row are sampled and stored, at commence of "SH_2", in S&H capacitors C_{j2} of the same column. Again all pixels in that row are then reset. Upon the activation of readout column signals "COL.", the two-stored signals are differenced using a differential amplifier (not shown for simplicity). This difference results in the spatial edge detection information of interest here. This equally applies to both modes of operation of the pixel, except that in logarithmic-mode there is no need to reset the pixels after each sampling. In fact, the reset signal is kept always high at V_{dd}. in this mode of operation, by choosing the appropriate Control signal "Cont".

IV. EXPERMENTAL RESULTS

The experimental setup is straightforward, it consists of the CMOS imager test fixture, power supplies to provide V_{dd}, and other biasing, pattern generator, light source, Lux (and/or light intensity power) meter, oscilloscope, and an image capture system using LABVIEW.

At higher illumination, like those resulted from a direct exposure to a lamp, the logarithmic-mode is more suitable. Shown in Fig. 3, the image of lamp and its surface-plot in the logarithmic-mode at light intensity of 7,170 Lux. The detected edge image is shown in Fig. 4.

For the linear-mode operation, we chose light intensity in the range of few hundreds Lux, to ensure good object illumination without saturating the pixels. The contrast presented here are those for ordinary objects like human hand as shown in Fig. 5(a). This contrast is clearly depicted by surface-plot in Fig. 5(b). The image in this figure is shown in lower resolution due to some bad columns in the imager array. The edge detection image is shown in Fig. 6.

V. CONCLUSION

A CMOS image sensor with focal plane image detector was demonstrated in the linear and the logarithmic modes of operation. The linear-mode operation exhibited, in addition to better image quality, a more robustness operation as shown in Fig.s 5,6. The degraded performance of the logarithmic-mode can be attributed to the inherently high fixed pattern noise, and to smaller output swing due to the logarithmic compression as shown in Fig.s 3,4. It is worthwhile to note that the frame rate used here is about 46 f/s. At higher frame rates (~230 f/s) and low illumination, both logarithmic and linear modes showed similar performance. This can be attributed to the fact that the integration-mode operation tends towards the logarithmic at very short integration times.

Other limitations are extrinsic to both mode of operation and related to system level operation. One example is the effect of the shape of the object on edge detection performance, especially in the logarithmic-mode of operation. We note that the performance is highly improved when we used a vertical bar stimuli instead of arbitrary object shapes like that of the hand and/or lamp presented here. This effect originates from our sampling technique (row-spatial) forced by raster scanning used, which makes the edge detector tuned with edges that are parallel to 1-D axis rather than both 2-D axes. Note that the image sensor used here is rotated such that the rows and columns are transposed. Another important point is that our edge detection technique relies on the pixellation of the captured image and provides a straightforward method for obtaining approximate outlines of the imaged objects. For higher resolution sensors, signal differences between the adjacent rows will be smaller than those found here. However, sub-sampling can still be used to estimate object's edge position. In conclusion, these results suggest that our technique is feasible for application such as security, and industrial inspection, where integrated functionalities are important.

ACKNOWLEDGMENT

The authors thank Materials and Manufacturing Ontario (MMO) for their support, and the Canadian Microelectronics Corporation (CMC) for providing the fabrication service of the prototype chip. The authors also thank N. Tu for the layout design.

REFERENCES

[1] N. Tu, R. Hornsey, and S.G. Ingram, "CMOS Active Pixel Image Sensor with Combined Linear and Logarithmic Mode Operation," *IEEE 1998 Canadian Conference on Electrical and Computer Engineering,* Waterloo, ON, Canada, p. 754, 1998.

[2] E. Roca, F. Frutos, S. Espejo, R. D-Castro, and A. R-Vázquez, "Electrooptical Measurement System for the DC Characterization of Visible Detectors for CMOS-Compatible Vision Chips," *IEEE Trans. on Instrumentation and Measurement*, vol. 47, p. 499, 1998.

[3] T. Lulé, S. Benthien, H. Keller, F. Mütze, P. Rieve, K. Seibel, M. Sommer, and M. Böhm, "Sensitivity of CMOS Based Imager and Scaling Perspectives," *IEEE Trans. Electron Device,* vol. 47, p. 2110, 2000.

[4] S. Kavadias, B. Dierickx, D. Scheffer, A. Alaerts, D. Uwaerts, and J. Bogerts, "A Logarithmic Response CMOS Image Sensor with On-Chip Calibration," *IEEE J. Solid-State Circuits,* vol. 35, p. 1146, 2000.

[5] E. Fossum, "CMOS image sensors: Electronic camera on a chip," in *Proc. Int. Electron Device Meetings*, p. 17, 1995.

[6] M. Tabet, N. Tu, and R. Hornsey, "Modeling and characterization of logarithmic CMOS active pixel sensors, " *J. Vac. Sci. Technol. A,* vol. 18, p.1006, 2000.

[7] H. Wong, "Technology and device scaling consideration for CMOS imagers," *IEEE Trans. Electron Device,* vol. 43, p. 2131, 1996.

[8] S. Mendis, S. Kemeny, R. Gee, B. Pain, Q. Kim, and E. Fossum, "CMOS active pixel image sensors for highly integrated imaging system," *IEEE J. Solid-State Circuits,* vol. 32, p. 187, 1997.

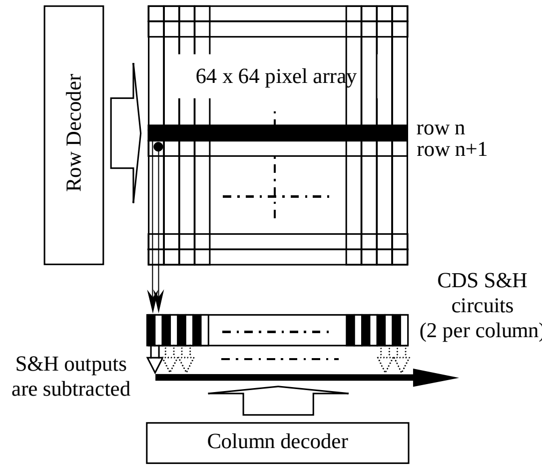

Fig. 1. Functional block diagram of the proposed system. Row "n" (black) is sampled in the left S&H while row "n+1" (white) is sampled in the right one. The outputs are then subtracted.

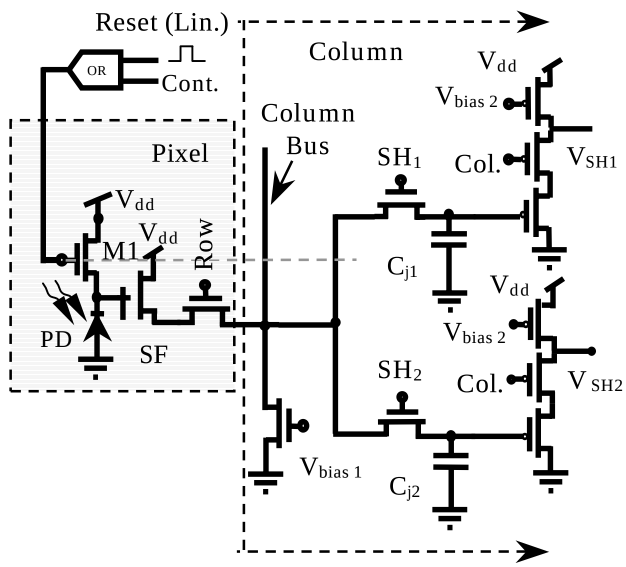

Fig. 2. The correlated double sampling circuit [8] used here for spatial edge detection is shown along with the dual mode APS pixel. The mode of operation is determined by selecting the proper state of "Cont." signal.

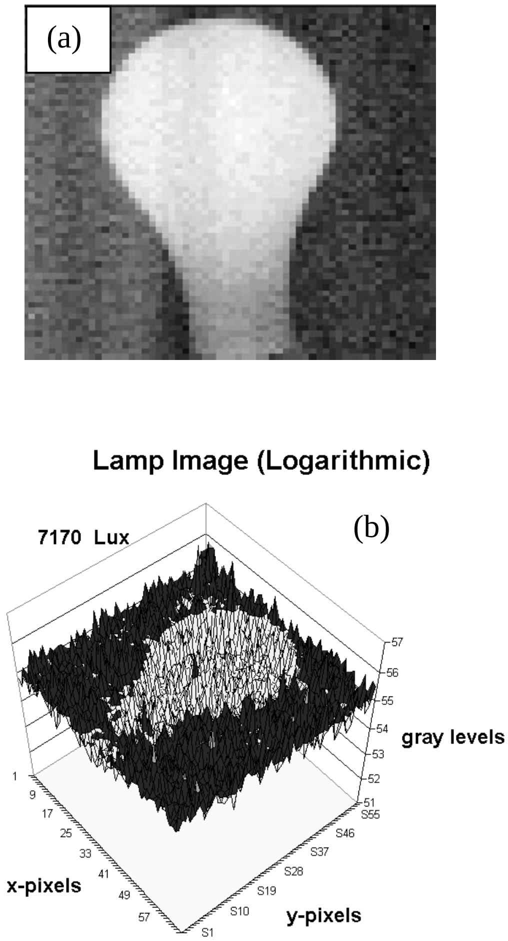

Fig. 3. Captured lamp image (at 7170 Lux) in the logarithmic-mode (a). Image surface-plot clearly shows image contrast (b).

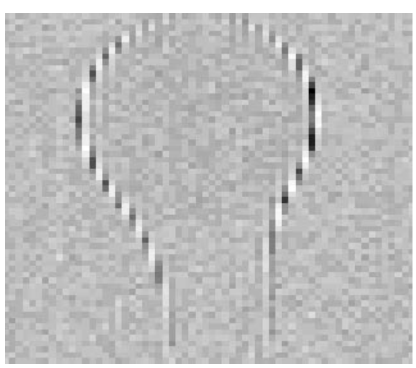

Fig. 4. Edge detection of the lamp captured the logarithmic-mode (7170 Lux) using CDS circuit.

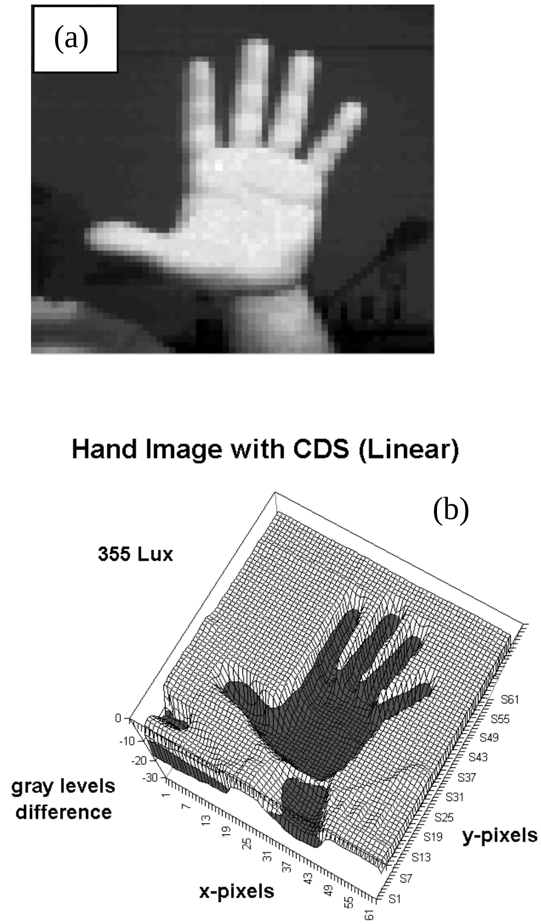

Fig. 5. Captured hand image (at 355 Lux) in the linear-mode using CDS circuit to enhance image quality (a). Image surface-plot clearly shows image contrast (b).

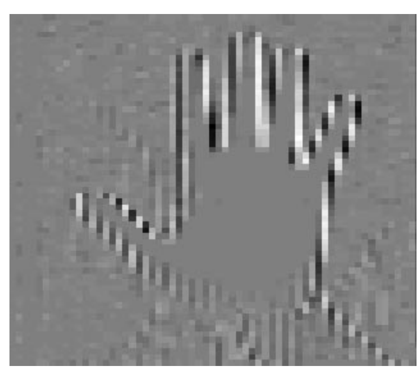

Fig. 6. Edge detection of the hand captured in the linear-mode (at 746 Lux) using CDS circuit with the proposed timing pattern.