A VGA ISIS for a Video Camera of 1,000,000 fps: A Proposal

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Abstract

A next-generation image sensor of 1,000,000 fps is proposed. It is basically an ISIS, In-situ Storage Image Sensor. The spatial resolution is sufficiently large. The format is originally a half VGA, i.e., 320x480 pixels, and the structure is buttable. Therefore, it can be expanded to a VGA sensor. The dynamic range is 8 bits. While the total number of consecutive images is only 100, an overwriting mechanism is installed in the chip. Therefore, it is easy to synchronize the image capturing to occurrence of a target event.

I. Introduction

An image sensor capable to capture images at 1,000,000 fps is proposed. The format is VGA, i.e., the pixel count is 640x480. The total number of frames, however, is limited to 100. During image capturing phase, the image signals are stored in a CCD attached to each photogate without readout from the sensor. Therefore, the sensor is an ISIS, In-situ Storage Image Sensor.

Various ideas to realize the ISIS have been proposed by the authors [Etoh et al. 1999, Poggemann et al. 2001]. New ideas are added in the layout proposed in the paper. The basic layout and new operation schemes are presented. The performances are being pre-tested by simulations.

II. Basic Layout

The concept is illustrated in Fig.1 and Fig.2. Fig. 1 shows a pixel, consisting of

(1) a large photogate,
(2) a linear CCD storage,
(3) a vertical readout CCD, and
(4) a double-functioned CCD element (a) for switching between the storage and the readout CCDs and (b) for overwriting drainage.

Fig.2 shows layout of pixels around the center line of the chip.

An ISIS was proposed and manufactured by Kosonocky et al [1996]. The major advantage of the proposed sensor is a linear one-direction transfer of charge packets during an image capturing phase, while the sensor by Kosonocky et al. employed the SPS, series-parallel-series, configuration for in-situ CCD storage, which utilizes two-direction transfer with right-angle change of transfer direction. Thus, the structure of the metal wire shunting and/or doping of the proposed design is much simpler, which makes the size of the pixel reduced and the pixel count increased.

The one-direction transfer during an image capturing phase became possible by introducing the in-situ storage of a linearly-elongated CCD channel slanted to the square grid of the phtogate array, as shown in Fig.2.

III. Vertical Readout and Switching CCDs

Switching CCD had been proposed by the second author into the ISIS design. It is placed at a cofluence of two CCDs at the lower end of a storage CCD and that of a segment of a vertical readout CCD for a pixel.

The CCD transfer scheme is a standard four-phase one, which requires four metal shunting wires to increase the transfer rate. Therefore, introduction of a vertical readout CCD requires additional four metal shunting wires on or along one CCD channel for vertical readout. It consumes a lot of space, since pitch of shunting wires should be larger than a critical value to keep the yield rate reasonable. An innovative scheme to decrease the number of shunting wires for the vertical readout CCD from four to two is proposed by the first author.

The scheme is conceptually explained in Fig.3.

The linear storage CCD is operated with a set of four electrodes on a CCD element, i.e., A1, A2, A3 and A4, while the vertical readout CCD with A1, B2, A3, B4. Namely, two of four electrodes, A1 and A3, are commonly used, and two additional electrodes, B2 and B4, are placed on the vertical readout CCD instead of A2 and A4.

Transfer voltage patterns for A1 and A3 are always those of standard four-phase transfer as shown in Fig.3 (a).

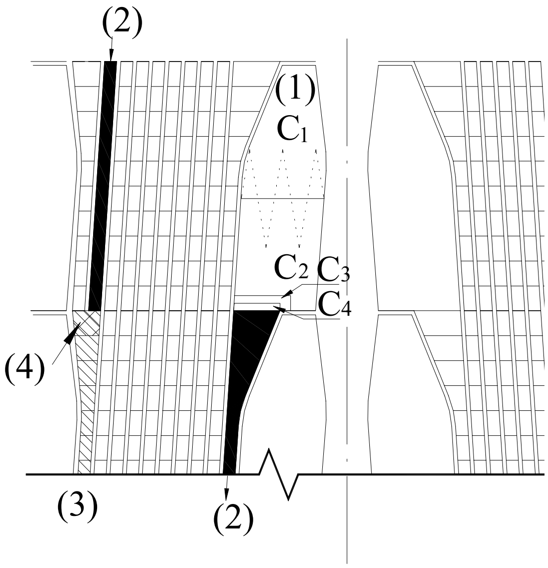


Fig.1 Pixel layout : detail (1) a large photogate (2) a linear CCD storage (3) a vertical readout CCD (4) a double-functioned CCD element (a) for switching between the storage and the readout CCDs and (b) for overwriting drainage

When voltage patterns for A2 and A4 (or B2 and B4) are the same as standard ones, charge packets are simply transferred.

If the voltage of A2 (or B2) is fixed at the higher level and A4 (or B4) at the lower level, A4 (B4) works as a blocking gate and A2 (or B2) as a reserving gate, and a charge packet is always kept beneath [A1 and A2] or [A2 and A3] (or [B1 and B2] or [B2 and B3]) alternately, as shown in Fig. 3(b). Consequently, without B1 and B3, the linear storage CCD and the vertical readout CCD are independently operated either as transfer CCD or as storage CCD.

Therefore, only two metal shunting wires for the B2 and B4 electrodes should be placed along one CCD channel for vertical readout, which greatly increases the yield rate of the sensor compared to that with four metal shunting wires along the channel.

IV. Zigzag n-doping on Large Photogates

In high-speed image capturing, higher light sensitivity is the second target in the design of a sensor or a camera, following the highest frame rate. The area of the photo-sensitive area should be as large as possible. In the layout shown in Fig.1 and Fig.2, the length of the photo-receptive area is more than 50 microns, which is about ten times larger than that of a standard CCD element.

To achieve on-chip high-speed shuttering and high-speed electron transfer on the long

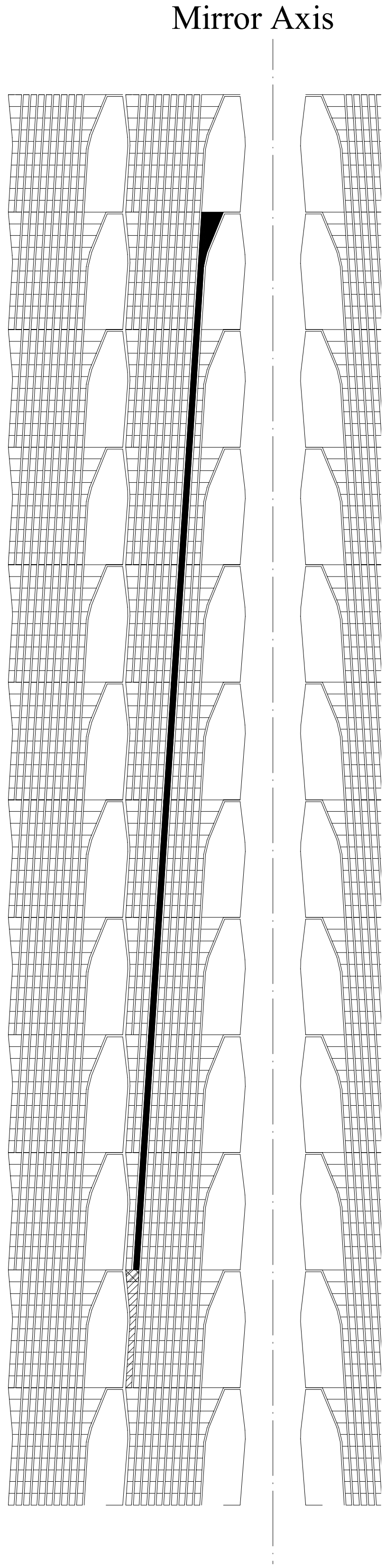
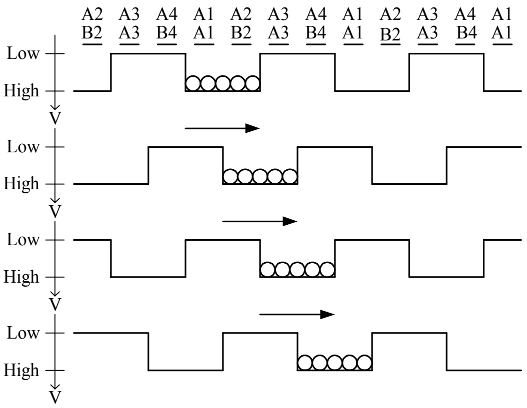
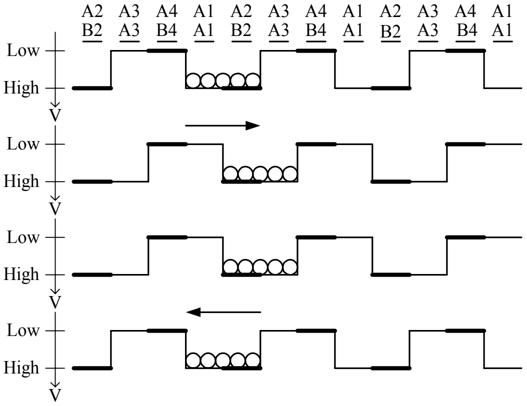


Fig.2 Pixel layout around the center line



(a) Transfer phase



(b) Storage phase

Fig.3 Operations of two adjacent CCD channels of 4-phase transfer with 6 shutting wires

photo-receptive area, photogates are employed, i.e., thin membrane electrodes (C1 and C2) are placed on the photo-receptive area. As shown in Fig.1, the first two gates among four for four-phase transfer of the photogate are large and the last two, C3 and C4, are small to be smoothly connected to the input part and, then, to the linear storage CCD.

To increase transfer speed of electrons on the photodiode, Kosonocky et al. applied additional three times of n-type surface doping to the photodiode area. Then, the doping concentration was increased toward the input gate.

To reduce the additional n-type surface dopings, some new ideas are introduced and tested by simulations. The most promising one among them is a zigzag partial deep n-doping with a dense surface n-doping all over the photogate area, shown in Fig.4. In Fig.5, the potential profile for the doping pattern is shown. Transfer time of an electron on the photogate is compared in Table 1, for the cases with and without the zigzag doping. As shown in Fig.6, smoothly-increasing potential profile along the center line of the photogate is realized. The transfer time is reduced to about 1/10 to 1/50, from 602 or 2,235 ns to 46 ns.

V. Buttable Design

As shown in Fig.2, the storage area can be excluded for the design of mirrored (or rotated) pair of ISISes, which provides a linear wide space at the center of the chip, making the buttable design practical. Together with the increase of the pixel count of the half sensor, the VGA format can be realized for ultra-high speed image capturing.

The pixel size is 51.0 x 51.0 square microns. The width of the storage area is about 40 microns, which provides 40-micron space at the center of the buttable design.

VI. Performance

The size of a storage CCD element is 3.3 microns x 5.1 microns, which can be non-square since it is not for Imaging, but only for storage. Charge handling capacity is proved to be about 15,000 by simulation, which provides more than 8 bits in gray-scale for the noise level of 40 electrons.

The expected performance is tabulated in Table 2.

Conclusions

A VGA image sensor of 1,000,000 fps is proposed. The basic layout and various ideas to support the high performance are presented. Preliminary simulations proved it's realistic.

References

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2) D. Poggemann et al., "An ultra–high-speed camera with an In-situ Storage Image sensor", Proc. of 2001 IEEE Workshop on CCD and AIS, to be published.

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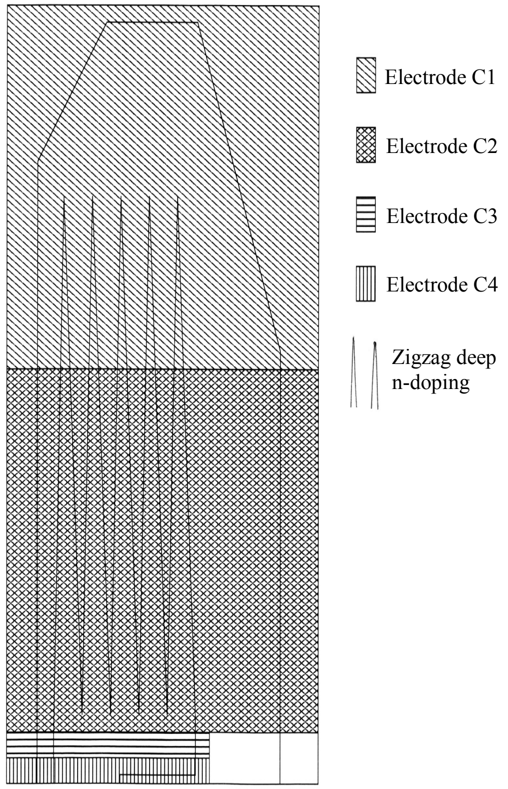

Fig.4 Large photogate

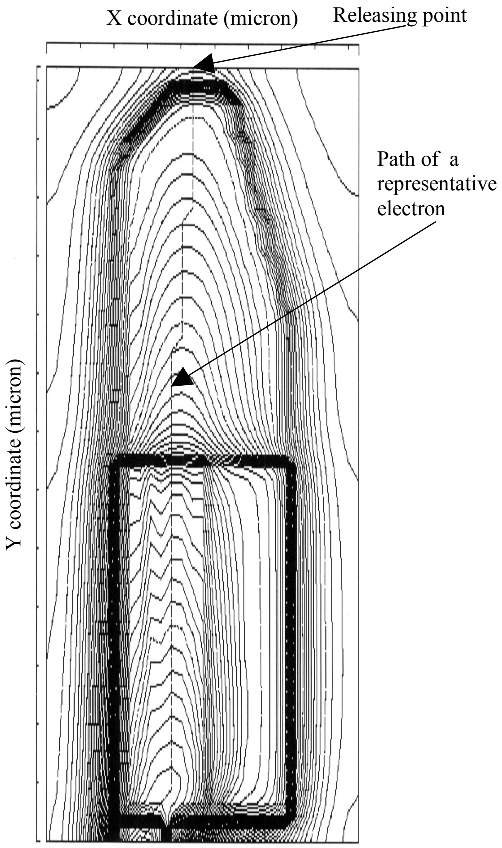

Fig.5 Potential profile

Table 1 Reduction of electron transport time by zigzag deep-n doping on a large photogate

DN-Doping pattern	Transport time (ns)
Zigzag doping	46
Large rectangular doping	602
No doping	2,235

Table 2 Performance of a proposed ISIS

Basic structure	Buttable ISIS
Pixel count	320x480 (Single Sensor) 640x480 (VGA for Buttable Design)
Number of consecutive images	100 frames
Size of a CCD element	3.3 microns x 5.1 microns
Size of a pixel	51.0 microns x 51.0 microns
Size of a photo-receptive area of a single sensor	16.32 mm x 24.48 mm
Fill factor	15%
Charge handling capacity	12,000 electrons
Grey levels	8 bits
Overwriting mechanism	included

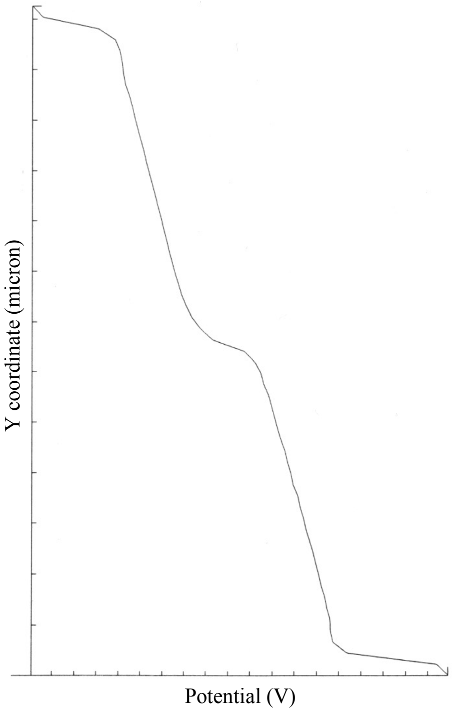

Fig.6 Smooth potential profile along an electron path