Small CMOS Pixel Design with Single Row Line

Vladimir Berezin
Photobit Corp.
135 N. Los Robles Ave., Pasadena, CA 91101
vberezin@photobit.com

Abstract

A number of small size pixels for CMOS image sensors using just one row line to control reset and select transistors has been designed, fabricated and characterized. The elimination of an additional control line and the associated contacts provides more pixel area that can be allocated to the photodiode. On one hand, this gives a substantially higher pixel fill factor, consequently higher quantum efficiency and optical sensitivity. On the other hand, it allows significant reduction of a pixel size. The smallest achievable pixel pitch is determined as CMOS process feature multiplied by a factor of 10. High performance of CMOS image sensors with 5.6 and 3.9 micron pixel pitches fabricated by different foundries with 0.5; 0.35 and 0.25 micron process features is reported.

I. Introduction

Small pixel size with high fill factor is one of the top goals of almost any CMOS image sensor design, especially in consumer electronics [1], [2]. Fill factor is the percentage of pixel area occupied by the photodiode. The proposed small pixel design reduces overall image sensor cost, keeping the pixel fill factor and quantum efficiency at a competitive level. The main aim of this approach to pixel design is to reduce the number of control lines necessary to drive the imaging pixel array. Our proprietary technique for reducing the number of control lines is to provide multiple control signals on lines shared by adjacent pixel rows in the array. We have named this single row line design as shared reset-select signal approach. This design brings about many advantages including higher quantum efficiency for the sensor, greater space resolution in the pixel array, and reduced number of interlevel contacts (e.g. metal to polysilicon) in the sensor circuit.

II. Architecture and Operation

Our approach features an imaging system that includes a plurality of pixels arranged into an array of lines forming rows and columns. Each of the pixels includes a photodiode that collects photo-generated charge when exposed to light, a source follower circuit that generates an output signal indicating the amount of charge collected by the photodiode. The system also includes a line decoder circuit. This circuit comprises a plurality of control lines and a block that delivers select signals and reset signals over the control lines. Each control line connects electrically to two different pixels in two different lines. The control line delivers a select signal to one pixel in one of the lines and delivers a reset signal to one pixel in the other line. The select signal causes the pixel in the first line to set its signal on the output line, and the reset signal clears information from the photodiode in the second line. Fig.1 illustrates the schematic and timing diagrams for CMOS image sensor with single row line and shared reset-select approach.

III. Pixel Layout Design and Scaling

Since three transistors, signal lines and their associated contacts are placed in each pixel, and since contacts typically consume a large amount of pixel area due to the required overlap and spacing of various layers, the fill factor for the pixel is reduced because of the large area consumed that could otherwise be used for the photodiode. The metal lines are optically opaque and can occlude regions of the photodiode in order to fit them into the pixel pitch. This also reduces the fill factor of the pixel. Decreasing the fill factor reduces the sensitivity and saturation signal of the image sensor. Fig. 2 shows the pixel design proposed to overcome the limitations described above. This illustrates the three alternative pixel designs layouts with shared reset-select signal approach.

Table 1. Minimum pixel pitch vs. CMOS process feature size and design

CMOS Process Feature Size	Type ”A”	Type ”B”	Type ”C”
0.5µm	5.0µm	5.5µm	6.0µm
0.35µm	3.5µm	4.0µm	4.5µm
0.25µm	2.5µm	3.0µm	3.5µm

Pixel pitch could range from 2.5µm to 5µm depending on the CMOS process used (0.25µm, 0.35µm or 0.5µm). Table 1 shows the minimum pixel pitch versus CMOS process feature size

and design type. The smallest achievable pixel pitch could be determined as CMOS process feature multiplied by a factor of 10. This innovative active pixel design allows Photobit to attain the world's smallest pixel size.

IV. Experimental Results

A number of CMOS image sensors using just one row line to control reset and select transistors has been developed, fabricated and characterized. Some of them are test-chips and have a fully flexible open architecture (FFOA).

Table 2. Image sensor performance vs. pixel pitch and foundry process

Pixel pitch, μm	5.6			3.9	
Array size, H x V	640x480			1,600x1,200	
Foundry	"A"	"A"	"B"	"A"	"C"
Process feature. μm	0.5	0.35	0.35	0.35	0.25
Capacitance, fF	3.5	5.0	2.9	3.2	2.0
Conversion gain, μV/e	46	32	55	50	80
Saturation signal, V	1.3	1.8	1.9	2.3	2.1
Saturation charge, Ke	28	56	35	46	26
QE, % @ 550nm	21	50	39	23	25
Sensitivity, V/lux*s	1.6	2.6	3.5	1.0	1.7
Dark current e/s @ 20C	400	260	220	140	130
Microlens	no	yes	yes	yes	yes

All data refer to Floating Diffusion (FD); Vdd=3.3V

The others have a camera-on-a-chip architecture and include ADC, timing, auto-exposure, and programmable gain controls. Fig. 3 shows the sensor response (signal and noise vs. light intensity) at the column node that calculated from the digital output of the camera-on-a-chip with pixel array operated in soft reset mode. Soft reset mode means that the voltage on the source of reset transistor is not equal to the voltage applied to the drain. This mode is used to reduce kTC noise [3] and increase saturation signal. The combination of shared reset-select line approach with soft reset mode leads to the appearance of "dead zone" for low-light signals due to operation of reset transistor in sub-threshold mode. The signal curve with "dead zone" affects the sensitivity and dynamic range of the image sensor, performance measures that are critical to obtaining good image quality. The reset pulse with boosted amplitude eliminates non-linearity in the small signal region and increases saturation signal. The voltage gain of the pixel source follower was measured as 0.7. Table 2 summarizes the image sensor performance versus pixel pitch and foundry process. Fig. 4 and 5 show quantum efficiency and color images obtained from CMOS image sensors with 5.6μm and 3.9μm pixel sizes.

V. Conclusion

The functionality of a three-transistor active pixel CMOS image sensor is maintained while eliminating the separate row line for reset or select transistors. This is done by sharing the reset control signals in one row with the select control signals means of an adjacent row. The advantages are higher fill factor or smaller pixel size. An inability to reverse scan in vertical direction is the principal disadvantage of this approach.

Acknowledgment

This presentation summarizes the achievements of Photobit in the area of small pixel design. The results were made possible by the effort of many people at Photobit as well as at Tower Semiconductor, UMC and TSMC. Their contributions are greatly appreciated. The author would like to extend his special appreciation to Ilya Ovsiannikov, Gennady Agranov and Grzegorz Waligorski for their dedicated and tremendous effort in sensor characterization. I also wish to express my sincere thanks to Eric Fossum for his long time support, many helpful discussions and opportunity to enter the world of CMOS imaging.

References

[1] E. R. Fossum, "CMOS Image Sensors: Electronic Camera-On-A-Chip", IEEE Trans. Electron Devices, Vol. 44, No. 10, pp.1689-1698, Oct.1997.

[2] H. Wong, "Technology and Device Scaling Considerations for CMOS Imagers", IEEE Trans. Electron Devices, Vol. 43, No. 12, pp.2131-2142, Dec. 1996.

[3] B. Pain et al. "Analysis and enhancement of low-light-level performance of photodiode-type CMOS active pixel imagers operated with sub-threshold reset", IEEE Workshop on CCD and Advanced Image Sensors, pp.140-143, 1999.

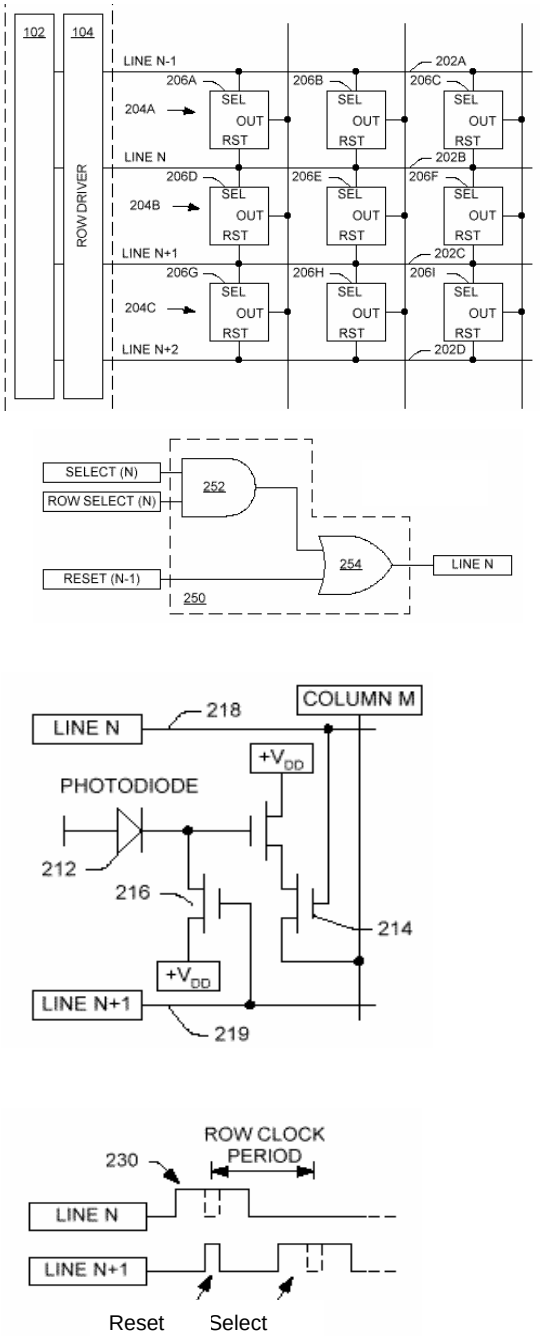
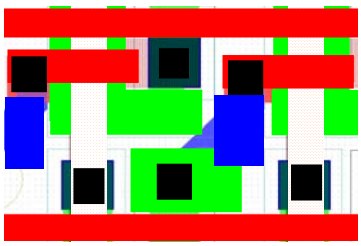
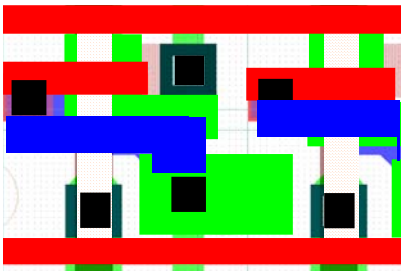


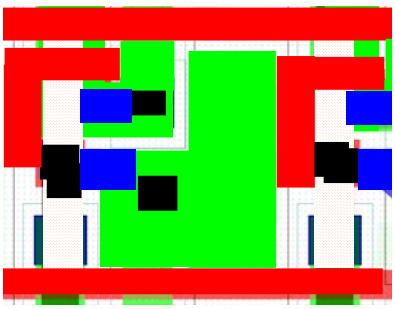
Fig.1. Schematic and timing diagrams of CMOS image sensor in which a single control line is shared by two adjacent rows of pixels.



Type “A”

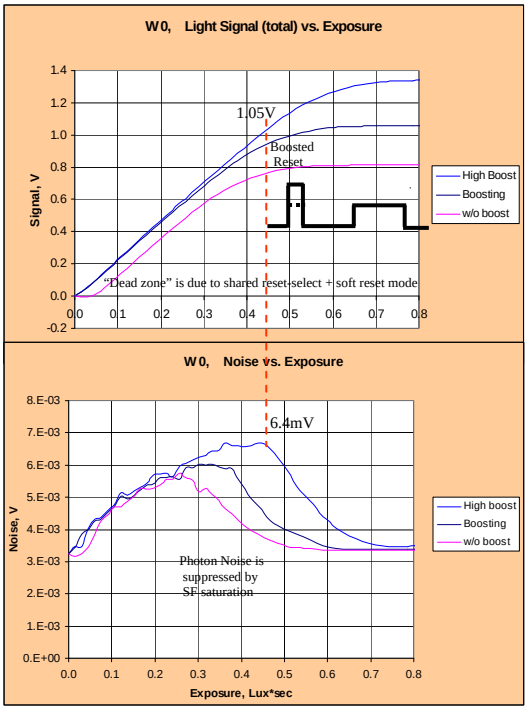


Type “B”



Type “C”

Fig.2. The alternative CMOS pixel design layouts with single row line.



Pixel size =5.6µm; Process feature =0.35; Vdd =3.3V;
Maximum linear signal on FD = 1.05V: 0.7 = 1.5V;
Maximum linear signal charge =1.5V: 55uV/e =27Ke;
Maximum SNR = $(27Ke)^{1/2}$ = 164 or 44dB;
Saturation signal on FD = 1.35V: 0.7 = 1.93V;
Saturation signal charge = 1.93V: 55uV/e = 35Ke

Fig.3. Signal and noise at the column node vs. light intensity for CMOS image sensor with a single row line.

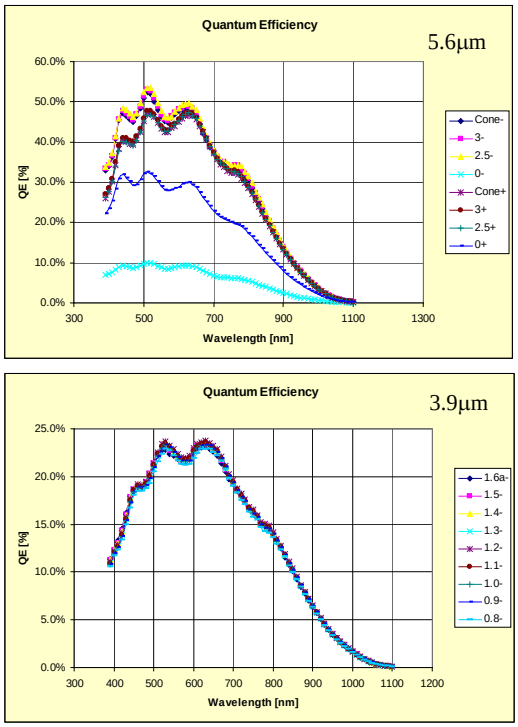


Fig.4. Quantum efficiency of CMOS image sensors with a single row line, microlenses, and variations in pixel design and size (5.6 and 3.9µm) fabricated by the same foundry (0.35µm CMOS process).

640 x 480 array; 5.6µm pixel; 0.5µm process

1,600 x 1,200 array; 3.9µm pixel; 0.35µm process

Fig.5. Color images captured by different CMOS image sensors with a single row line.