A CMOS Image Sensor with Non-Destructive Intermediate Readout Mode for Adaptive Iterative Search Motion Vector Estimation

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Abstract
A high-speed non-destructive CMOS image sensor with bi-directional multiple charge transfer active pixel scheme is presented. The high-speed intermediate pictures are used in the motion vector estimation with adaptive iterative search. The sensor has an ability to cancel FPN of intermediate image. The proposed adaptive iterative search with high-speed non-destructive intermediate pictures reduces the complexity of full search motion vector estimation by a factor of 1/13 in average.

1. Introduction

On-sensor processing is very useful for low-power image compression. On-sensor video processing with optimized algorithms further reduces the power.

In order to realize a low-power motion vector estimator for video compression, we proposed an on-sensor implementation by utilizing high-speed imaging. In the on-sensor application, high-speed pictures can be transferred easily to the signal processing circuit. By using high-speed images, the computational complexity of motion vector estimation is greatly reduced, since a wide search area is not required.

However, practical video compression requires video-rate pictures with sufficient signal accumulation and motion vector of video-rate pictures.

This paper describes a CMOS image sensor that captures high-speed intermediate pictures and also video rate pictures with sufficient signal accumulation for focal plane motion vector estimation based on iterative block matching [1]. An adaptive search strategy for the iterative block matching to further reduce the computational power of the motion vector estimation is proposed.

2. Non-Destructive APS

2.1. High-Speed Non-Destructive Intermediate Imaging

In a typical 3-transistor type active pixel sensor (APS), accumulated signal is readout non-destructively through a buffer. In order to cancel fixed pattern noise (FPN) due to variation of in-pixel source follower input transistor between pixels, reset voltage of the FD node has to be readout also.

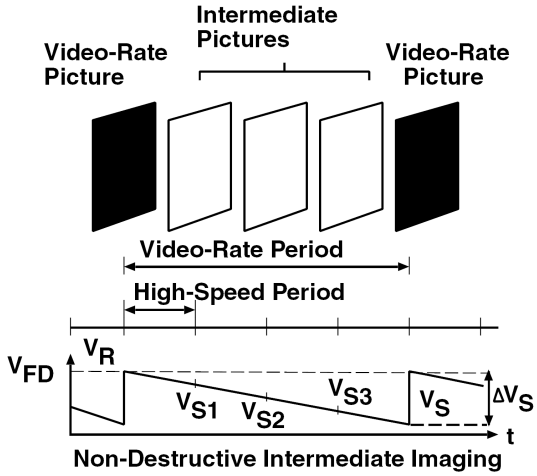

Fig. 1. Operation principle of the high-speed non-destructive intermediate imaging

In case of conventional high-speed imaging, since the accumulated signal is destructed in each time of signal readout, the signal quality is degraded due to shorter accumulation time.

Fig. 1 shows the operation principle of the non-destructive high-speed intermediate imaging. In this method, the intermediate pictures between two video-rate pictures are readout without destroying the accumulated signal. The accumulated signal charge is destroyed in the readout of video-rate pictures only. Therefore, the charge can be accumulated during video-rate period.

However, in the typical 3-transistor type APS, the sensor does not have an ability to cancel the fixed pattern noise (FPN) for intermediate high-speed pictures, because the intermediate high-speed pictures have to be read out without reset operation.

2.2. High-Speed Non-Destructive Intermediate Imaging with FPN Cancellation

High-quality intermediate pictures are required

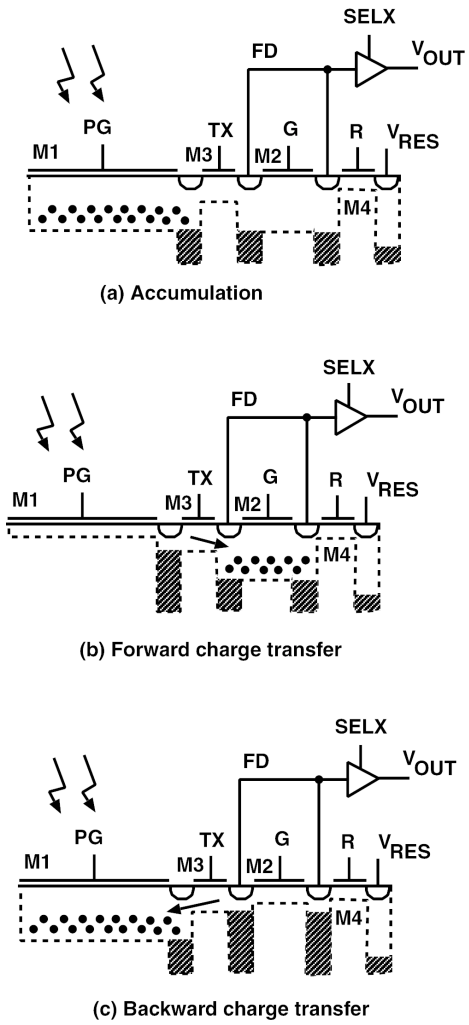

Fig. 2. Active pixel with bi-directional multiple charge transfer scheme for non-destructive imaging with FPN reduction.

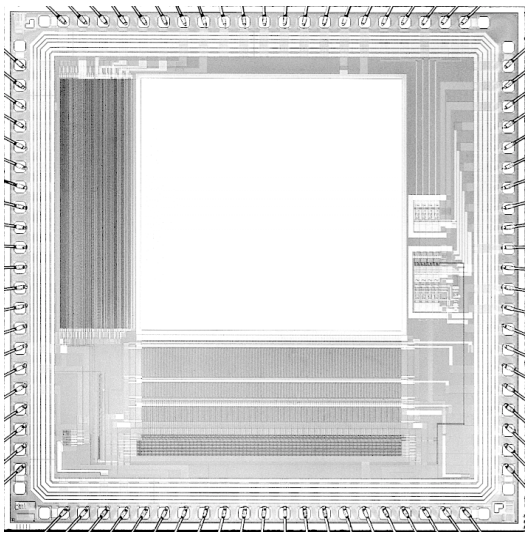

Fig. 3. Chip micrograph of the prototype image sensor.

order to achieve high-precision estimation. A CMOS high-speed non-destructive Intermediate imaging device with bi-directional multiple charge active pixel scheme has been proposed by the authors [1]. It captures high-speed pictures in non-destructive manner and video rate pictures with sufficient signal charge accumulation.

The sensor has two in-pixel analog memories. The signal charge is transferred back and forth between these memories in order to obtain high-speed non-destructive intermediate pictures with reduced fixed pattern noise. Fig. 2 shows the equivalent circuit and the operation principle of the sensor.

The prototype of the image sensor chip based on the proposed active pixel scheme has been designed and fabricated by using 0.35μm CMOS process. Fig. 3 shows the micrograph of the sensor. The sensor captures 480 frame/s high-speed intermediate pictures and 30 frame/s fully accumulated video rate pictures with 3.3V of power supply. The measured pixel-to-pixel fixed pattern noise of the sensor is about 1.2mV. The power dissipation of the sensor is about 17.8mW. Table I shows the specification of the fabricated chip.

Table 1. Features of the chip.

Technology	0.35μm CMOS
Number of pixels	272×260
Pixel size	9×9 μm^2
Fill Factor	16%
FPN (pixel-to-pixel)	1.2mV
Chip size	4.95×4.95mm^2
Frame rate	480 fps intermediate picture 30 fps video rate picture
Power Dissipation	17.8mW

Fig. 4 shows the captured 2nd, 4th, 8th high-speed intermediate pictures and a fully accumulated video rate pictures (16th high-speed intermediate pictures). The gradual increment of the contrast in the pictures demonstrates the successful operation of the sensor.

3. Iterative Block Matching

3.1. Operation Principle

A new motion vector estimation so called iterative block matching, that uses high-speed pictures between two neighboring video-rate

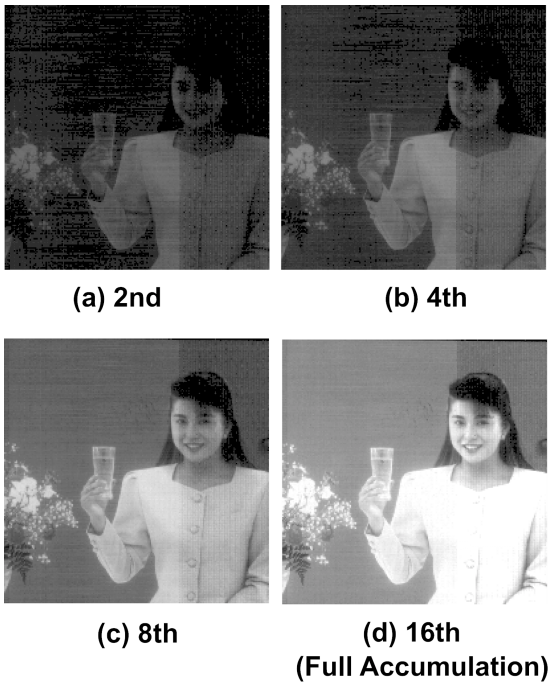

Fig. 4. Captured 2nd, 4th, 8th high-speed intermediate pictures and a fully accumulated video rate pictures (16th high-speed intermediate pictures).

pictures to obtain accurate video-rate motion vector with low computational complexity is proposed [2]. It utilizes the small movement of object between neighboring high-speed pictures to reduce the computational complexity of the block matching.

Fig. 5 shows the operation principle of the iterative block matching. The iterative block matching has two main characteristics. First, it uses a fix reference frame while obtaining motion vector of high-speed intermediate pictures, and

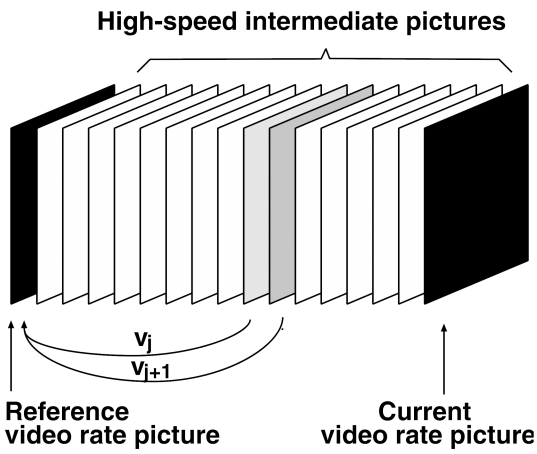

Fig. 5. Operation principle of the iterative block matching.

second it uses previously obtained motion vector of high-speed intermediate pictures as a predictive vector in order to obtain motion vector between current intermediate pictures and the reference picture [2]. Therefore, though the time difference between fix reference frame become larger, the iterative block matching only search for small search range. Iterative block matching by using full search reduce the complexity of full search block matching in video-rate pictures by a factor of 1/10.

3.2. Adaptive Iterative Search

Since pictures are captured non-destructively in a high-frame speed, there is a high-correlation between high-speed intermediate pictures, Therefore, an adaptive search in the iterative block matching is effective to further reduce the computational power of motion vector estimation.

There are many ways of adaptive search in the iterative block matching. The proposed adaptive search is performed as follows:

1. Estimate motion vector between the first high-speed intermediate picture and the reference picture with the search range of ± *p*.
2. For latter high-speed intermediate pictures:
   a. If the corresponding previous small motion vector is bigger than zero, then the search range is extended to -*p* to 2*p*.
   b. If the corresponding previous small motion vector is less than zero, then current search range is extended to -2*p* to +*p*.
   c. If the previous motion vector is 0, the

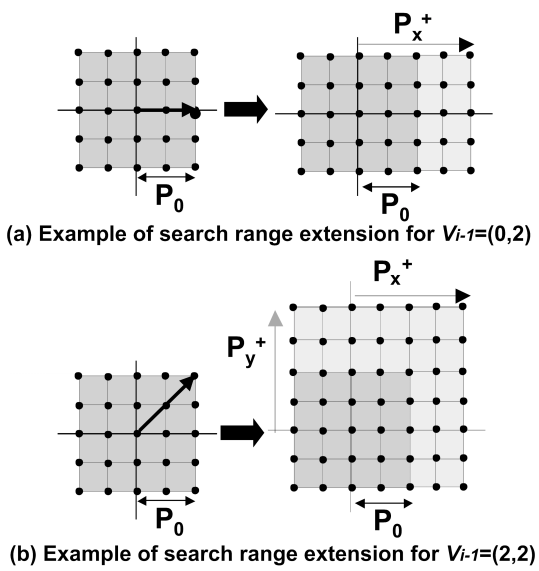

Fig. 6. Example of search range extension in the adaptive iterative search.

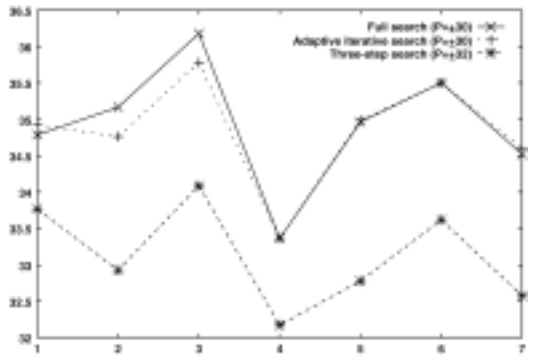

Fig. 7. Moving picture compression simulation results of the three search methods.

search range remains unchanged.

These adaptive rules are applied to both horizontal and vertical search range. By this way, the search range can be extended to the direction of the object movement. Therefore, inefficient search in the full search is eliminated. The search range can be extended without a significant increase in the computational complexity. Examples of the search range extension in the adaptive search are illustrated in Fig. 6.

Simulation results of moving picture compression using three search methods are shown in Fig. 7. In this simulation, 120 frame/s high-speed pictures captured by using conventional high-speed CCD camera are used. The 15 frame/s video pictures are generated by averaging eight high-speed pictures, intermediate pictures are generated by averaging *k* (*k*=1,…,7) high-speed pictures.

The comparison of computational complexity is shown in Table 2. Full search block matching on video-rate pictures obtain the highest SNR of the pictures, however it has a huge computational complexity. The three-step block matching on video-rate pictures has the lowest computational complexity, however the pictures quality is degraded. On the other hand, the adaptive iterative block matching maintains the picture quality of the full search block matching while it reduces the computational complexity by a factor of about 1/13 in average. Moreover, the adaptive iterative search reduces the high-speed frame-rate requirement of normal iterative block matching to about half, which in turn reduces the power of analog circuits of the sensor.

Table 2. Comparison of computational complexity of various search algorithms.

Search Algorithm	Computational Complexity Ratio	Frame rate (fps)
Full search	**82.7**	**1**
Iterative search	**8.3**	**15**
Adaptive iterative search	**4.4~8.7**	**8**
Three-step search	**1**	**1**

4. Conclusions

A new CMOS image sensor with bi-directional multiple charge transfer active pixel scheme and a focal-plane motion estimation technique so called iterative block matching have been described. The sensor captures high-speed intermediate pictures non-destructively for the use in the iterative block matching with FPN reduction. Also it captures video-rate pictures with sufficient signal accumulation. The image sensor chip has been fabricated by using a standard CMOS 0.35μm process. The experimental results confirm the proper operation of the sensor.

The iterative block matching estimate motion vector of video-rate pictures by utilizing the advantage of high-speed pictures with reduced computational complexity compared to full search block matching. The adaptive search of the iterative block matching further reduce the computational complexity by a factor of 1/13 in average, while maintaining the estimation precision. Furthermore, it reduces the high-speed frame rate requirement of the iterative block matching to about half.

The practical implementation and the performance demonstration of the proposed method are left as a future subject.

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