A mega-pixel high speed CMOS imager with sustainable Gigapixel/sec readout rate

By: Stefan Lauxtermann[1*], Georg Israel[1], Peter Seitz[1], Hans Bloss[2]
Jürgen Ernst[2], Heidrun Firla[2], Stephan Gick[2]

[1]CSEM, Badenerstrasse 569, CH-8048 Zürich, Switzerland
stefan.lauxtermann@philips.com

[2]Fraunhofer IIS, Am Weichselgarten 3, D-91058 Erlangen, Germany

Abstract

A high-speed active pixel (APS) imager with a physical resolution of 1024x768 pixels is presented which acquires up to 1000 frames/sec. The imager has a physical resolution of 1024x768 pixels and acquires up to 1000 frames/sec. The light sensitive photodiodes in the array are arranged in a chessboard like pattern and are color masked with an RGB Bayer pattern. Interpolation then leads to a resolution of 1536x1024 pixels. Analog data are transmitted off-chip through 32 output channels that operate at over 30 MHz each. For electronic exposure control the sensor can be operated with a rolling line as well as a global shutter. Also, the photo response is programmable to have a linear, logarithmic or combined lin-log characteristic. For processing a standard 0.5µm CMOS technology was chosen. The chip has physical dimensions of 14 x 20 mm^2 and dissipates 600 mW at full resolution and maximum speed. The sensor resolution can be reduced without having to modify the analog output rate, as long as only center symmetric sub-arrays are considered. Therefore the frame rate is proportional to the inverse of the imager resolution.

I. Introduction

The development of electronic high-speed imagers has become an important topic for many groups and companies that are currently active in the field of active pixel photo sensing. State of the art CMOS sensors today achieve (frame rate) x (resolution) products that are at least 4 times the one of their CCD counterparts [1,2,3,4]. This improvement is directly related to the active pixel sensor architecture, which offers the designer more freedom to optimize a projected sensor for a particular application, e.g. high-speed imaging. In particular, the memory-like APS architecture makes the implementation of highly parallel readout structures comparatively simple. In contrast, the CCD principle is based on a serial readout structure. Although special CCDs with several readout taps are commercially available, their operation requires a considerable amount of power to drive the electrodes and a substantial signal generation and processing effort, e.g. for matching the response from different outputs. As a consequence such camera systems are rather expensive, which limits the range of applications.

Compared to a standard video camera, three main requirements can be identified on the sensor side for a high-speed video system: increased light sensitivity, maximum data throughput and the availability of an efficient global electronic shutter. As our sensor was to be integrated in standard 0.5 µm CMOS technology without process modifications, for maximum sensitivity a rather large pixel with a size of 11x22 μm^2 and a fill factor of 45% was chosen. The photodiode is based on an n-well in p-substrate implantation, which has the best quantum efficiency of all available photo sensing devices in this technology.

For maximum data throughput, the data stream characteristics of an image capture device for video application is reflected in our sensor architecture. This means: 1. Highly parallel readout structures based on an analog bus with 32 channels. 2. Implementation of on-chip sample and hold stages to reduce slew rate requirements of the 1st and 2nd APS stage. While the first aspect is also reflected in the architecture for digital memories, the second feature is only possible for imagers, where address patterns are extremely repetitive and no real time data processing is required in the case of video image capture.

Regarding the global shutter, in a previous design [5] only unsatisfactory functionality could be observed because parasitic photo-charge carriers diffuse through the substrate to the light shielded storage node. Therefore a new pixel was developed for this sensor. In this pixel the storage node is protected against light with a metal shield and against parasitic charge

* now with Philips Semiconductors, Binzstrasse 44, CH-8045 Zürich, Switzerland

integration through the substrate with a guard implantation. This was achieved by placing the p^+ storage node in an n-well implantation, i.e. the storage node is a p+ in n-well implantation

II. Sensor Architecture

The APS has three amplification stages as shown in figure 1. Inside the pixel an APS typical source follower provides an impedance conversion of the photo-generated signal. For each column there is a unity gain buffer, optimized for low power consumption, low noise, medium speed and good linearity. The output of this amplifier is switched onto the horizontal analog bus by a column select signal. In order to minimize overall power consumption, the column select signal also controls the connection to VDD for this stage. The output stage is working continuously and provides sufficient drive strength to connect off-chip ADCs directly to the sensor output pads.

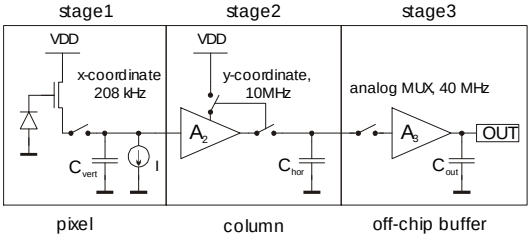

Fig. 1: The APS is based on a 3-stage amplification

The pixel schematic is given in figure 2. In this pixel the shutter and reset transistors are PMOS type, so that the storage node is isolated against the substrate from parasitic charge integration by the surrounding n-well.

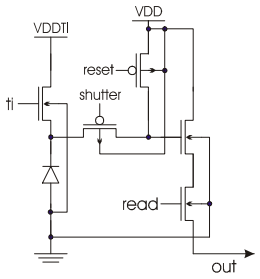

Fig. 2: Pixel schematic with global electronic shutter

Also, these PMOS transistors increase the dynamic range by approximately 7 dB compared to pixels only based on NMOS transistor because (a) the reset node can be reset to VDD and (b) the charge injection from shutter and reset transistor is positive. Note, however, that the storage node, a p^+-n-well diode, has a comparatively high leakage current which limits the maximum storage time to approximately 4 msec. For long storage times this leakage current is also a significant noise source. Most important, it is possible with this pixel to already accumulate light for the next frame while still reading out the present frame.

In order to reduce the slew rate requirements on the first and second APS stage, a pre-charge architecture was implemented. In figure 3 a simplified view of the integrated address logic is given for the first stage. A signal coming from a pixel in the left sensor half is loaded onto C_{vert} (capacitance of the vertical output line inside the pixel array) half a row cycle before it is transmitted by the second stage. During this time, the pixel values from the right sensor half of the previous row, that were already pre-charged before, are read by stage 2. These cycles of pre-charging and reading out alternate between the left and right sensor half. In that way, the readout is fully continuous and no time interrupts have to be inserted between rows. Only at the end of a frame, a short interrupt is required to globally reset the storage nodes and photodiodes in all pixels and sample the photo-generated electrons onto the storage node for the next frame.

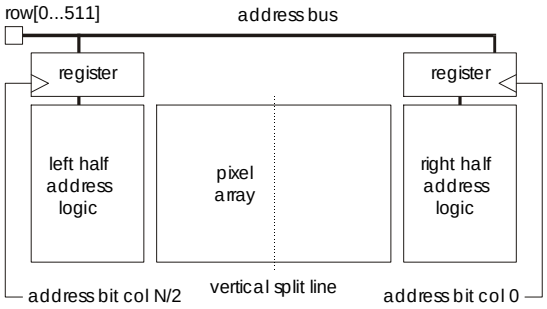

Fig. 3: First stage address logic for pre-charging

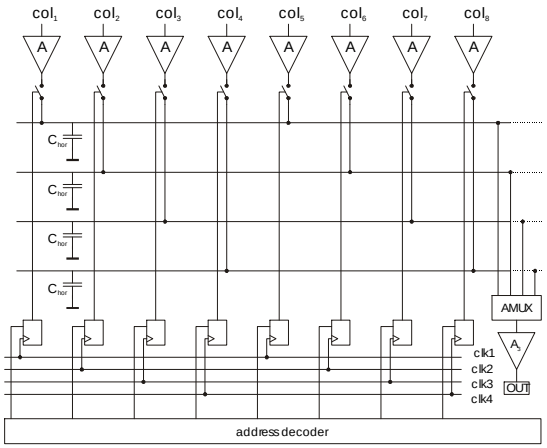

Fig. 4: Simplified address logic for 2nd APS stage

A similar pre-charge concept was implemented for the second stage. There, it is, however, somewhat more complex due to the 32 output channels. A simplified timing diagram, applied to control the first stage is given in figure 5.
For a chess pattern like photodiode distribution

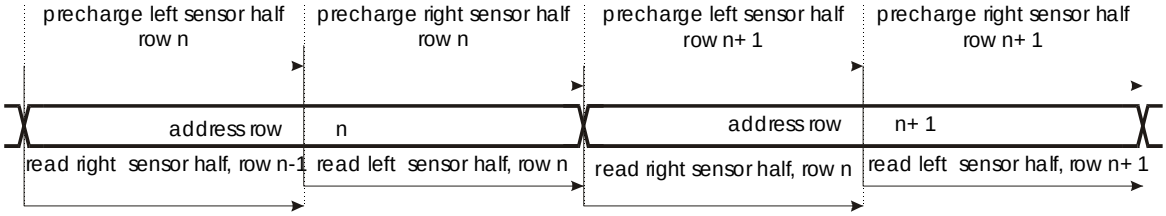

Fig. 5: Simplified timing diagram to illustrate the pre-charge concept for the 1st stage of the APS

the advantage that the pixel rate can be kept constant even when the resolution in the horizontal dimension is reduced to 1/4. For example a sub-array with a non-interpolated resolution of 256x256, i.e. 128 row addresses and 512 column addresses achieves a maximum frame rate of 12,000 pictures/sec.
Figure 6 also shows the RGB pattern that was used for the sensor.

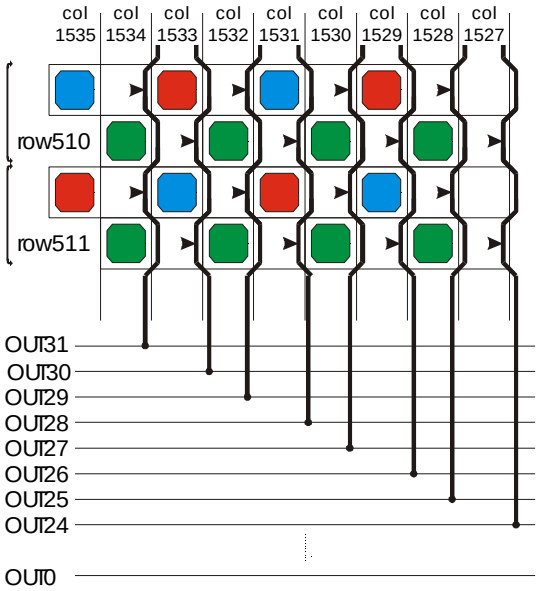

Fig. 6: Simplified representation of bottom left corner of pixel array. The array is read out to the right and upwards. The address field is 512 rows by 1536 columns as indicated, which is equivalent to 1024x768 pixel resolution.

III. Results

The sensor was tested and characterized inside a prototype high-speed camera. Further information about the high-speed camera system behind this APS imager can be found in reference [6]. An overview of the sensor characteristics and camera performance is summarized in the following table.

Feature	value
resolution	768 x 1024
interpolated resolution	1536 x 1024
chip size	20 x 14 mm^2
analog outputs	32
power dissipation	600 mW
pixel size	11 x 22 μm^2
geometrical fill factor	45%
power supply	3.3 V
response	linear, logarithmic
Max. pixel rate	>1Bpixel/sec
max. frame rate	1000 fr/sec

A sample picture, recorded at the full resolution and the maximum frame rate of 1000 pictures/sec is given in figure 7. For this picture extensive post-processing was applied, i.e. gain and offset correction, demosaic filtering and inter-pixel interpolation. This leads to a resolution of 1024x1536 pixels.

Summary

A high-speed active pixel sensor in standard CMOS technology was presented that supports a sustainable pixel rate of 1 Gpixel/sec. Excellent global shutter function could be demonstrated for the required storage time of up to 1 msec. In future developments we will focus on increasing the sensor sensitivity and resolution by transferring the design to more aggressive CMOS technologies. Also the integration of digitizers and programmable on-chip control logic is expected to improve the overall camera characteristics in terms of power consumption, ease of use and minimum overhead of external electronic components.

Fig. 7: Sample picture taken at a frame rate of 1000 pictures/sec. (This pictures was compressed to reduce the file size of this document. For a full resolution sample see reference [6])

References:

1. P. Levine, D. Sauer, F. Hseuh, F. Shallcross, G. Taylor, G. Meray, J. Tower, L. Harrison, W. Lawler, ”Multiport backside-illuminated CCD imagers for high-frame-rate camera applications”, *Proc. SPIE*, Vol 2172, pp.100-114

2. http://www.fillfactory.com/htm/news/news.htm#hispeed, 1024x1024 sensor with one gigapixel per second

3. http://www.photobit.com/Products/Megapixel_Sensors/megapixel_sensors.htm, Megapixel CMOS image sensor with 500 frames/sec

4. G. Allen, D. Dattani, D. Dykaar. E. Foc, G. Ingram, S. Kamasz, M. J. Kijk, B. Li, A. Pavlov, Q. Tang, “High-Speed VGA CMOS Image Sensor”, IS &T/SPIE’s Electronic Image Sensing 2001, 20-26 January 2001, San Jose, CA (USA)

5. S. Lauxtermann, P. Schwider, P. Seitz, H. Bloss, J. Ernst, H. Firla, “A high speed CMOS imager acquiring 5000 frames/sec“, Tech. Digest IEDM, pp. 875-878, Washington, DC (1999)

6. http://www.weinberger.ch, SpeedCam Visario