CMOS Image Sensor with CIF/QCIF Switching Function

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1.Introduction

Most of commercial CMOS camera modules consist of two chips, a CMOS image sensor and an image processing chip [1]. This configuration is suitable to attain high image quality because each chip can be indepedently optimized. On the other hand, a single chip camera [2] is also attractive in the field where the size and/or power consumption are critical. In this case, high image resolution is not always necessary. We present a novel CMOS image sensor that is effectively applicable to both camera configurations. A CIF/QCIF switching function is introduced in pixel addressing.

□□Chip Architecture

Figure 1 shows the block diagram of the sensor chip. The pixel array has 352x288 pixels with RGB Bayer color filter pattern. Figure 2 (a) indicates a conventional pixel addressing method which provides 352 x 288 raw format data, namely CIF addressing method. To get RGB data, color interpolation processing is necessary. Figure 2(b) is an original method where 2 by 2 sensor pixels are regarded as a single pixel of the reproduced image and sensor pixels are addressed in zigzag way. With averaging two green data, 176x144 RGB format image is obtained. This QCIF addressing method is achieved due to flexible pixel accessibility of CMOS sensor [3], [4]. To implement both addressing methods in one chip, the horizontal scanner consists of a 176-stage shift register and 352 AND gates. The shift register selects a pair of adjacent lines out of 176 pairs and two AND gates select either line of a pair utilizing a global even/odd signal. The configuration of the vertical one is the same.

As analog peripheral circuits, CDS, gain amplifier, white balance and gamma correction circuits are integrated. Compared with the case where CDS circuit is employed in each column, a single CDS circuit scheme has an advantage not to form stripe FPN essentially[5].

According to the CIF/QCIF switching function, our chip enables the implementation of two kinds of camera modules. When the QCIF addressing method is used, all the elemental color processing is executed by sensor chip. By executing the adjustment of gain and white balance coefficient with system controller to which the camera is applied, a single chip

camera module with relatively low resolution, QCIF resolution can be realized (Fig.3(a)). On the other hand, the combination of the sensor chip operated with the CIF addressing method and color image processing chip with color interpolation function, enables a camera module with higher resolution, CIF resolution (Fig.3(b)).

Experimental results

The sensor chip was fabricated using 0.35um CMOS process technology. The pixel size is 10.0um x 10.0um. The light sensitivity is as high as 1.3V/lxs. The FPN level of green signal with QCIF addressing is lower than that with CIF addressing as shown in Table 1. This is due to green averaging. Since human eye is sensitive to green component, this FPN suppression is effective. The power consumption is as low as 25mW at the driving voltage of 3.0V.

Figure 4 shows the captured image with CIF/QCIF addressing method. In the CIF method, color interpolation was executed by software. It is confirmed that a unique accessing in the QCIF method does not degrade image quality.

We are also developing a compact camera module. As shown in Fig.5, our CMOS sensor is mounted in the lens-equipped package. The size is as small as 0.7cm^3.

Reference

[1] J. Hurwitz et al., "A Miniature Imaging Module For Mobile Applications," ISSCC Digest of Technical Papers, pp.90-91, February 2001.

[2] S.G.Smith et al., "A single-Chip CMOS 306x244-Pixel NTSC Video Camera and a Descendant Coprocessor Device," IEEE J. Solid-State Circuits, vol.33, pp.2104-2111, December 1998.

[3]E.R.Fossum, "CMOS Image Sensors: Electronic Camera-On-A-Chip," IEEE Trans. Electron Devices, vol.44, pp.1689-1698, October 1997.

[4]E.Funatsu, Y.Nitta, Y.Miyake, T.Toyoda, J.Ohta, and K.Kyuma, "An Artificial retina Chip with Current-Mode Focal Plane Image Processing Function," IEEE Trans. Electron Devices, vol.44, pp.1777-1782, October 1997.

[5]K.Yonemoto, H.Sumi, R.Suzuki, and T.Ueno, "A CMOS Image Sensor with a Simple FPN-Reduction Technology and a Hole Accumulated Diode," ISSCC Digest of Technical Papers, pp.102-103, February 2000.

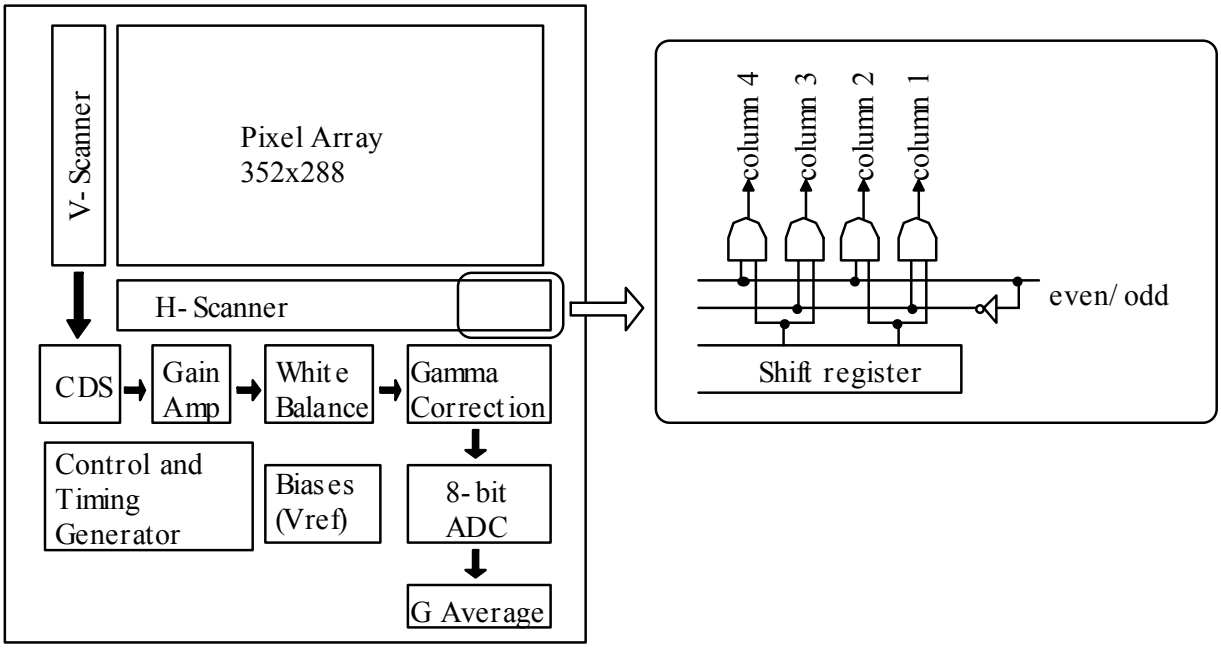


Fig.1 Block Diagram

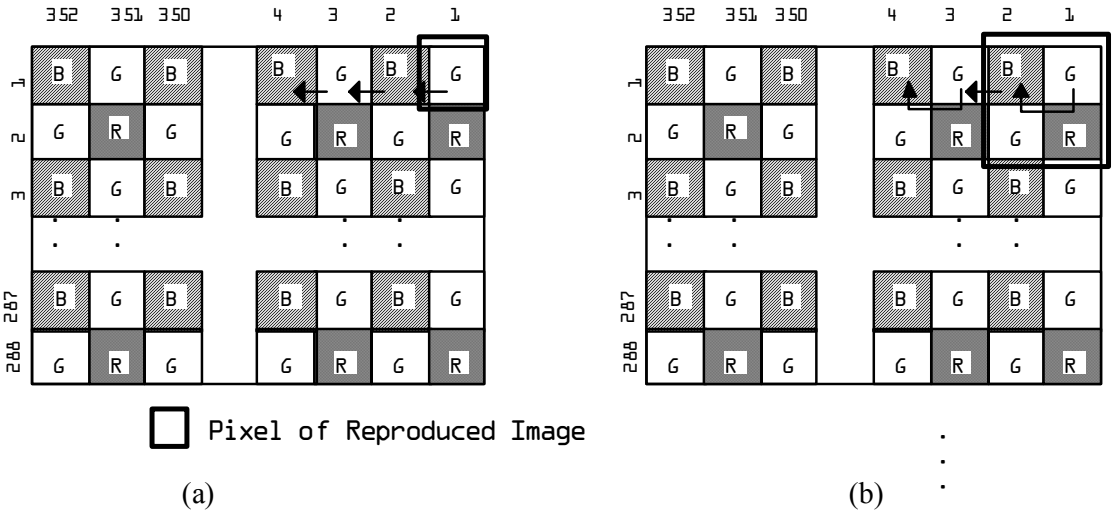


Fig.2 Color filter pattern and pixel addressing method
(a) CIF addressing method (b)QCIF addressing method

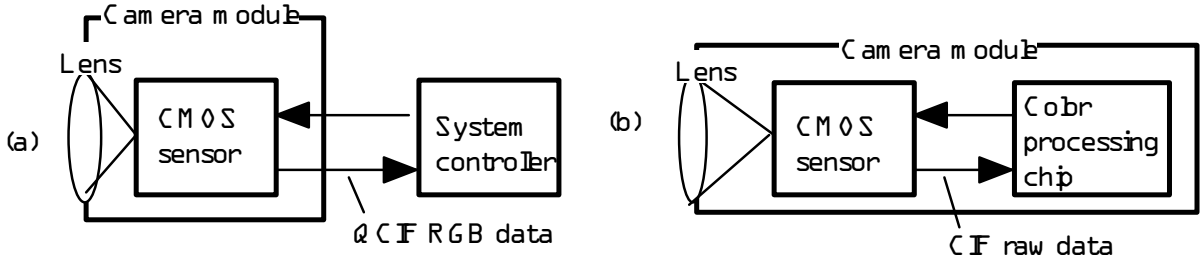
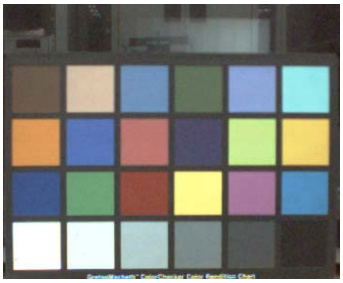


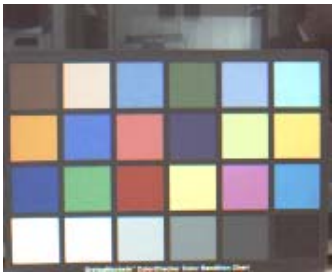
Fig.3 CMOS camera module configuration
(a) Single chip configuration with QCIF resolution
(b)Two chip configuration with CIF resolution

Table 1 Charcteristics

Pixel Size	10.0um(H)x10.0um(V)
Number of Pixels	352(H)x288(V)
Process	0.35um CMOS, 1 poly 3 metal
Chip Size	6.3mm x 5.65mm
Sensitivity	1300mV/ lx s
FPN (dark)	2.4mV(CIF,green)
	2.0mV(QCIF,green)
Frame Rate	15fps
Power Supply	3.0V
Power Consumption	25mW



(a)



(b)

Fig.4 Captured images
(a) CIF addressing method (b)QCIF addressing method

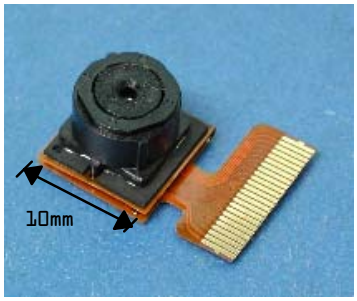


Fig.5 Photograph of a camera module