

A High-Sensitivity Oversampling Digital Signal Detection Technique for CMOS Image Sensors Using Non-destructive Intermediate High-Speed Readout Mode

Shoji Kawahito*, Nobuhiro Kawai** and Yoshiaki Tadokoro**

*Research Institute of Electronics, Shizuoka University
3-5-1 Johoku, Hamamatsu 432-8011, Japan

TEL:+81-53-478-1313, FAX:+81-53-412-5481, E-mail:kawahito@idl.rie.shizuoka.ac.jp

** Toyohashi University of Technology,

Abstract

This paper discusses the possibility of a high-sensitivity digital signal detection technique using frame oversampling and a CMOS image sensor with non-destructive high-speed intermediate high-speed readout mode. Simulation results show that the frame oversampling is very effective to reduce output amplifier noise and quantization noise of ADC.

I. Introduction

CMOS image sensors are expected not only for the low-power smart image imaging devices but also for the high-sensitivity imaging devices. In the pixel, a buried photo diode enables its random noise to be comparable to that of the CCD [1][2]. The merit of the CMOS image sensor over the CCD on the amplifier noise is discussed by Matsunaga et al [3]. Another possibility of the high-sensitivity imaging in the CMOS is the use of signal processing technique. A few techniques using oversampling ADC for CMOS image sensors have been proposed such as pixel-level A/D conversion [4], and column parallel A/D conversion using delta-sigma modulation [5].

This paper discusses the possibility of another type of a oversampling signal processing technique for ultra-low light level CMOS image sensors, that is frame oversampling signal processing [6]. This technique allows us to use high-gain column parallel amplifier array and to reduce the noise of the output amplifier broadband noise and the quantization noise of the ADC. The necessary imaging device for this signal processing is a CMOS image sensor that the signal can be read out during the signal charge accumulation without destructing

it. A simple three transistor APS as well as an APS specially designed for non-destructive readout [7] can be used for this purpose.

In the following, architecture, principle and simulation results of the frame oversampling signal processing using non-destructive intermediate imaging are described.

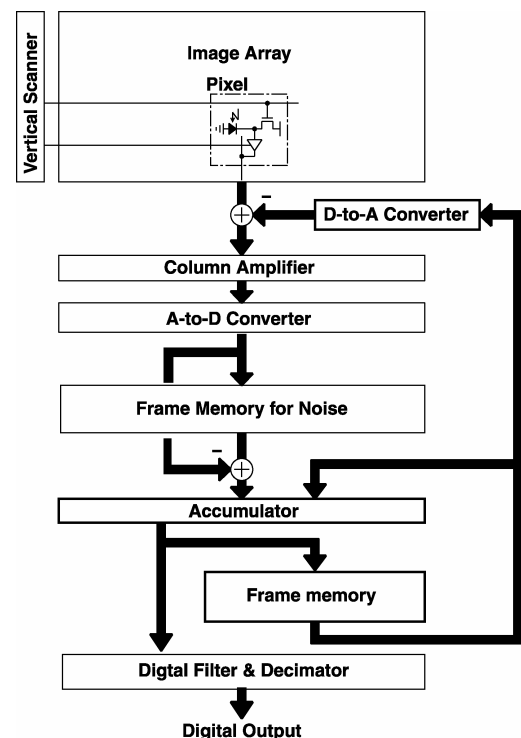


Fig. 1 Architecture of the frame oversampling imaging system.

II. Architecture and Principle

Fig. 1 shows the proposed scheme for the digital CMOS image sensor system. The corresponding signal flow diagram is shown in Fig. 2. The important features are 1) each frame is read

out at M times higher rate than the video rate (f_v) without resetting the signal charge, 2) the read sensor signal is amplified by the column amplifier with the gain of M , 3) the digitized signal by the A/D converter is accumulated in the digital integrator, 4) the integrator output is converted to analog signal with the gain of $1/M$, 5) the analog output is subtracted from the read sensor signal in front of the column amplifier, and 6) a digital low-pass filter with frame memory sampled at $M \times f_v$ eliminates the noise component in the frequency range larger than the Nyquist frequency of the video frame and the output is decimated to the video rate.

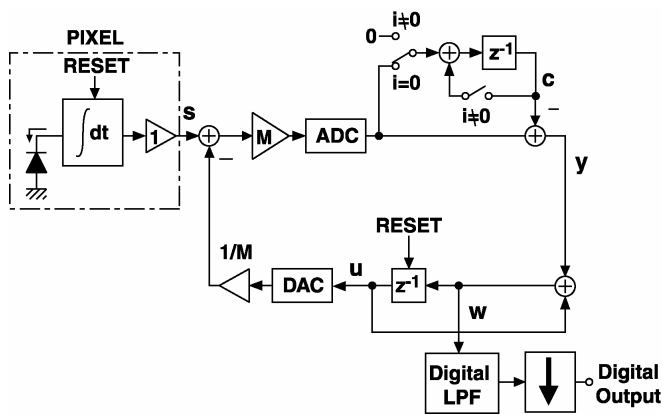


Fig.2 Signal processing diagram of the over-sampling CMOS image sensor system.

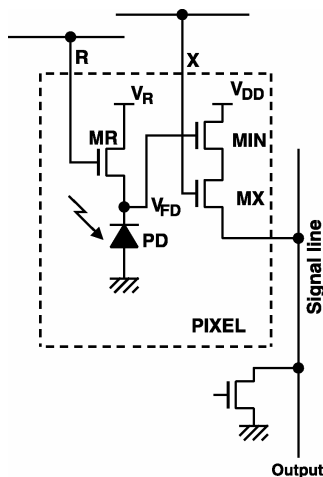


Fig. 3 Three transistor type active pixel circuit.

This scheme acts as a prediction coder in differential pulse code modulation (DPCM). The

most important advantage is that a large-gain column amplifier array can be used so that the noise level of the final amplifier is negligible. Without this prediction, the large gain cannot be used because the amplifier output will saturate for the large input signal. The quantization noise of the A/D converter is also reduced by this scheme. The digital integrator and the digital filter increase the equivalent resolution of A/D converter. If the noise is ideally filtered, the theoretical improvement of SNR for the quantization noise is given by approximately $30 \log_{10} M$ [dB] with the frame-oversampling rate of $M \times f_v$. For instance, in the case of $M=16$ and 10bit ADC, the equivalent resolution is 15bit. We can expect a very-wide linear dynamic range.

The active pixel is either simple 3-transistor type shown in Fig. 3 or in-pixel charge transfer type using buried photo diode. In the case of 3-transistor type, the waveform of the cathode voltage of the photo diode and the readout timing are shown in Fig. 4 in the case of $M=4$. After resetting, the reset level is read out, converted to digital, and memorized. The intermediate signal during photo signal charge accumulation is read out without destructing the signal charge and converted to digital. The reset signal is subtracted from the intermediate signal in digital domain, and the fixed pattern noise (FPN) and kTC noise in the pixel can be cancelled out in digital domain. The column amplifier is useful to make sure the exact canceling of the FPN and kTC noise. For example, in the case of 10bit ADC, the full-scale voltage of 0.8V and the column amplifier gain of 16, the equivalent resolution in noise canceling is $50\mu\text{V}$. The digital low-pass filter further reduces the kTC noise and the pixel source follower noise by a factor of \sqrt{M} .

Another important feature of this scheme is that the noise is not accumulated in the digital integrator because of the noise negative feedback using DAC. The noise stored in the frame memory $v_n(0)$ is given by

$$v_n(0) = M \times v_{np}(0) + v_{nc}(0) + q(0)$$

where $v_{np}(0)$, $v_{nc}(0)$ and $q(0)$ are pixel and column amplifier noise, circuits noise, noise between the column amplifier and the ADC, and the quantization noise of the ADC, respectively, at the sampling

instance of $t=0$. The signal sampling is at the instances of $t = i \times T_0 - \Delta T$ ($i=1,2,\dots,M$), where i is the integer, T_0 is the oversampling frame period, and the ΔT is the time difference of the reset sampling instance from the final signal sampling instance, respectively. In the signal sampling, the following relationship is obtained:

$$y(i) = M \times s(i) + v_n(i) - u(i) - c(i)$$

$$w(i) = u(i) + y(i)$$

$$u(i) = u(i-1) + y(i-1),$$

where $v_n(i)$ is

$$v_n(i) = M \times v_{np}(i) + v_{nc}(i) + q(i)$$

and $y(i)$, $u(i)$, $c(i)$ and $w(i)$ are the signals shown in Fig. 2. The output of the noise memory is given by

$$c(i) = \begin{cases} 0 & (i=0) \\ v_n(0) & (i \neq 0) \end{cases} \cdot$$

From these equations, the final output at the sampling instance of $t = M \times T_0 - \Delta T$ is obtained as

$$w(M) = M \times s(M) + v_n(M) - v_n(0)$$

or

$$w(M) = M \times s(M) + M \times (v_{np}(M) - v_{np}(0)) + v_{nc}(M) - v_{nc}(0) + q(M) - q(0)$$

In the usual digital signal integration, the noise is also accumulated as well as the signal. The M times integration leads to the increase of the noise power by a factor of M . In contrast to such a digital integration, the proposed method allows us to suppress the noise accumulation because the system predicts the in-pixel signal charge integration.

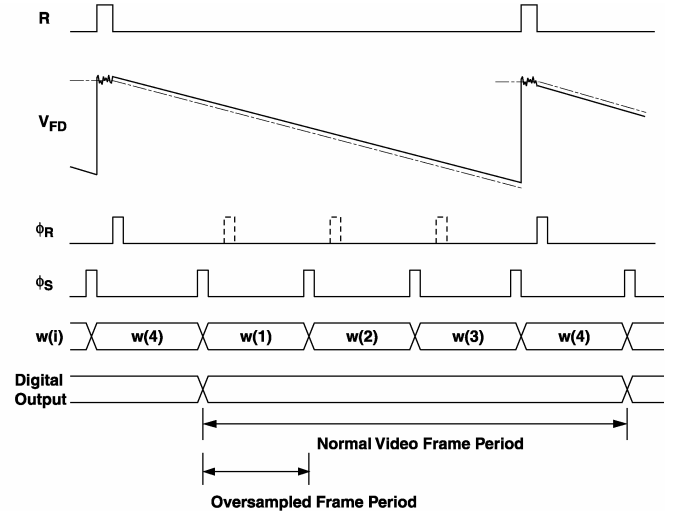


Fig. 4 Timing diagram of the non-destructive

III. Performance prediction with simulation

Figure 5 and 6 show the simulated prediction of the SNR improvement versus oversampling ratio (OSR) for the quantization noise of ADC and the circuits' noise in front of and at the back of ADC, respectively. A CIF(352 x 288) size image sensor with the video rate of 30 frames/s is assumed. In the case that the digital LPF is used, the SNR improvement for the quantization noise at the oversampling ratio of 16 is about 27dB. This means that the equivalent resolution is about 14bit if 10bit ADC is used. In the case of the quantization noise and the circuits' noise at the back of the column amplifier, the 6dB/octave factor of the noise improvement is due the amplifier gain itself. The noise accumulation is successfully suppressed.

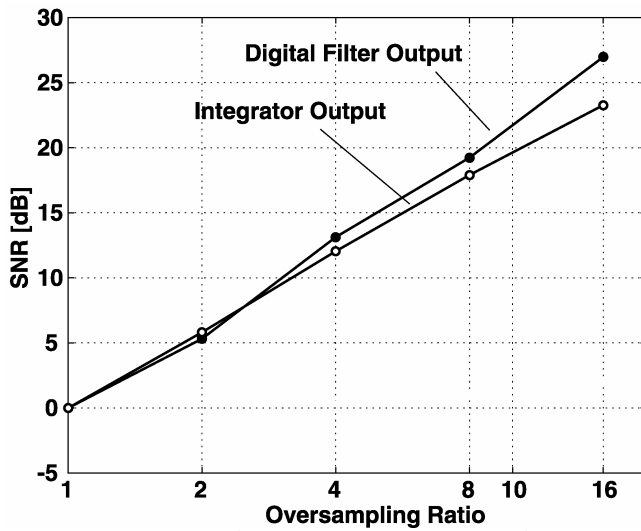


Fig. 5 Reduction of quantization noise of ADC using oversampling processing.

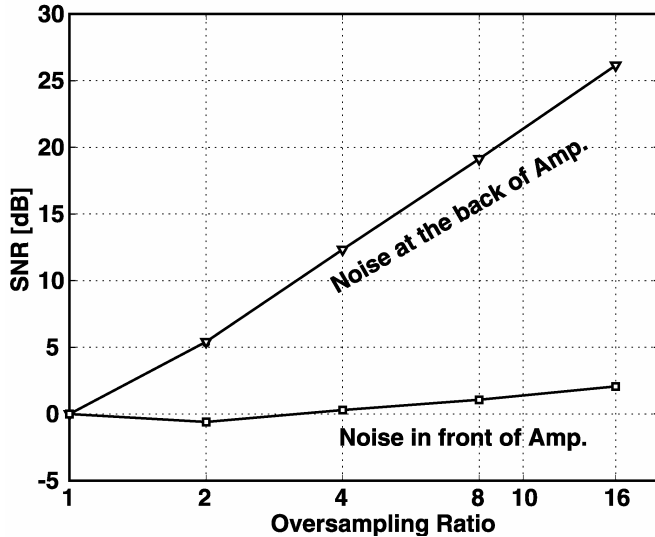


Fig. 6 Reduction of circuit noise in front of and at the back of column amplifier using oversampling.

In the case of the quantization noise, digital filter is effective for the reduction of the noise with the oversampling. In the circuits' noise in front of the column amplifier, the oversampling is not so effective from the simulation results. However, the dominant noise components are the wideband output amplifier noise and the quantization noise of the ADC. Therefore, the oversampling technique is useful for the reduction of the total noise behavior. The low-pass FIR digital filter is not effective for the circuits' random noise. We need another noise reduction technique such as a least

square method.

Table 1 Assumption of the noise performance of a CMOS image sensor.

Item	Value
Conversion gain of the pixel	25 $\mu\text{V}/e^-$
Input referred noise due to circuits in front of column amplifier	2 e^-
Input referred noise due to circuits at the back of column amplifier	10 e^-
Full scale voltage of the 10b ADC	1V
Input referred noise due to the quantization noise of the ADC	10 e^-
Image sensor size	CIF (352x288)
Video frame rate	30 frames/s

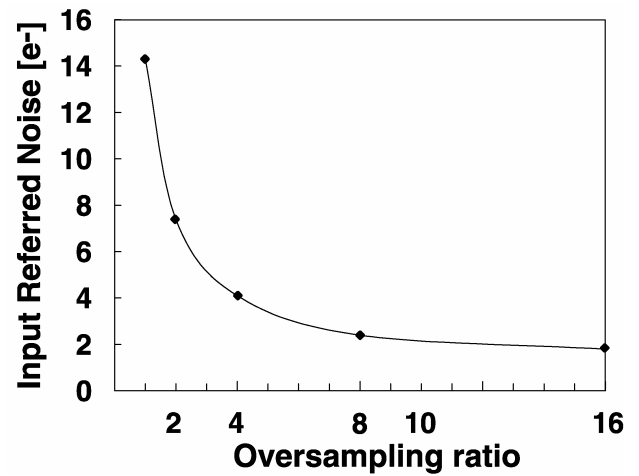


Fig. 7 Total input referred noise as a function of the oversampling ratio.

Using the results of the simulation shown in Fig. 5 and Fig. 6, the improvement of the total input referred noise as the number of electrons is estimated. The assumption of the CMOS image sensor performance is shown in the Table 1.

Figure 7 shows the relationship between the oversampling ratio and the total equivalent noise referred to the input (electrons) under the assumption of the image sensor shown in Table 1. Without the oversampling, the input referred noise is about 14 electrons in this case. At the oversampling ratio of 16, the input referred noise can be reduced to be about 2 electrons.

IV. Conclusions

This paper presents a signal processing technique to reduce the circuits' noise and quantization noise using frame oversampling and a CMOS image sensor in non-destructive readout mode. The random noise level can be reduced the input referred noise of 2 electrons. Another effective noise reduction technique is to use estimation with least square method in the digital filtering section. This is left as the near future subjects.

References

- [1] I.Inoue et al, "Low-dark current pinned photo-diode for CMOS image sensor, " 1999 Workshop on CCD and AIS, pp. 25-28 (1999).
- [2] K. Yonemoto et al, " A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode," Dig. Tech. Papers, ISSCC, pp. 102-103 (2000).
- [3] Y. Matsunaga, Y. Endo, " Noise cancel circuit for CMOS image sensors, " ITE Technical report (in Japanese), IPU'98-2. Vol. 22, No. 3, pp. 7-11 (1998).
- [4] B. Fowler, A.E. Gamal, D. X. Yang, " A CMOS area image sensor with pixel-level A/D conversion," Dig. Tech. Papers, ISSCC, pp. 226-227 (1994).
- [5] J. Nakamura et al., " On focal-plane signal processing for current-mode active pixel sensors," IEEE Trans. Electron Devices, Vol. 44, No. 10, pp. 1747-1758 (1997).
- [6] S. Kawahito et al, " A high-sensitivity digital CMOS image sensor using oversampling signal processing, " ITE Tech. Report (in Japanese), IPU2001, pp. 25-30 (2001).
- [7] D. Handoko, S. Kawahito et. al., "A CMOS image sensor for focal-plane low-power motion vector estimation," Dig. Tech. Papers, Symp. VLSI Circuits, pp. 28-29 (2000.6).