

A 3.25M-pixel APS-C size CMOS Image Sensor

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Abstract

This paper describes a 3.25 M-pixel CMOS Image Sensor developed for a digital SRL (Single Reflex Lens) camera system. The image size of the sensor is 15.1mm (V) by 22.7mm(H), namely APS-C (Advanced Photo System-Classic) size.

I. Introduction

CMOS image sensors have emerged as low-voltage, low-power image pickup devices suitable for mobile applications. Their image quality, however, is still poor compared with that of CCDs due to low signal-to-noise ratio. The reduction of noise is a key issue to broadening the application area of the CMOS sensors.

A new noise cancellation scheme has been developed along with low leakage photodiode for the CMOS image sensor. The sensor chip is integrated with GCAs (Gain Control Amplifiers) and offset cancellation circuits. Maintaining low power dissipation feature, the sensor realizes signal-to-noise ratio and dynamic range comparable to those of CCDs.

II. Sensor chip configuration and operation

The circuit block diagram of the developed sensor chip is shown in Fig.1. The image area is 15.1mm x 27.1mm by size and consists of a 1440(v) x 2160(H) pixel array. The pixel is 10.5 μ m by 10.5 μ m and consists of a photodiode and four transistors. The aperture ratio of the pixel is 37%. On-chip micro-lenses along with Bayer-arranged color filters are designed and fabricated to meet both the sensitivity and

optical requirements. The pixel signals are scanned and readout into two terminals via noise cancellation circuits described later. Each channel signal is amplified with selected gain and the offset voltage between the terminals is cancelled before signal multiplex.

A 0.35 μ m 1poly-3metal CMOS technology optimized with additional photodiode fabrication process has been developed and employed for the fabrication.

A pixel and a corresponding column noise cancellation circuit diagram are shown in Fig.2 [1][2]. The pixel consists of a buried-type photodiode for photoelectric conversion, a reset MOS for resetting the FD (floating diffusion) node, a SF (source-follower) MOS for charge-voltage conversion, a select MOS for row selection and a transfer MOS for perfect charge transfer [3] of the photo-generated carrier to FD node.

A signal readout timing chart is shown in Fig.3 to describe the noise cancellation scheme. The sequence of the readout is as follows:

(1) *Photodiode reset, FD reset and Photo signal charge accumulation*

Switch ON reset MOS and transfer MOS, then, switch OFF transfer MOS to start photo signal charge accumulation.

(2) *Noise readout and store*

Switch ON select MOS and noise readout MOS \square N (Fig.2) to amplify and store noise held in FD node into CTN.

(3) *Photo signal charge transfer*

Switch ON transfer MOS to transfer accumulated photo signal from photodiode to

the FD node.

(4) *Signal readout and store*

Switch OFF transfer MOS and switch ON signal readout MOS \square s to amplify and store signal plus noise into CTS.

(5) *Differential readout*

Switch ON \square H to subtract voltages stored in CTN from CTS.

The noise stored in CTN consists mainly of the reset thermal noise and the fixed pattern noise of the pixel. The reset noise is a random noise that inevitably appears during the previous reset operation. The fixed pattern noise is mainly due to the variance among the threshold voltages of SF MOS transistors. The point here is that the noise component in the photo signal is retained between noise readout and signal readout so that both random noise and fixed pattern noise are successfully cancelled. This operation is realized thanks to the existence of transfer MOS.

III. Sensor characteristics

The photo-electric conversion characteristics diagram is shown in Fig.4 and the sensor specification and characteristics is shown in Table. 1.

The sensitivity is 1.4V/lxsec with green color filter. The saturation voltage is 1.3V and is determined by the dynamic range of the output differential amplifier. The random noise is 0.27mVrms and fixed pattern noise is 0.8mVpp. The dynamic range for the random noise is 74dB. The dark current density is 60pA/cm² at 60 \square C.

The power consumption is measured 250mW at 5V bias voltage and 12MHz signal readout rate. The value is estimated to be about 1/5 that of CCDs with same size and number of pixels.

The sensor has been successfully applied to digital SRL camera system.

The photograph of the packaged sensor is shown in Fig.5 and a sample image taken by the applied camera system is shown in Fig.6. The low noise and the low dark current performance of the sensor are the key factors for excellent image quality realized by the system. The low power consumption capability, particularly low peak current of the CMOS image sensor has enable the system to operate with relatively 'small and light' lithium-ion battery as opposed to conventional 'large and heavy' Ni-H batteries.

Conclusion

A new noise cancellation scheme has been developed and successfully applied the 3.25M-pixel CMOS image sensor.

This sensor has developed a new high image quality and 'large-image-size' application area for CMOS, which area has conventionally been dominated by CCDs.

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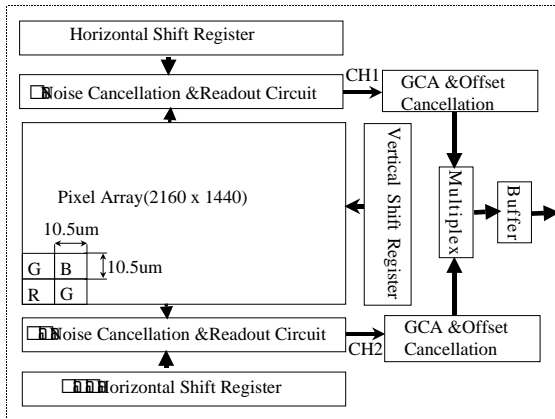


Fig.1 Sensor circuit block diagram

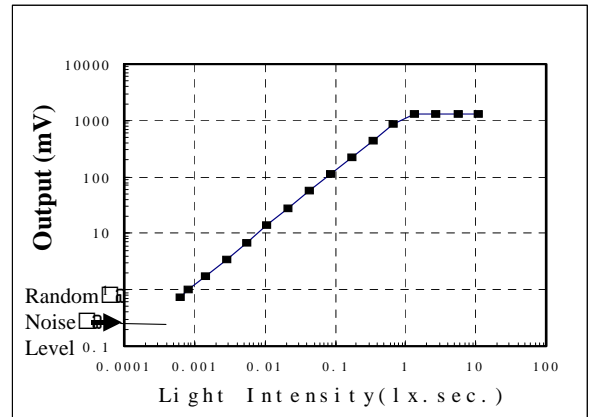


Fig.4 Photo-electric conversion characteristics

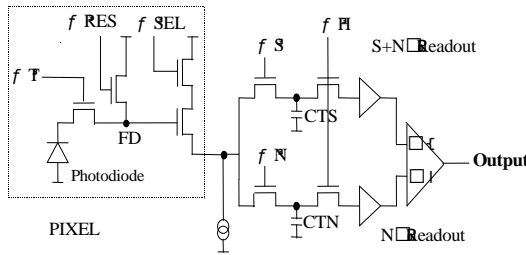


Fig.2 Pixel and noise cancellation circuit diagram

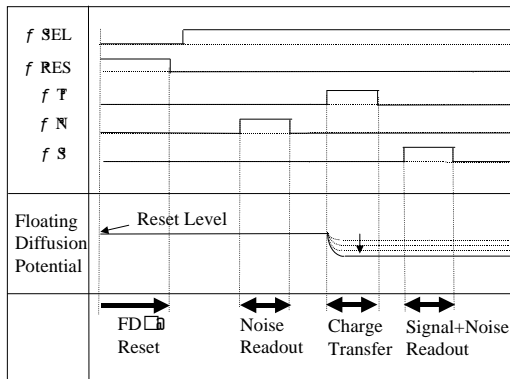


Fig.3 Readout timing chart

Total number of pixels	1460(V) x 2226(H) (3.25Mpix.)
Number of pixels in image area	1440(V) x 2160(H) (3.11Mpix.)
Chip Size	18.1mm x 24.9mm
Image Area Size	15.1mm x 22.7mm (APS-C size)
Pixel Size	10.5µm x 10.5µm
Aperture Ratio	37%
Saturation Voltage	1.3 V
Power Supply	5V
Power Consumption	250mW
Technology	0.35µm CMOS (1Poly / 3Metal) with photodiode formation
Color Filter	RGB Bayer with lenses
Package	DIP Ceramic
Signal Readout Rate	12MHz
GCA	X1, X2, X4
Sensitivity	1.4 V/lx \cdot s
Dark Current Density	60 pA/cm ² (@60 °C)
Random Noise	0.27 mVrms
Fixed Pattern Noise	0.8 mVpp

Table.1 Sensor specification and characteristics chart

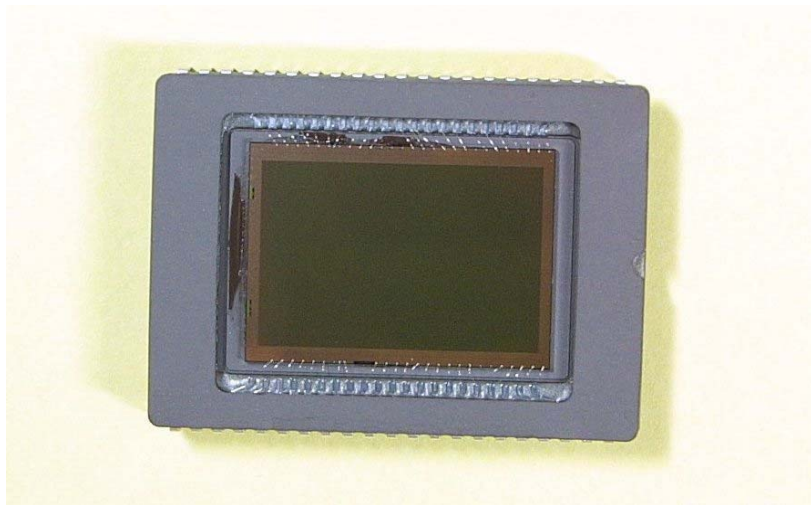


Fig.5 Packaged sensor chip photograph



Fig.6 Image sample captured with the camera