

R 39: A 1/4-inch 630K-pixel IT-CCD Image Sensor with High-Speed Capture Capability

Masao Kimura, Hiroyuki Yoshida, Isao Hirota, Atsuhiko Yamamoto, Kazuomi Ezoe,
 Yuuichi Okazaki, Youji Takamura, Hiroyuki Mori*, Yukio Fujita*
 CCD System Division, Semiconductor Company, Core Technology & Network Company,
 Sony Corporation, Kanagawa, JAPAN

*SONY Kokubu Corporation, Kagoshima, JAPAN

Address: Sony Corporation, Core Technology & Network Company,
 Atsugi Tec., 4-14-1, Asahi-cho Atsugi-shi, Kanagawa, 243-0014 Japan

Phone: +81-462-30-5449, FAX: +81-462-30-6170

E-mail (for Masao Kimura): kimura@saccd.semicon.sony.co.jp

Abstract

We have newly developed a 1/4-inch 630K interline transfer CCD (IT-CCD) image sensor with a new CCD structure and driving methods which realize advanced "High-Speed Capturing". Dynamic resolution can be higher than that captured by the normal method and, in the best case, nine times the fields-read-out rate can be obtained than with it. In addition to this feature, we can also obtain such characteristics as high sensitivity, low smear, and large saturation voltage.

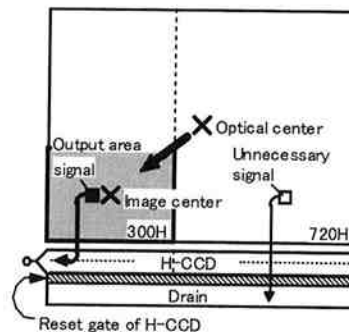
1. Introduction

An interline transfer CCD (IT-CCD) image sensor for DV-C with 1/4-inch optical area and 630K effective pixels, provides high quality images for diverse applications. The main features of this CCD are a new CCD structure and driving methods that realize advanced "High-Speed Capturing".

With high-speed capturing, it is possible to capture images up to 540 fields/s at the center of the optical area. A high-speed camera realized by only a CCD image sensor is the most reasonable for cost, miniaturizing of cameras, and the like. The function, which is similar to our "High-Speed Capturing", is realized by CCD structure previously described [1, 2].

However, as shown in the top of Figure 1, it is achieved by resetting the signals in horizontal register, so the output image is limited only to the corner of the effective area. Therefore, the center of the image is not the same as the optical center. For example, zooming is incompatible with this method.

【Conventional structure】



【New structure】

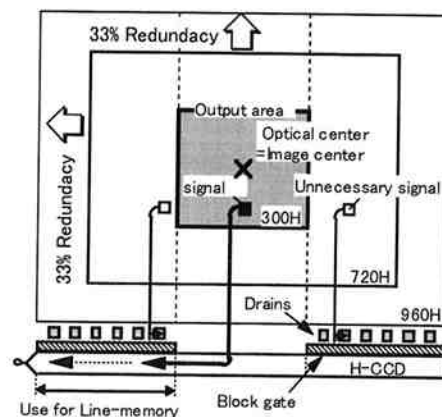


Figure 1: High-Speed capturing comparison.

2. Device Structure

To make the center of the image coincide with the optical center, as shown in Figure 2 and the bottom of Figure 1, the last gate area of vertical registers is divided into three horizontal segments with the almost same size. In the left and right part (each has 331 packets = about 1/3 of 962 all effective packets), there is the "block gate". The block gate can form a barrier sufficient to block the signals from the vertical register to the horizontal register at any period. The "drains" are arranged in front of the block gate in order to empty the signal charge. As shown in Figure 3, beside every drain there is an overflow barrier connected with the vertical registers. The drains are always biased sufficiently to discharge the blocked signals.

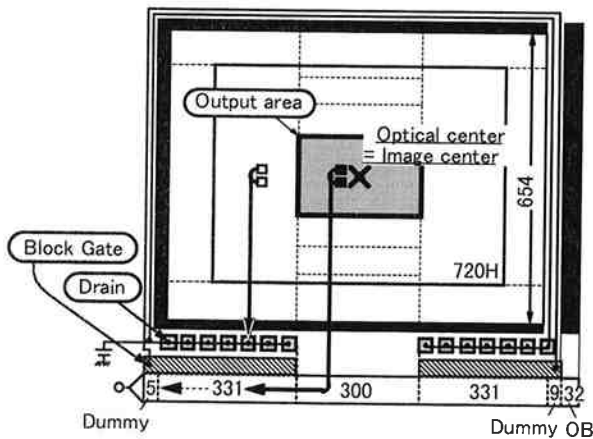


Figure 2: Schematic diagram.

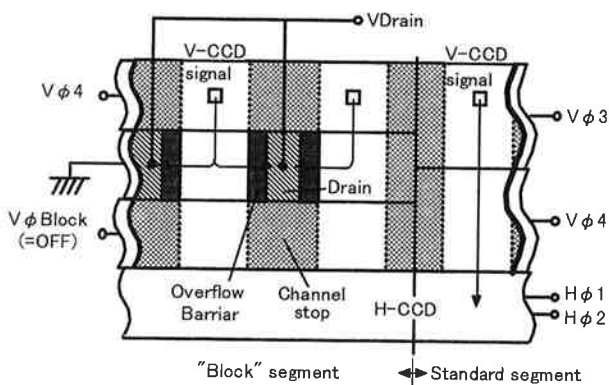


Figure 3: Block gate and drains structure.

When the block gate is low-level and the barrier beneath the block gate is formed, the blocked signals overflow through the barrier and reach the next drains. Thus, unnecessary signals are reset to the clamp bias. In the case that the block gate is high-level and there is no barrier beneath the block gate, the signals from the vertical registers are transferred to the horizontal register. The center area of horizontal direction (300 packets) has a standard structure without "block gate" and "drains". The optical black part used for clamping the black level also has the standard structure.

3. High-Speed Capturing

The principle of motion and the clock timing for the high-speed capturing are shown in Figures 4 and 5. During the vertical CCD transfer, when the VBLOCK clock level is "OFF", only the 300 signal charge packets of the center part are transferred to the horizontal register (as shown in <3-1> of Figs. 4 and 5). After that, the horizontal CCD transfer is completed only 1/3H (336 times) (<3-2>), and then the next vertical transfer is completed (<4-1>). The horizontal register corresponding to the block gate can be used as a line memory. Therefore, by repeating this process, there are three times more fields per second than with normal drive. These images are based on the center of the optical area. Since this driving method has H-blanking in every 1/3H, it is called the extra H-blanking as "virtual H-blanking".

On the other hand, regardless of the block gate level, black level signals are transferred from the vertical registers in the optical black part (32 packets) to the horizontal register (<3-1>). After the 1/3H (336 bits) horizontal CCD transfer, these black level signals stay in the horizontal register corresponding to the block gate and just after the central 300 packets (<3-2>). The next vertical transfer synthesizes the signals for image and black level. By the next horizontal transfer (336 bit) (<4-2>), these synthesized signals are just in front of the central 300 packets forming one set. Thus, these signals are not broken even when the next vertical transfer is performed.

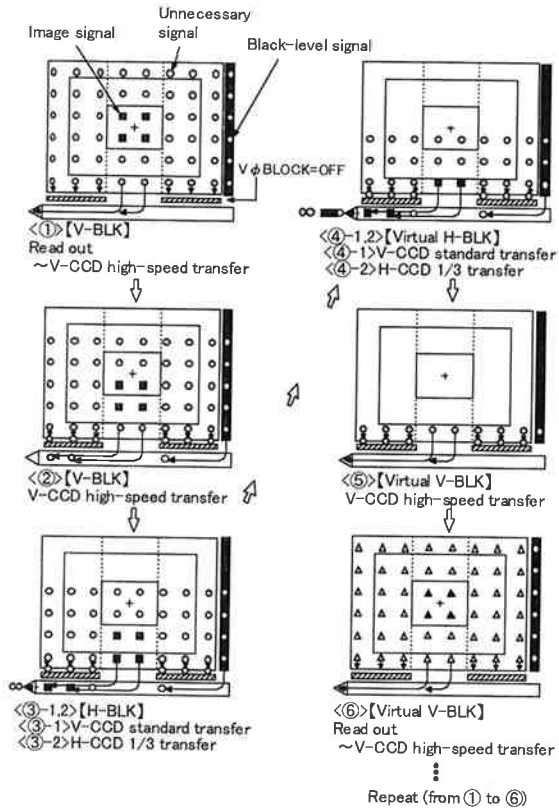


Figure 4: Principle of motion.

Fields/s can be increased by high frequency drive of the vertical CCD during the V-blanking (<5>, <6>) [3]. This method can read out the vertical effective area selectively. By combining these methods, in the best case, nine times the fields-readout rate can be obtained than with the normal method. Moreover, the number of fields/s can be selectable.

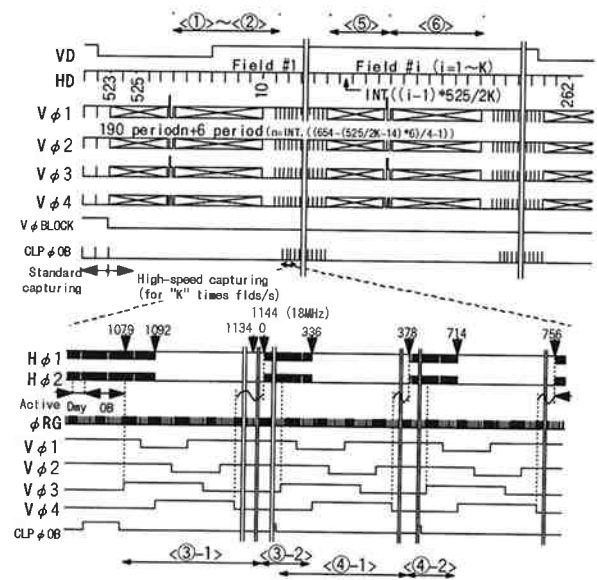


Figure 5: Clock timing.

This feature can have various advantages for image outputting. For example, an object can be captured in high-speed motion with this feature and played back by slow motion. Dynamic resolution can be higher than that captured by normal method. For static image output, excellent effects such as successive pictures with short time steps can be obtained. An example of an output image is shown in Figure 6.

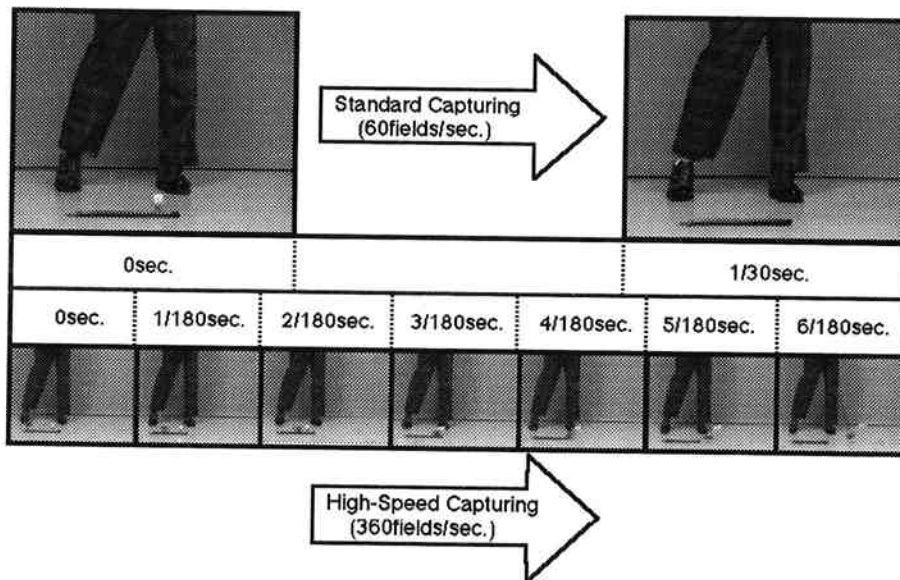


Figure 6: Example of output image (every 1 frame).

As shown in Figure 2, this CCD has a pixel array format composed of about 630K total effective pixels (962(H) x 654(V)). This format realizes various features, such as electric vibration stabilization with 33% for both the horizontal and the vertical direction, and provides high-quality pictures with exactly 16:9 aspect ratio [3].

The 630K pixels are realized in a 1/4-inch optical area, which is the main format of the image sensors for consumer video cameras. The pixel size is $3.80 \mu\text{m}$ (H) x $4.15 \mu\text{m}$ (V) (is 56% of the conventional 1/3-inch 630k-pixel CCD image sensor) for NTSC format, and $3.85 \mu\text{m}$ (H) x $3.50 \mu\text{m}$ (V) for PAL format. This pixel size is the smallest in the consumer market. The characteristics of this CCD are superior to the conventional characteristics of the 1/3-inch 630k-pixel CCD [3].

Table 1: Characteristics.

Optical format 1/4 inch
Image area 3.66(H) x 2.71(V)mm ²
Number of effective pixels 962(H) x 654(V)
Pixel size 3.80 x 4.15 μm^2
Sensitivity (color temperature=3200K) 44mV/lx
Saturation voltage 600mV
Smear level (V/10) -94dB
Horizontal resolution 570 TV lines (full-line output, color)
Vertical resolution 470 TV lines (full-line, field integration interlaced scan, color)

Sensitivity is 44mV/lx at 3200K color temperature, compared to 34mV/lx for a 1/3-inch 630k-pixel CCD. The smear level is -94dB compared to -90dB for a 1/3-inch 630k-pixel CCD. These sensitivity and smear are obtained by thinning the insulating film under the light-shielding layer and by increasing the light-gathering area of the micro-lens. Further, the saturation voltage of this CCD is equal to 600mV, which is obtained by fine patterning of the registers and sensors (the smallest size of pattern is $0.35 \mu\text{m}$), optimizing its impurity profile, and thinning down the register gate oxide.

In addition, charge conversion gain is raised by fitting the impurity profile of the transistors and decreasing parasitic capacitance around the floating diffusion. At the same time the signal to noise ratio is improved by MOS gate oxide of the output circuit about 30% thinner than that of the conventional MOS. The characteristics of this CCD are shown in Table 1. The on chip color filters are coded by complementary color mosaic (Yellow, Cyan, Magenta and Green).

5. Conclusion

We have developed a 1/4-inch 630k pixel IT-CCD image sensor with "High-Speed Capturing". To realize this function, we have developed a new CCD structure and driving method. With this structure, we can make the center of the image coincide with the optical center. We can also obtain, in the best case, nine times the fields-read-out rate and higher dynamic resolution than with the conventional method. In addition to these features, we can achieve such superior characteristics as high sensitivity, low smear, and large saturation voltage. All of these features are very effective and useful for various digital applications.

6. Acknowledgement

The authors would like to thank Mr. H. Matsumoto, Mr. T. Suzuki and Mr. A. Kayanuma for their encouragement and valuable suggestions and many people in SONY Kokubu Corporation and SONY Core Technology & Network Company, Semiconductor Company for their cooperation to development of this new CCD.

7. References

- [1]: Naito, Y., et al, "A 1/3-inch 360k-pixel Progressive-Scan CCD Image Sensor," ITE Technical Report vol. 20, No. 21, pp.1-6, Mar., 1996.
- [2]: Kobayashi, A., et al, "Video camera with high speed capturing feature.", ITE Technical Report vol. 20, No. 21, pp.7-12, Mar., 1996.
- [3]: Fujikawa, K., et al., "A 1/3-inch 630k-pixel IT-CCD Image Sensor with Multi- Function Capability," ISSCC Digest of Technical Papers, pp.218-219, Feb. 1995.