R32: On-Chip Focal Plane Filtering for CMOS Imagers

J. Huppertz, T. Kneip*, M. Schwarz, and B. J. Hosticka
Fraunhofer Institute of Microelectronic Circuits and Systems,
Finkenstraße 61, D-47057 Duisburg, Germany
Phone: +49 (0)203 3783-206, Fax: +49 (0)203 3783-266, email: huppertz@ims.fhg.de

Abstract

The use of the CMOS technology for imaging enables the cointegration of additional signal processing circuitry on the same chip as the imager. We propose an architecture for a CMOS imager with linear voltage readout and on-chip filtering. Instead of increasing the pixel complexity, we have realized the filtering at the periphery of the imager. Therefore, the pixel pitch can be preserved without degrading the fill factor and requiring large optics.

I. ARCHITECTURE

Figure 1 shows the architecture of the proposed CMOS imager with on-chip filtering. The imager contains a pixel array with each pixel consisting of a photodiode (formed by a drain diffusion and substrate) and reset, select, and source follower transistors. The pixel is operated in integrating mode and the imager employes rolling shutter with variable integration time.

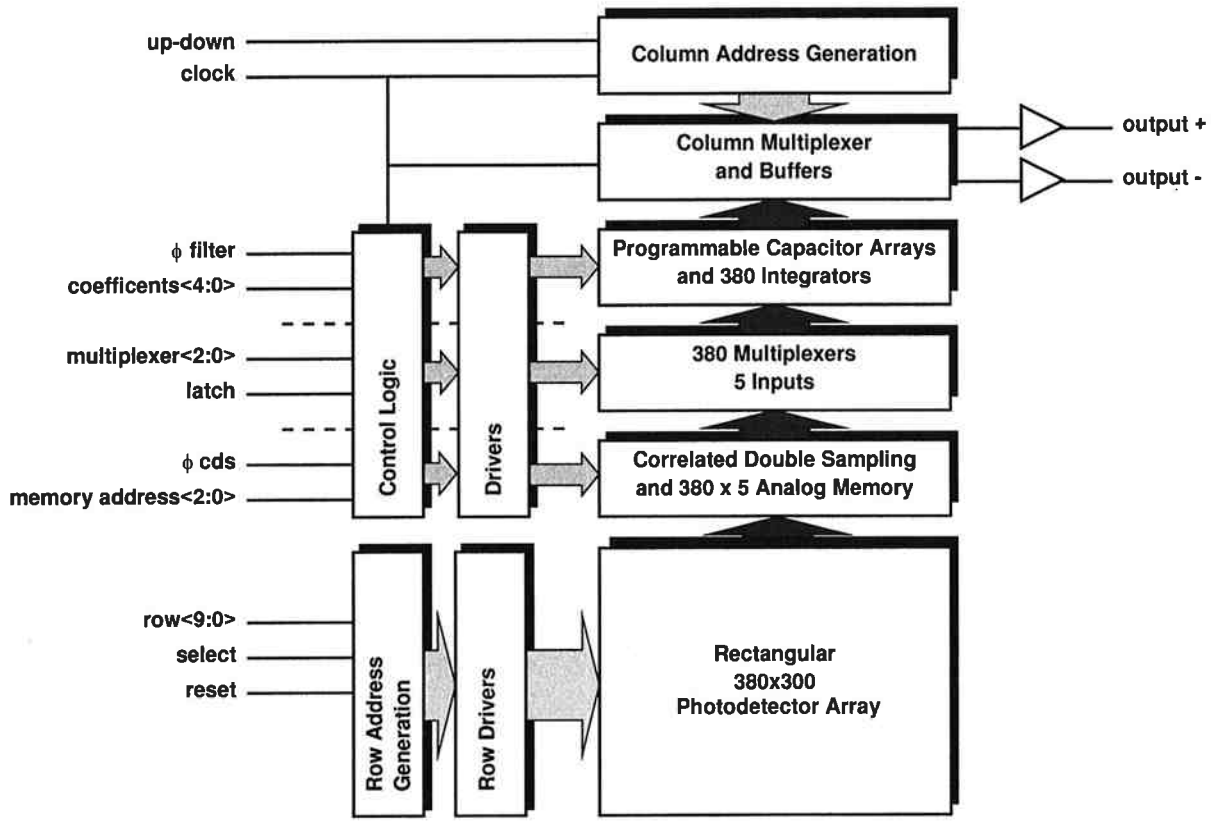

Fig. 1. Architecture of the Imager

*T. Kneip is now with Infineon Technologies, Design Center, Düsseldorf, Germany

The column readout amplifiers are based on analog switched-capacitor (SC) technique and employ correlated-double-sampling (CDS) in order to reduce low-frequency random and fixed pattern noise. They also convert the single-ended output signals of the pixels to fully differential signals needed for the filtering operation, the conversion ensures high noise immunity. After readout the pixel output signals are transfered into analog memory. Each memory cell contains a storage capacitor and a source follower for buffering and nondestructive readout. During the pixel readout cycle each column readout amplifier accesses successively all pixels of that column, while the corresponding memory cell is inserted into the feedback loop of the column readout amplifier in order to ensure a precise signal transfer and high linearity. The memory always records signals of the 5 last rows accessed. The access is shifted during frame processing in vertical direction thus allowing hardware multiplex. It can be thus modeled as 380-pixel wide window sliding along the y-axis.

II. Filter

The on-chip analog SC filter bank consists of 380 filter cells each connected to one column. The signals from neighbouring columns necessary for spatial operations are connected via multiplexer to each filter input. Since all 380 multiplexers allow connecting of 5 input signals each, the kernel processing size is 5×5, because the memory keeps 5 rows in store. Each filter cell contains a digitally real-time programmable SC integrator with reset capability. This allows realization of programmable two-dimensional FIR transfer functions. The filter bank operates in serial manner: all column input signals of a single row are processed in 5 time cycles and this is repeated row-by-row thus allowing 25-point calculation per pixel in each frame (see Fig. 2). Note that the

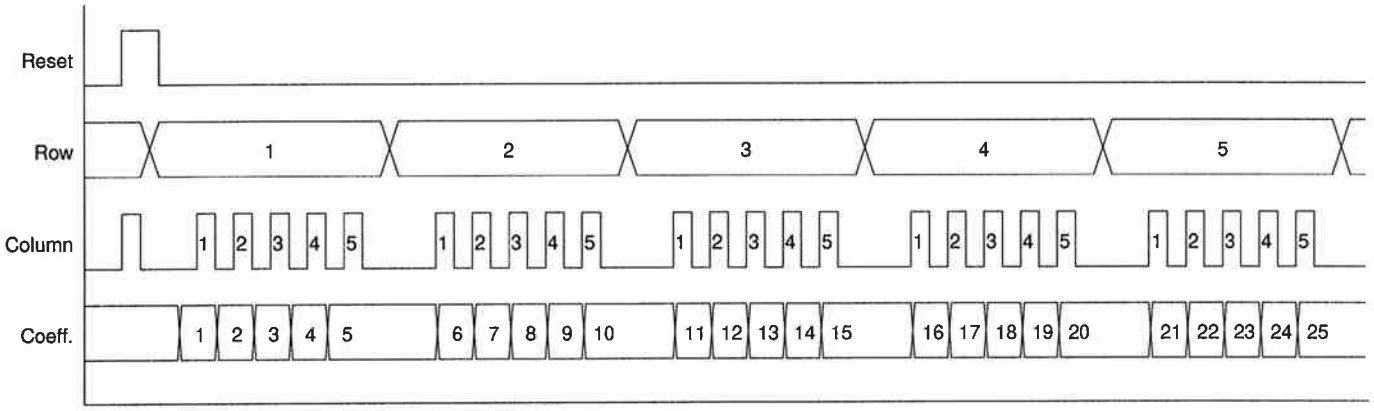

Fig. 2. Timing of the filtering operation

spatial displacement in horizontal and vertical directions appears as a time delay. Hence summing operations and the temporal-spatial reconversion of the result is achieved by employing a discrete-time integrator. This saves area, but it requires that the integrators are real-time programmable in order to realize various coefficients required for each point in the filter-kernel. For this purpose each SC integrator contains a capacitor array that is digitally real-time controlled. The filter bank performs 260 million multiply-and-add operations at 100 Hz frame rate.

III. Measurements

The chip has been fabricated in $1\mu m$ standard double metal CMOS technology. The total chip area including the imager is $140mm^2$ while the imager area is only $90mm^2$ (see Fig. 3). The imager contains a 380×300 pixel array with $17.2\mu m$ pixel pitch. Remaining technical data can be found in Table I. Figure 4 shows two images acquired by the imager without filtering. The scope hardcopy in Fig. 5 shows the differential output signal of a 5×5 binning operation. Trace 1 and 2 show the differential output signal, trace 4 is the reset signal for the filter, and trace 3 depicts the clock of the integrator. Note that at each clock period one coefficient is processed.

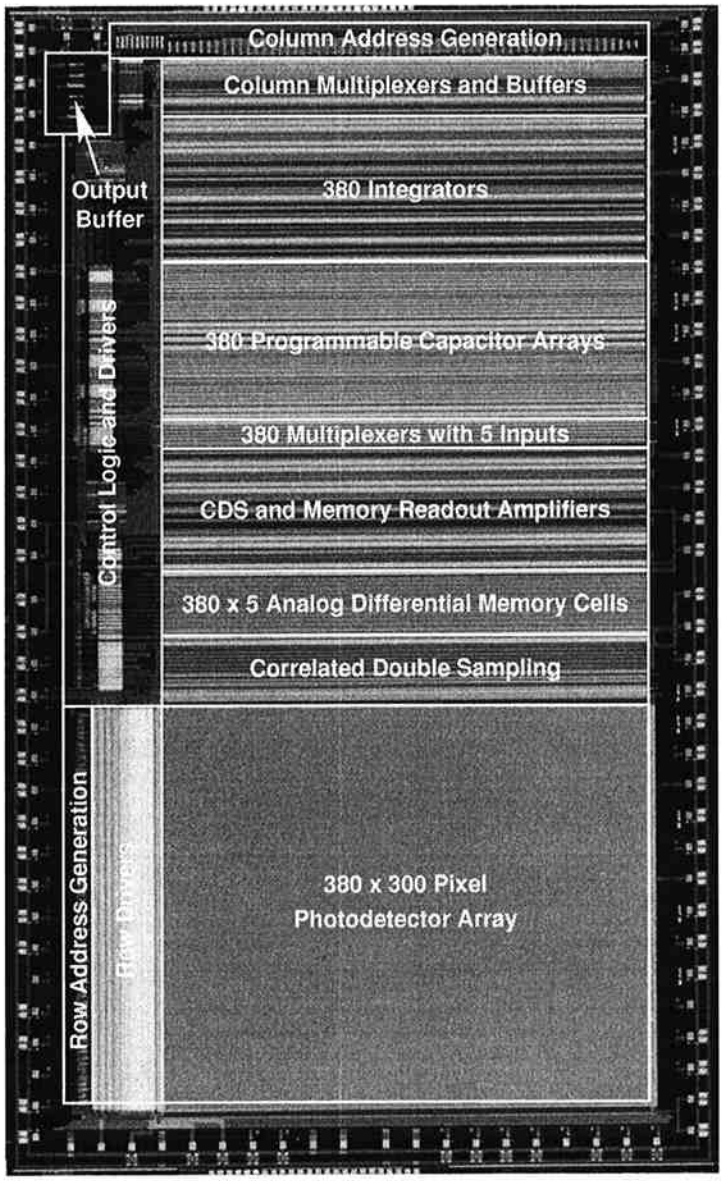

Fig. 3. Chip photomicrograph

IV. SUMMARY

In this contribution we have presented a CMOS imager with on-chip filtering. Unlike other inter-pixel processing approaches that incorporate image processing into the pixel matrix, we have employed off-matrix processing. When compared with in-matrix realization this yields high pixel fill factor and small lense diameter.

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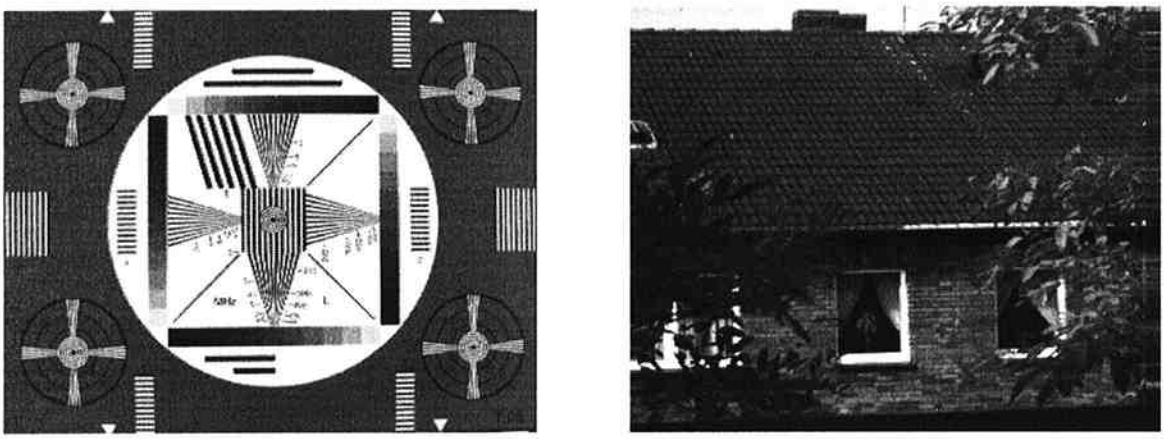

Fig. 4. Test images without filtering

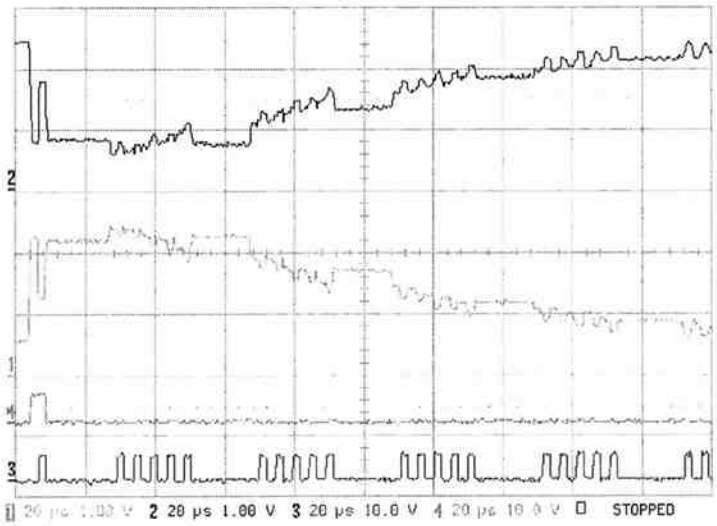

Fig. 5. Differential output signal of the filter

TABLE I
TECHNICAL DATA OF THE CHIP

Total pixel count	380×300	
Readout pixels	360×288	
Pixel pitch	$17.2\ \mu m \times 17.2\ \mu m$	
Chip area	$140\ mm^2$ in $1\ \mu m$ CMOS	
Sensor dynamic range	$> 60\,dB$	
Signal / noise ratio	$> 50\,dB$	
Conversion ratio	$4mV$	
Output voltage range	$2.1\,V$	$525,000\,e^-$
Fixed pattern noise	$< 2\,mV$	$800\,e^-$
Random noise	$< 2\,mV$	$800\,e^-$
Pixel clock	$> 20\,MHz$	
Frame rate	$> 100/s$	