(R31) Area Auto Focus CMOS sensor

Hidekazu Takahashi, Taku Ezaki, Mahito Shinohara, Shirou Furudate,
Hiroyuki Nakamura, Toshihiko Ichise, and Shigetoshi Sugawa
Device Development Center, Canon Inc.
6770 Tamura, Hiratsuka-shi, Kanagawa 254-0013, Japan
Tel +81-463-54-2211, Fax +81-463-53-9142, E-mail hide.takahashi@chcc.canon.co.jp

Abstract

We have developed a new CMOS area sensor for an auto-focus camera system. This device has been developed for our AF SLR (Auto-Focus-Single-Lens-Reflex) camera EOS-3 [1] [2] that realizes 45-point area AF. The area AF CMOS sensor is fabricated using 1.2 μ m CMOS process, which consists of new CMOS sensor cells, new CMOS memory cells, signal transfer circuits and peak monitor circuits. This device realizes low noise characteristics by new noise cancellation technology. The area AF CMOS sensor exhibits excellent performance such as a high sensitivity of 26.6V/lx·s and wide dynamic range of 73.6dB. In addition, this area AF sensor realizes the low power consumption, high-speed readout and on-chip peripheral circuit.

1. Introduction

Recently, CMOS sensors have begun to be used as AF sensors for SLR cameras [3], replacing traditional CCD and BASIS [4][5]. TTL-SIR (Through-The-Lens-Secondary-Imaged-Registration) AF system requires high signal to noise ratio (S/N). Generally, a CMOS sensor has been considered superior to CCD in low power consumption, X-Y address capability and on-chip peripheral circuits, but inferior to CCD in the S/N ratio. Realization of high S/N ratio is indispensable to the CMOS sensor to be used as the AF sensor for SLR cameras. On the other hand, increase in the number of focus points is demanded since AF SLR camera appeared in the world. Five focusing-point system is realized now, but are still not enough. Ideally, the camera capable of auto-focusing at any point in a viewfinder is desirable, but it has been difficult with a conventional line sensor technology to realize this area AF. We have developed a new CMOS area sensor to realize 45-point area AF. This area AF sensor not only increases the number of pixels, but also realizes high S/N ratio, high-speed drive and high precision auto-focus.

2. Area AF Concept

The optical system concept diagram is shown in Fig.1 [2]. This AF system is called TTL-AREA-SIR (Through The Lens-AREA-Secondary Imaged Registration). The subject image, which passes a photography lens, is formed in two positions on an AF sensor by secondary image-formation lens. Two sets of secondary image formation lenses are constituted in order to do the vertical line detection and the horizontal line detection. Focus information of a subject is obtained from distance of these two images, and the auto-focus control is performed. The viewfinder of EOS-3 is shown in Fig.2. Forty five focusing points are constituted in an area of 15mm×8mm of the viewfinder center. Highly precise cross-type auto-focus is possible at central 7 focusing points.

3. Device Structure

A chip photograph of the area AF sensor is shown in Fig.3. The chip size is 11.3mm×6.0mm, cell size of vertical line sensors and horizontal line sensors are 13.6 μ m×73.6 μ m and 13.6 μ m×101.6 μ m, respectively. Each area is curve shape in accordance with an optical system as shown in Fig.3. The Block diagram of this sensor is shown in Fig.4, which includes a sensor block, an analog block and a digital block.

The sensor block consists of vertical line sensors and horizontal line sensors. The vertical line sensors consist of two areas of 145 pixels×42 lines, and a horizontal line sensors consist of two areas of 56 pixels×18 lines. The vertical line sensors are divided into two blocks in order to perform high-speed control. The circuit constitution diagram of vertical line sensors is shown in Fig.5. The horizontal line sensors have approximately same circuit configuration with the vertical line sensors. The vertical line sensors consists of CMOS sensor cells, CMOS memory cells, signal transfer circuits, peak monitor circuits and block selection circuits. In the horizontal line sensors, AGC (Automatic Gain Control) is performed at individual line. In the vertical line sensors, each line is divided into plural (two or three) blocks and AGC is performed at each block. By the X-Y address capability along with the block selection circuit, the AGC can be performed at all 45 AF point individually.

The analog block consists of an AGC circuit to do the accumulation time control and the gain control, an analog amplification circuit to amplify sensor signals and a various voltage supply circuit. The gain of the analog amplification circuit and accumulation time of the sensor cell are decided by the AGC circuit and the peak monitor circuit of the sensor. The gain of the analog amplification circuit switches between four different values (×10, ×20, ×40, ×60).

The digital block consists of a timing generator for sensor drive, a communication circuit with a microcomputer and SRAM to memorize data such as accumulation time and AGC gain.

4. Basic operations

The basic circuit configuration is shown in Fig.6. The sensor and memory cells are both new CMOS active pixel sensors. Each pixel contains an inversion amplifier that has a gain of about –1.0. The transfer circuit consists of a source follower and a capacitance, which is a clamp circuit. Fixed pattern noise (FPN) can be canceled by this inversion amplification readout and the transfer circuit. This FPN cancellation technology is indispensable in order to do the precise AGC. Moreover, a high S/N output signal can be obtained by canceling reset noise of the sensor cell by inversion amplification type frame memory. Basic operational timing chart is shown in Fig.7.

① Reset operation.

First, Φ RES and Φ PS1 are turned into a high level, and the photo diode and the capacitance of the transfer circuit are reset. Next, Φ SL1 and Φ FT1 are turned into the high level, thus the signal begins to be read from the sensor cell, and is input into the transfer circuit. Then Φ FB1 and Φ PS1 are turned into the high level, and the signal from the transfer circuit is written in the photo diode again. Initial FPN of the sensor cell is returned to the photo diode with a gain of -1.0, so that the initial FPN can be canceled. Offset noise of the transfer circuit is written into the sensor cell at the same time. Then a noise signal from this sensor cell is written into the memory cell through the transfer circuit. This memorized noise signal is used for noise cancellation of the last output signal.

② Accumulation operation.

AGC operation is performed during accumulation period by peak monitoring of the sensor signal. A conventional line-type AF sensor monitors the voltage of each photo diode at real-time [2], but this operation is difficult in case of area sensors because of the layout size limitation. Accordingly, it is monitored by time sharing method, but several thousand times of sensor readout operation becomes necessary by maximum. Therefore the CMOS sensor with completely non-destruction readout is required. Φ SL1, Φ FT1 and Φ FB2 are turned into the high level, and the peak monitor signal of the photo diode is output. In this mode, FPN of the sensor cell and the transfer circuit are canceled. The major noise component of the AGC signal is a reset noise of the sensor cell.

③ Memory write operation.

A signal is read from the sensor cell after the accumulation period, and the signal is written to the memory cell. First, Φ SL1 and Φ FT1 are turned into the high level, and a signal from the sensor is clamped by the transfer circuit. Next, Φ SL2 and Φ FT2 are turned into the high level, and the initial noise is input into the transfer circuit from the memory cell. Φ PS2 is turned into the high level, and the output from the transfer circuit is written into the memory cell again. In this mode, RN of the sensor cell, FPN of the sensor cell, the transfer circuit and the memory cell are canceled. The major noise component of RN is a reset noise of the memory cell, but it can be made small enough by designing the memory capacitance large.

④ Signal readout operation.

A signal begins to be read using a horizontal shift register from the memory cell to the analog amplification circuit after all the signal writes from the sensor cell to the memory cell were finished.

5. Characteristics

Photo-electronic conversion characteristics is shown in Fig.8. This characteristics is obtained under the conditions as follows : 1.03ms accumulation time, the light source with color temperature of 2854K, IR cut filter with cutoff wavelength of 740nm. The measurement values are taken before the analog amplification circuit. The conversion linearity has been obtained in the range of the output voltage from about 1mV to 1200mV. Sensitivity of 26.6V/lx·s and saturation voltage of 1200mV are obtained from Fig.8. The characteristics of this sensor is shown in Table.1. Sufficient values are obtained as the AF sensor. FPN and RN are suppressed at the level that is not a problem in practical use by new noise cancellation technology of this sensor. RN at room temperature is $0.25mV_{rms}$. Dynamic range for RN is 73.6dB. Dark current density is $0.3nA/cm^2$ at the ambient temperature of 45 ℃. Since dark current shot noise cannot be canceled, dark current reduction is necessary in order to increase operation range in low brightness. High sensitivity of about 1700V /lx·s is achieved in the highest gain setting, therefore an AF operation in low brightness is made possible. The AF operation range of EOS-3 is EV 0 to 18 (108dB), which is comparable to conventional system.

6. Conclusion

A new CMOS area sensor to realize an area AF has been developed. The area AF CMOS sensor is successful in increasing the number of AF points without losing AF performance such as AF speed, AF precision and AF ability in low brightness. This device realizes low noise characteristics by new noise cancellation technology . The area AF CMOS sensor exhibits excellent performance such as a high sensitivity of 26.6V/lx·s and the wide dynamic range of 73.6dB. AF SLR camera EOS-3, which uses this area AF sensor, realizes 45-point area AF for the first time in the world.

7. References

[1] "EOS-3 Test Report", Photographic Industries, vol.57, no.598, pp55-68, Feb.1999.

[2] Canon EOS-3 Technical Overview

[3] M. Uno, "A CMOS Linear Image Sensor for Passive Auto Focusing Systems", Annual Meeting of SPSTJ'96, A20, pp69-71, May1996.

[4] N. Tanaka, T. Ohmi, and Y. Nakamura, "A Novel Bipolar Imaging Device with Self-Noise-Reduction Capability", IEEE Trans. Electron Devices, vol.ED-36, no.1. pp31-38, Jan.1989.

[5] N. Tanaka, T. Ohmi, Y. Nakamura, and S. Matsumoto, "A Low-noise Bi-CMOS Linear Image Sensor With Auto-Focusing Function", IEEE Trans. Electron Devices, vol.ED-36, no.1. pp39-45, Jan.1989

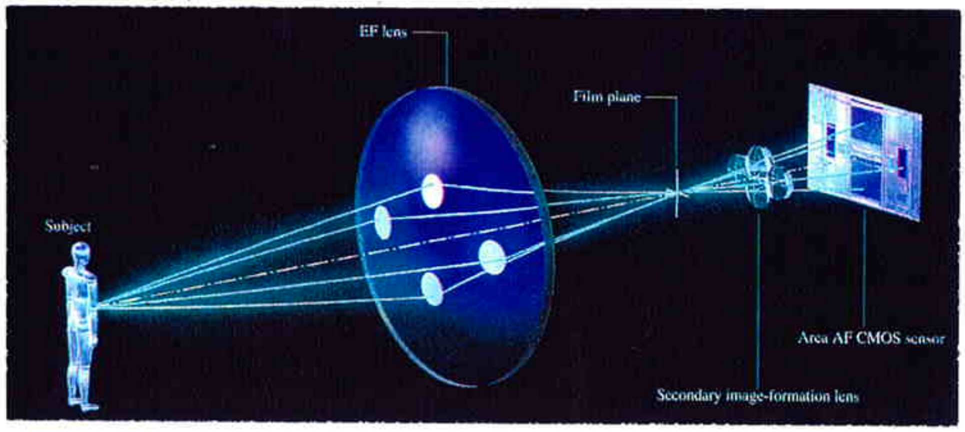


Fig. 1 Optical system conception diagram

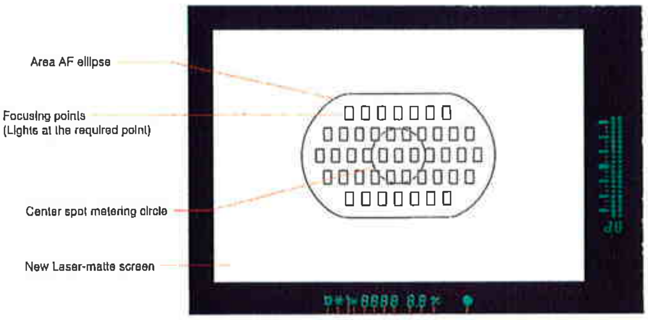


Fig. 2 Viewfinder display

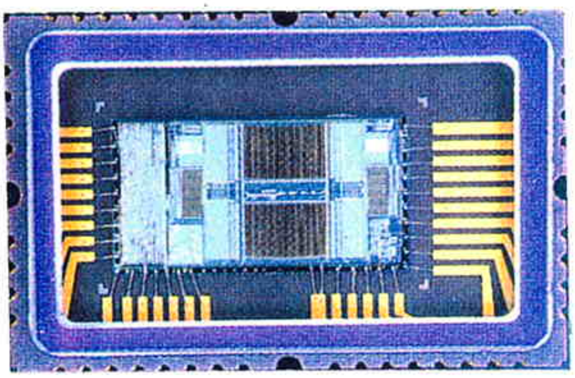
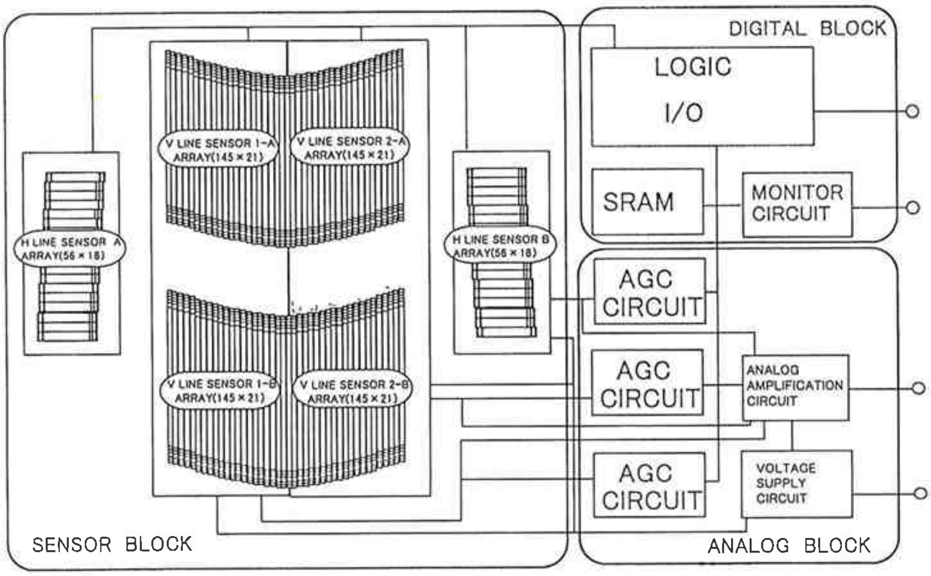


Fig. 3 Chip photograph



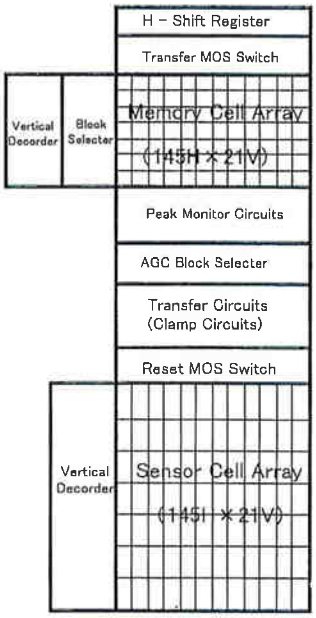


Fig. 4 Block diagram

Fig. 5 Circuits constitution of vertical line sensors

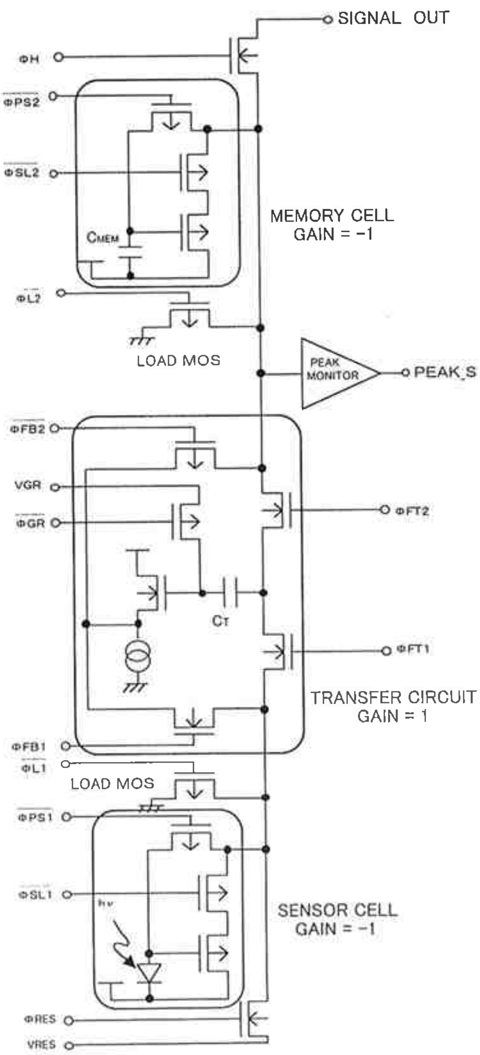


Fig. 6 Basic circuit configuration

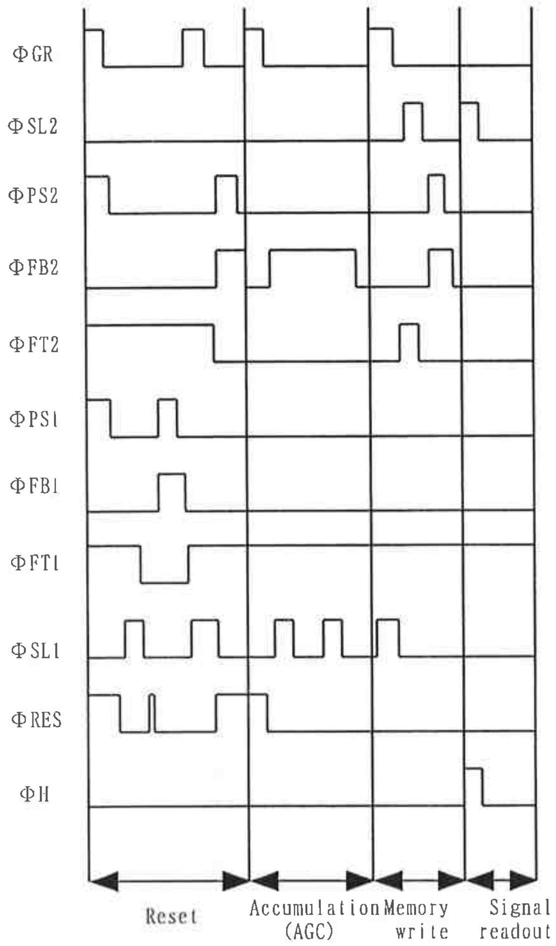


Fig. 7 Basic operational timing chart

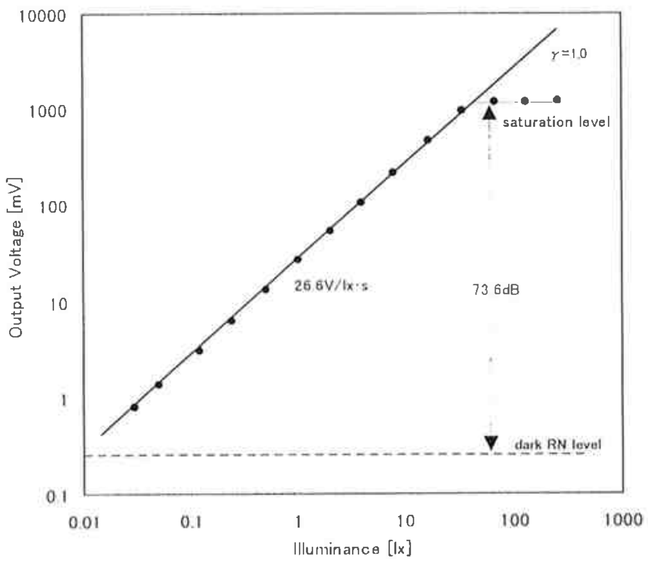


Fig. 8 Photo-electronic conversion characteristics

Pixel size	13.6 μm × 73.6 μm 13.6 μm × 101.6 μm
Number of effective pixels	145 (H) × 42 (V) × 2 56 (H) × 18 (V) × 2
Chip size	11.3mm × 6.0 mm
Process	CMOS Technology
Design rules	1.2 μm
Saturation signal	1200 mV
Dark random noise (R.T)	0.25 mV_{rms}
Dynamic range	73.6 dB
Fixed pattern noise	3 mV_{pp}
Sensitivity	26.6 V/lx·s
Power supply	5.0V
Power dissipation	150 mW
Package	32pin Ceramic LCC

Table. 1 Device specification and performance