

R18 A Stacked CMOS APS for Charge Particle Detection and its Noise Performance

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Abstract

A stacked CMOS active pixel image sensor(APS) has been developed for detecting various kinds of charged particles. In this talk, we present the image sensor architecture along with its pixel structure and operational principle. Also, preliminary experimental results on noise performance are addressed.

1. INTRODUCTION

Charge particles such as ions and electrons with kinetic energy of keV order are useful probes for surface analysis of material. A measurement system which yields two-dimensional image of charge particles with wide dynamic range and high accuracy is strongly demanded.

The conventional system uses a micro channel plate(MCP), a florescent plate which generates a visible image from multiplied secondary electrons, and a visible image sensor[1]. However, its limited dynamic range and non-linearity in the electron-to-photon conversion process make a quantitative measurement difficult.

The proposed system using a stacked CMOS APS has several advantages over the conventional system such as high spatial resolution, no insensitive time, wide dynamic range, nondestructive readout(NDRO) capability, high robustness and low power consumption[2].

2. PIXEL STRUCTURE AND OPERATIONAL PRINCIPLE

The circuit configuration and a schematic cross sectional view of the stacked APS are shown in Fig. 1(a) and (b), respectively. Three layers of metal are stacked on so called a photodiode APS or AMI (Amplified MOS Imager) with three transistors. The top metal layer named "pixel electrode" receives charge particles and protects the device underneath. Another two layers of metal are used for electric interconnection and device flattenization.

Charge particles which hit the pixel electrode release secondary electrons or ions due to the interaction at the surface of the pixel electrode. A part of the incident charge particles is hit into the electrode. The pixel electrode is thereby charged through these interactions. The generated carriers are integrated on the pixel capacitor C_{PIX} . The feature of this pixel structure is that the detecting part of charge particles and the carrier integrating part are separated. It results in the protection of the device from the high energy collision of the charge particles and the effective carrier transport to the pixel capacitance even for the charge particles with energy of eV-keV, for which the interaction depth from the surface is shorter than 10nm.

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The pixel accepts either negative charge carriers(electrons) or positive charge carriers(holes).

3. ION DETECTION

The circuit configuration of the stacked APS (AMI) for ion detection is shown in Fig. 2. A off-chip load resistor is put at the end of the horizontal signal line and forms a source follower with the driver transistor M_{RD} inside the pixel. Typical readout rate is 50 $\mu\text{s}/\text{pixel}$.

Because irradiated ion density is very low, signal integration time should be longer than a second. Therefore, the APS is cooled to reduce the thermal leakage current.

Responsivity for ions in the stacked APS was measured using a secondary ion mass spectrometer (SIMS) CameraIMS-3F[2]. Positive secondary ions ($E = 4.5\text{eV}$) emitted from a specimen equipped at the spectrometer were irradiated at the center of the image area of the stacked APS. The irradiation currents were monitored before and after the irradiation period to the APS by a Faraday-cup and a secondary electron multiplier. Fig. 3 shows the experimental setup. Ion transfer characteristics along with the noise behavior are shown in Fig. 4. Dynamic range of 1.1×10^4 with good linearity was obtained. A reproduced ion image is shown in Fig. 5.

Though this system can be used for some applications in the field of SIMS, much wider range of applications should appear if the noise floor is reduced to less than one ion. Since multiplication factor between generated charge and an incident ion is experimentally estimated 2.5~5 when 4.5 keV Al ion is irradiated, noise floor of lower than 5 electrons should be a target of the next step improvement .

4. PIXEL NOISE MEASUREMENT

In order to analyze pixel level noise at low temperatures, preliminary experiments were performed using a test pixel structure which was fabricated on 1.2 μm 5V CMOS process. Pixel capacitance is estimated to be 28 fF from its layout and process parameters. The readout transistor size is $W/L=2.1/1.2$ μm . First, the source follower noise was measured by turning the reset transistor constantly on while reading the output signal every 50 μs . Then the test structure was driven in a normal mode where the reset pulse was applied every 50 μs as shown in Fig. 6. The output signal was converted to a digital value with a 16 bit A/D converter and a frequency spectrum was obtained with FFT(Fast Fourier Transform). Pixel noise was measured both at room temperature(RT) and liquid nitrogen temperature(LNT) of 77K.

Fig. 7 (a) and (b) show the frequency spectra obtained at RT and LNT, respectively. Noise voltage is expressed as equivalent voltage at pixel electrode. The source follower noise exhibits 1/f characteristics over the experimented frequency range from 1Hz to 20kHz. It is found that the 1/f noise voltage at LNT decreased about 1/2 of that at RT. The noise spectra obtained from a normal operating mode is white, that means that every data after a reset has no correlation each other. It is seen that the temperature dependence is quite weak. The noise voltage obtained by integrating the spectrum over the bandwidth is 0.9 mV_{r.m.s.} at RT. This value is not consistent with the estimated value of 0.4 mV_{r.m.s.} ($C_{PIX} = 28\text{fF}$) derived from the conventional kTC noise formula. These preliminary results will be detailed in the workshop.

Although noise generated by reset operation can be suppressed by the correlated double sampling between before and after the ion irradiation period using non-destructive readout capability of APS, the $1/f$ noise component would still remain. Thus the $1/f$ noise has to be reduced in order to detect single ion.

5. CONCLUSIONS

A practical solid-state imaging device for charge particles with energy range from eV to keV has been realized with a stacked active pixel sensor. Features of this stacked CMOS APS include;

1. Two dimensional detection of charge particles such as ions or electrons.
2. No insensitive time due to its integrating mode
3. Small irradiation damage due to the separate charge particle-to-carrier conversion at the pixel electrode which covers the device underneath.
4. Other advantages of APS, such as NDRO capability, low power consumption, are retained.

These features will provide a new two dimensional detecting method in various material analyses such as mass spectroscopy. Further reduction of noise floor is needed to obtain a solid-state detector array with wider dynamic range.

REFERENCES

- [1] Mantus D.S. et al., "Secondary Ion Mass Spectrometry SIMS VII", Edited by A. Benninghoven et al., p.921 (1990), (J. Wiley & Sons, New York)
- [2] Matsumoto et al., IEEE Trans. Electron Devices, vol. 40, no. 1, pp. 82-85, January 1993.

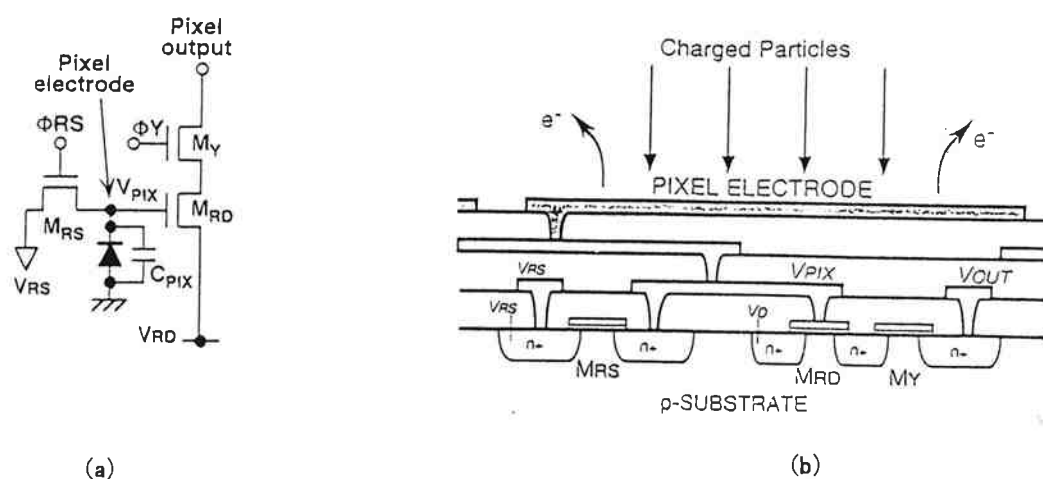


Fig. 1 (a) Circuit configuration and (b) cross sectional view of the pixel unit.

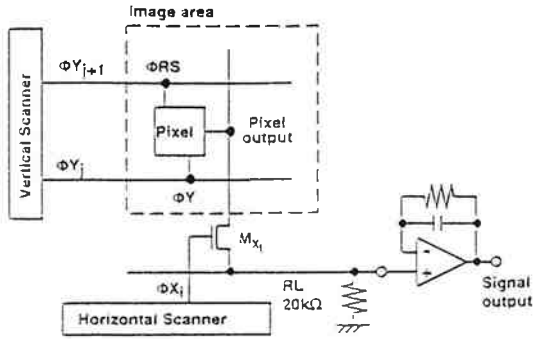


Fig.2 Circuit configuration of the Stacked APS(AMI) for ion detection.

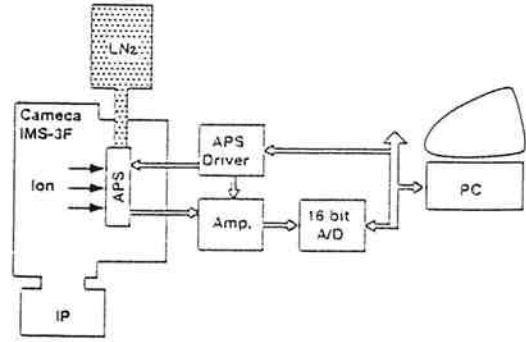


Fig.3 Block diagram of evaluation system.

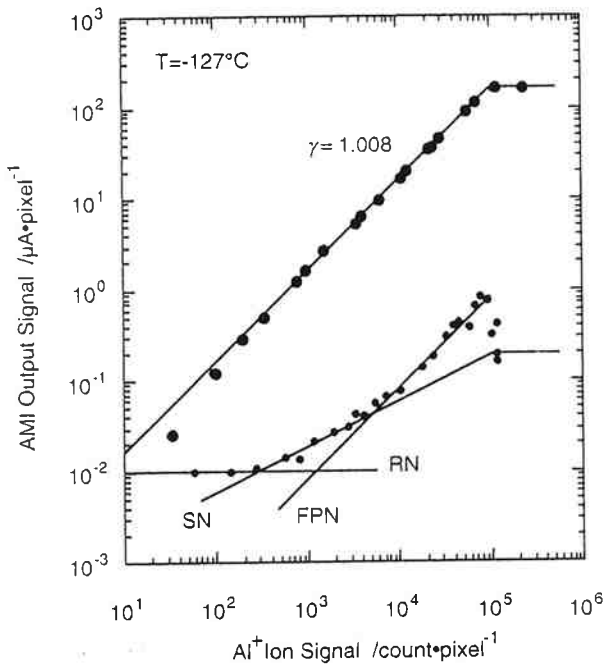


Fig. 4. Ion transfer characteristics

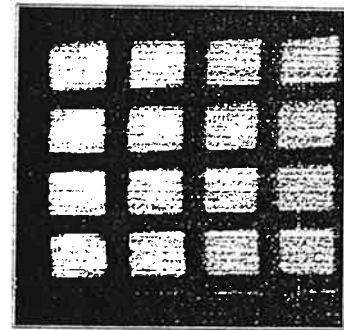


Fig.5. Reproduced ion image.

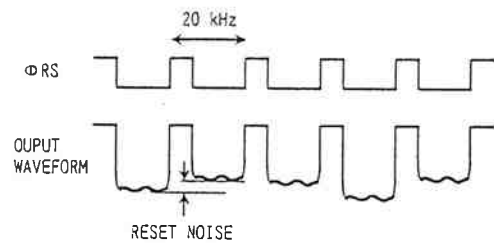
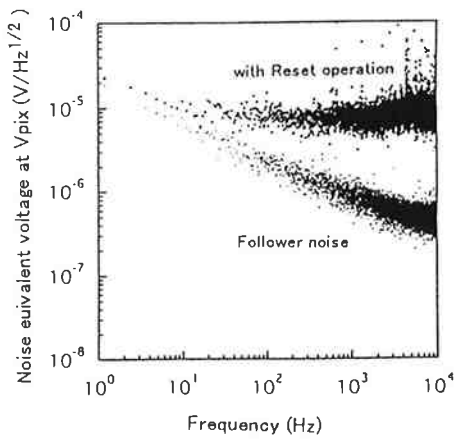
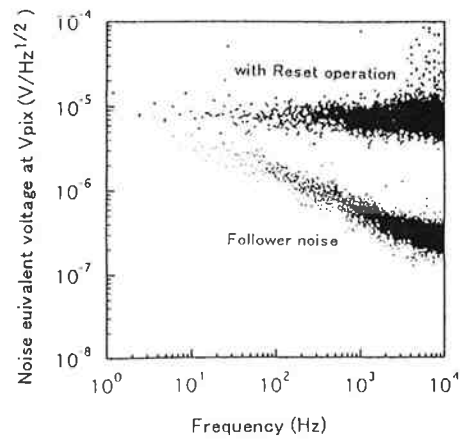


Fig.6 Pulse timing for pixel noise measurement



(a)



(b)

Fig. 7. Frequency spectra of pixel noise at (a) room temperature and (b) liquid N₂ temperature.