

## A CCD-CMOS Image Sensor for Ultra-High Speed Image Capturing

T. Etoh\*, H. Mutoh\*\* and K. Takehara\*

\*Kiniki University, Higashi-Osaka, 577-8502 JAPAN

\*\*Link Research Corporation, 1-18-5 Kojima, Taito-ku, Tokyo, 111-0056 JAPAN

### ABSTRACT

A layout of an ISIS, In-situ Storage Image Sensor, for ultra-high speed image capturing is presented, which consists of slanted CCD storage and amplified CMOS readout. The layout has two different sets of orthogonal axis systems: one is mechanical and the other functional. Photodiodes, CCD registers and all the gates are designed parallel to the mechanical axis system. The squares on which pixels are placed form the functional axis system. The axis systems are inclined to each other. The inclined design inlays the straight CCD storage registers for fifty to one hundred images in the photo-receptive area of the sensor. The amplified CMOS readout circuits built in all the pixels eliminate line defects in reproduced images, which are inherent to CCD image sensors. The yield rate is significantly improved by the elimination of the line defects. It is pointed out that MOS-type readout circuitry in the presented design can be fabricated by a usual CCD process line.

**Keywords:** ISIS, CCD, high-speed video camera, CMOS-APS

### AN ISIS WITH SLANTED CCD STORAGE AND AMPLIFIED CMOS READOUT

#### **a. Direction for Development**

An ISIS, in-situ storage image sensor, is most promising as a sensor for an ultra-high speed video camera. Kosonocky et al.[1] proposed and fabricated an ISIS with an SPS (Series-Parallel-Series)-type CCD register for storage within each macro-pixel. A problem associated with the design is sudden change in charge transfer direction from a horizontal to parallel vertical CCD registers.

CCD registers are preferably straightly elongated without any direction changes. If straight CCD registers are employed for in-situ storage without any bends, each CCD storage register associated with each photodiode straightly extends, penetrating several macro pixels. The basic idea of the authors in development of the ISIS with CCD storage registers is to find a technically-sound two-dimensional layout for inlaying photodiodes and associated straight CCD storage registers on a photo-receptive area of the sensor with no waste of space, instead of enclosing the storage registers within each macro pixel.

#### **b. Slanted Dual-axis System**

The proposed layout is shown in Fig. 1 in the last page.

In the layout, there are a pair of orthogonal axis systems; one is the mechanical axis system and the other the functional axis system. Each photodiode, each CCD register, and each of all other gates are designed in parallel to and orthogonal to the mechanical axis system. Centers of macro pixels, i.e., the centers of the collection well in Fig. 1, are located on the grid points of the functional axis system. The two axis systems are not parallel, but inclined to each other, which makes it possible 1) to extend straight CCD storage registers through several macro pixels, and 2) to place macro pixels in a square grid array.

#### **c. Photodiodes, Channels and Gates**

A macro pixel includes a pair of photodiodes and six CCD transfer channels, among which one CCD channel transfers image signals generated in the pair of photodiodes extending downwards and penetrating six macro pixels, and other five channels transfer image signals of photodiodes of other macro pixels.

A collection well is placed at the center of each pair of photodiodes, from which image signals are transferred to the CCD register through the input gate. Image signals are transferred on the register through the length of six macro pixels, and drained through the drain and, then, to the outside of the sensor, which defines "a CCD storage segment", from the input gate to the drain. This provides an overwriting

mechanism during an image capturing phase, i.e., updated fifty to one hundred image signals for each pair of photodiodes are always stored in the elongated CCD storage segment and older ones are continuously drained to the outside of the sensor.

An overflow/reset gate is placed at the right side of the collection well, which eliminates blooming and serves for on-chip gating.

#### **d. Amplified CMOS Readout**

At the end of each CCD storage register, a CMOS readout circuitry with in-situ amplifier is placed. In a read-out phase after release of a trigger signal to cease the continuous image capturing operation, the image signals are transferred in a longitudinal direction as employed in usual CCD operations, and, then, amplified and read out to a readout circuit placed outside of the photo-receptive area. Since the readout frame rate is very low, thirty times of amplification is easily done by a small amplifier, which compensates random noise.

## **PERFORMANCE**

#### **a. Chip Size, Spatial Resolution and Fill Factor**

CCD pitch is 3 to 5 microns, depending on the design rule. In the design shown in Fig. 1, eight CCD elements are placed in each macro pixel. For 5-micron CCD pitch, the length of a macro pixel is 40 (=8x5) microns. For smaller pitch and/or larger size of a macro-pixel, more storage registers can be placed.

When the numbers of columns and rows of a CCD storage register of each macro-pixel are 7x14 and the CCD pitch is 3 microns, the storage capacity increases to 98 (=7x14) and the size of a macro-pixel is 42x42 (=14x3) square microns. The area for the storage CCD register is 50 %. Therefore, the fill factor can be more than 30 % without on-chip micro lenses.

The size of the photo-receptive area is about 12x12 mm, which can be fabricated by a common stepper. As the size of a macro-pixel is about 40x40 square microns, number of macro pixels in the photo-receptive area are about 300x300 (=12,000/40).

#### **b. Frame Rate and Fill Factor**

The frame rate of an ISIS basically depends on transfer rate on the CCD registers. Rates of operations of input and drain gates also restrict the frame rate. The maximum transfer rate of current FIT-CCD sensors is about 5 MHz. Therefore, it is not difficult to achieve 1,000,000 pps.

#### **c. Noise Reduction**

The design provides the uni-direction transfer on CCD registers and amplified CMOS readout, both effectively serving for noise reduction.

FPN, Fixed Pattern Noise, due to individual amplification is serious in CMOS image sensors for consumer cameras. In scientific and engineering applications, digital post processing is commonly applied. Fixed noise without temporal change can be easily eliminated by the digital processing. Therefore, the FPN is not a significant problem in the proposed design.

#### **d. Yield Rate**

The design effectively suppresses the occurrence probability of line defects inherent to CCD imagers. For example, if a small dust particle falls on a CCD channel during production stage, image signals generated in upper macro pixels connected to the channel cannot be transferred through the point, causing a line defect. In the present design, each CCD channel is connected to only one pair of photodiodes of one macro pixel, and, thus, if a channel is blocked by a dust particle, image signals only for the associated macro pixel cannot be readout and the defect remains as a point one.

The length of each CCD channel is short. Image signals are transferred on 50 to 100 CCD elements. If overall transfer efficiency of 95% is required, the transfer efficiency of a single element is only 99.9%. This is very low level compared to the current standard of 99.999%. This increases the yield rate and decreases the production cost.

#### **e. Intermittent Operation**

Another advantage of the design is introduction of intermittent operation in a camera-setting phase to avoid heating. To reproduce continuous movement on the monitoring for camera-setting at the frame rate of 30 pps, image signals for a single image should be read out within 1/30 second. If CMOS readout is not employed and image signals are read out all the way through CCD registers, it takes more than 1/30 second and the continuous operation of the CCD registers in higher voltage, as explained below, generates heat.

On the other hand, in the present design, image signals for the single image are transferred on only 50 to 100 CCD elements, which requires less than 1/10,000 second. Then, the image signals are slowly read out through CMOS readout circuitry.

#### **f. Voltage**

In design of image sensors for a domestic consumer use, which should be handy, battery consumption is one of the most serious problems. Thus, lower voltage is one of the major technical targets.

On the other hand, application of higher voltage is the most practical way to increase transfer capacity and/or rate. In high-frame-rate image capturing, very strong illumination is necessary, which requires high electric power. Therefore, seeking a design for lower voltage makes no sense for high-frame-rate image capturing.

#### **g. Summary of Performance**

The present design achieves the following performance:

- (1) Frame rate: 1,000,000 pps
- (2) Resolution: 300x300 pixels
- (3) Relatively large fill factor: 30%
- (4) Number of consecutive images: 50 to 100
- (5) Less noise
- (6) High yield rate
- (7) Overwriting mechanism for synchronization of image capturing to the occurrence of an event of interest

A micro cylindrical lens, a color filter array, etc, can be attached to the sensor, to provide additional higher performance.

### **FABRICATION OF CMOS READOUT CIRCUITRY BY CCD PROCESS LINES**

MOS transistors can be fabricated on CCD process lines. The design rule is, however, significantly large, i.e. 1 to 2 microns, because the lines are optimized for CCD processing. The area of a CMOS-APS readout circuitry within a macro-pixel designed in the rule may reach 100 square microns. The size of a pixel is about 40x40 (=1,600) square microns. Therefore, the portion of the area of the readout circuitry to the pixel area is less than 6.7 %, which is allowable.

One of advantages of CMOS image sensor is low energy consumption. As mentioned above, this is not a major technical target in high-speed image capturing. Therefore, n-MOS circuitry can replace CMOS circuitry to reduce the area for the amplified readout by further deleting some transistors.

Since FPN is not a significant problem, as previously explained, transistors for circuitry to suppress FPN are also unnecessary.

Consequently, for the proposed design, a CMOS (or n-MOS)-APS XY-readable readout circuitry can be fabricated within a macro pixel by CCD process lines.

Large-size transistors require slower operation. Readout circuitry is operated in a readout phase at a low frame rate after cease of an image capturing phase. Therefore, in the proposed design, the transistors can be fabricated by the larger design rule.

### **CONCLUSION**

A layout of an ISIS, In-situ Storage Image Sensor, for ultra-high speed image capturing is presented, which consists of slanted CCD storage and amplified CMOS readout. The sensor achieves the following performance:

- (1) very high frame rate (1,000,000 pps), (2) reasonable resolution (300x300 pixels), (3) relatively large fill factor (30%), (4) the minimum and sufficient storage capacity to reproduce moving images (50 to 100), (5) less noise, (6) high yield rate, and (7) overwriting mechanism for synchronization of image capturing to the occurrence of an event of interest.

It is also pointed out that MOS-type readout circuitry in the presented design can be fabricated by a usual CCD process line.

## REFERENCE

1. F. W. Kosonocky, Lowrance, et al., "360x360-element very-high frame-rate burst-image sensor", Digest of Technical Papers, ISSCC96, pp.182-183, 1996.

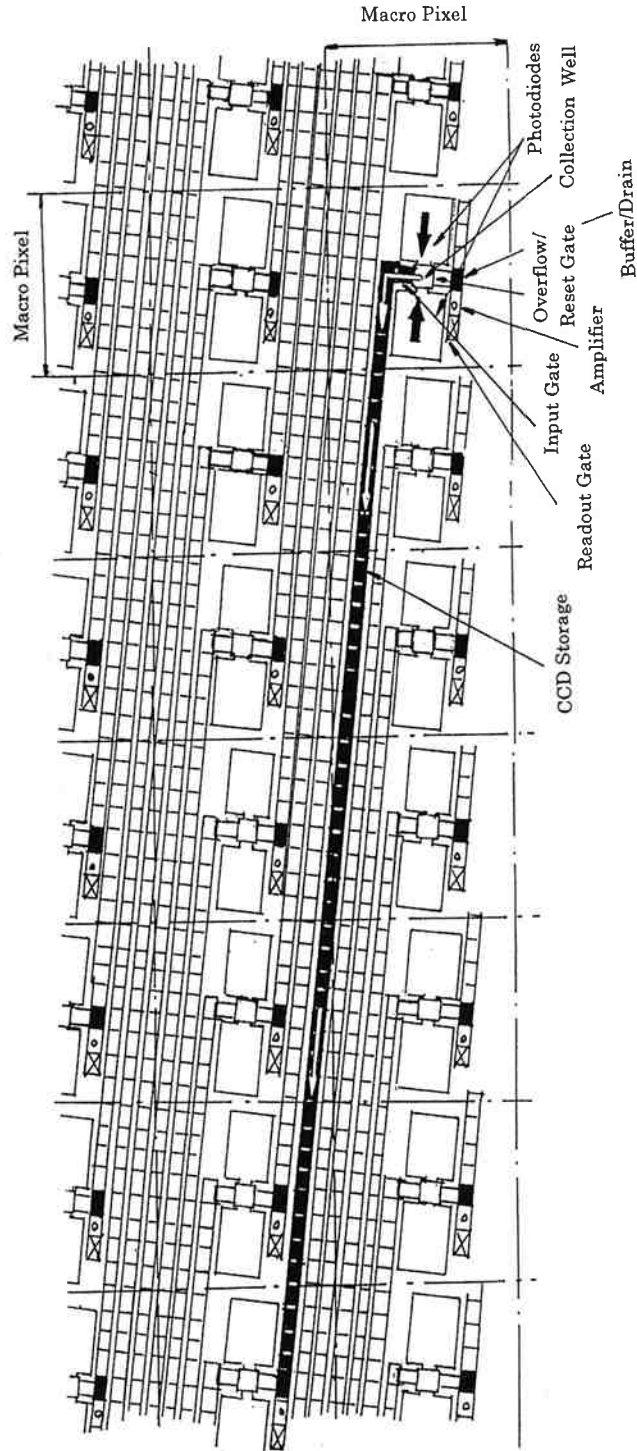


Fig.1 An ISIS with SLANTED CCD storage and amplified CMOS readout