P8 : On-chip offset calibrated logarithmic response image sensor

Spyros Kavadias, Bart Dierickx, Danny Scheffer
IMEC, Kapeldreef 75
3001 Leuven, Belgium
Tel. + 32 16 28 16 86, Fax. +32 16 28 15 01
e-mail : kavadias@imec.be, dierickx@imec.be, scheffer@imec.be

Abstract

A CMOS image sensor with logarithmic response is proposed. The basic feature of this sensor is the suppression of the fixed pattern noise through calibration with a reference current. The high dynamic range, which is related with the logarithmic response, is combined with a readout process that provides a signal free from offsets due to non-uniformities in device parameters.

1. Introduction

The major drawback of logarithmic CMOS image sensors compared with their linear counterparts, is the increased Fixed Pattern Noise (FPN). This noise is caused from the non-uniformities of the parameters associated with the various devices present on the sensor chip. It appears as an offset in the output signal delivered by the each pixel. In integrating sensors the photocurrent is integrated on a capacitance over a well-defined time period therefore, methods for the elimination of this offset have been proposed based on the readout of the voltage of the integrating capacitance during two states.

Sensors employing pixels with logarithmic response are very attractive devices in applications where a high dynamic range is required. However, they suffer from high FPN due to the non-availability of two distinct pixel levels as in the case of integrating sensors. A few techniques to suppress this noise have been proposed in the literature [1],[2].

The present work is an attempt to tackle this problem. A new pixel structure with logarithmic response is introduced where offset extraction is possible. The offset extraction is accomplished through the calibration of each pixel against a known reference. In the following paragraphs the principles of operation are presented as well as the actual implementation details. The pixel operation will be assessed by means of circuit simulation.

2. Principles of Operation

The basic idea in order to suppress the FPN is to calibrate each pixel against a known reference. This reference is a current source in place of the photodiode. Figure 1 shows the basic pixel structure, where transistor M1 acts as the bias of the photodiode and provides the logarithmic response, M2 is the driver transistor of the on-pixel source follower and M3 is used for row selection. Transistor M4 connects the pixel to the calibration source I_{cal} which is common for pixels lying on the same column. Transistor M5 connects the photosensitive node to the gate of M2. The calibration process is accomplished in two states. First, M4 is switched off and the pixel voltage is stored. This voltage is logarithmically related to the photocurrent delivered by the photodiode shown also in the figure. Then, M4 is switched on and the pixel output is again sampled and extracted from the previous level. The difference between these two levels has a very small offset provided that I_{cal} is much higher than the photocurrent.

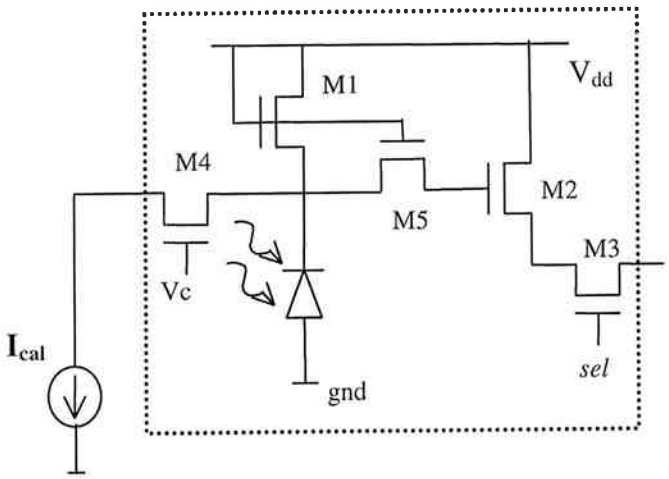


Figure 1. The pixel (enclosed by the dotted line) and the calibration source.

3. Pixel Implementation

The current source designated as I_{cal} in figure 1 is implemented using switches and capacitors. This is preferred because a very good reproducibility can be achieved among columns. This implementation is shown figure 2 where for simplicity only one pixel is drawn. The calibration source consisting of a capacitor C_{cal} and a transistor M_{cal} used as a switch, is common for each column of pixels.

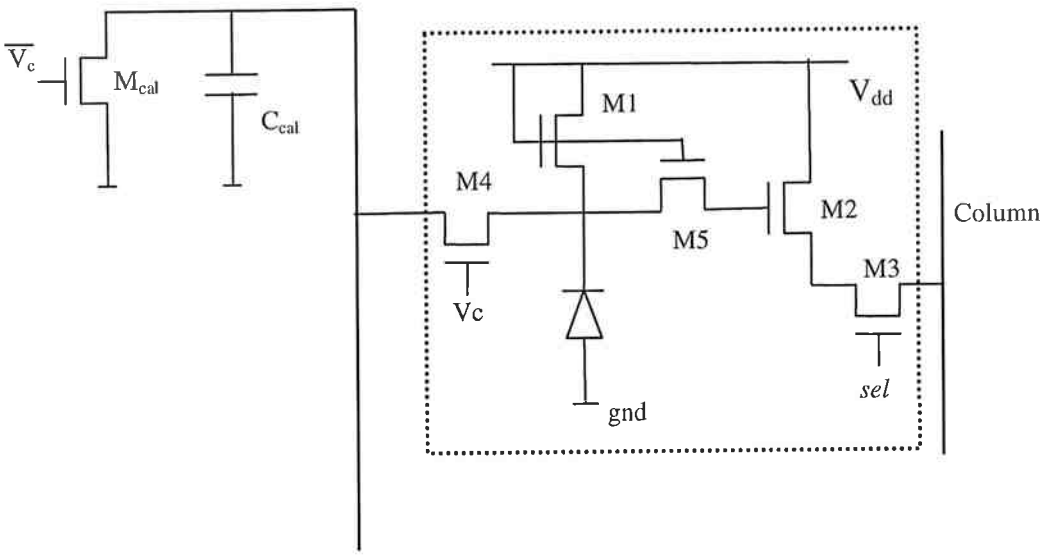


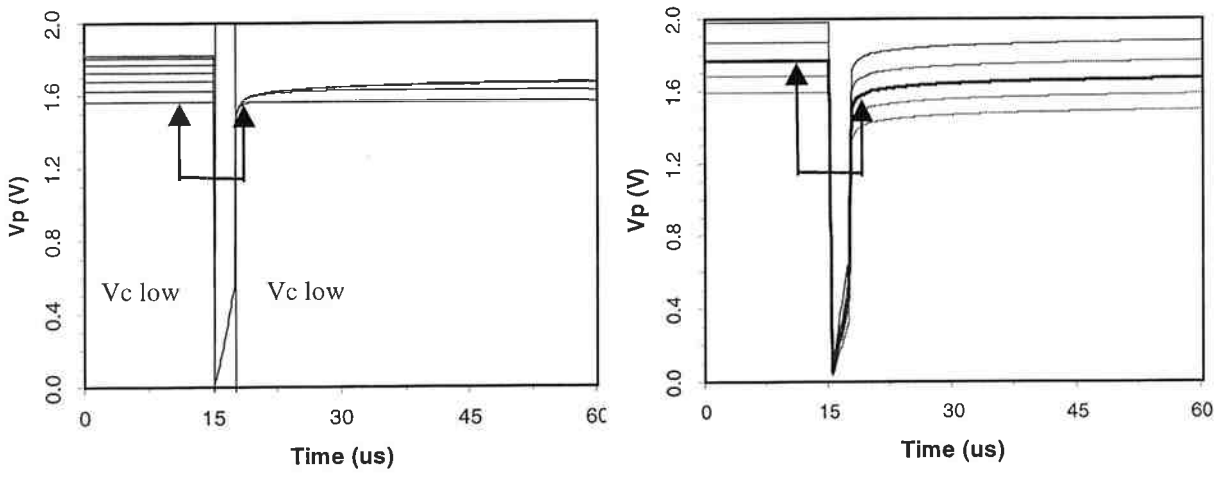
Figure 2. The calibration source together with one pixel.

Based on this pixel a sensor is designed using a CMOS technology with a minimum feature size of 0.5μm. This sensor employs a 525×525 pixel array with pixel dimensions 10μm×7.5μm. In the following paragraph simulation results are presented.

4. Pixel Simulations.

The pixel response is studied by means of circuit simulation. Parameters used in the simulations like spectral response, fill factor, dark current and pixel capacitance are measured directly from especially designed pixels.

Figure 3a shows the voltage at the pixel output before, during and right after the calibration pulse V_c for seven different photocurrents corresponding to a range of seven decades of light intensity. Pixels are biased with 20μA current.



(a) (b)

Figure 3. a) Pixel output during the calibration process for photocurrents corresponding to seven decades of light intensity. b) Monte Carlo analysis result of the pixel output during the calibration process when transistor parameters are varied between their corner values. The thick line corresponds to the typical values. Calibartion capacitance C_{cal} is 1pF. The arrows indicate the sampling points.

In this simulation for the first 15μs the pixel output is determined from the photocurrent exhibiting a sensitivity of approximately 60mV per decade of light intensity. However, for very low light levels the effect of the dark current is a decrease in sensitivity as shown in the figure. This decrease is somehow exaggerated due to the transistor models used in this simulation. Right after, the calibration pulse V_c goes high forcing pixel output to zero voltage. The photocurrent charges the calibration capacitance C_{cal} until V_c goes low again. Then, pixel voltage returns to it's value before the application of the calibration pulse with a time constant determined by the pixel capacitance and the transconductunce of the biasing transistor M1. This transistor is biased in the weak inversion region, therefore its transconductance is proportional to the photocurrent. In the sensor under examination this time constant for the medium light levels is in the order of a few ms. A very important observation must be pointed out here. For some microseconds right after the instant that V_c goes low the pixel output is independent of the light level. Therefore, the above scheme is effectively identical to the calibration with the current source shown in figure 1. The readout sequence is accomplished in two phases. First, before the application of the calibration pulse the pixel output is sampled and stored. Then, the calibration pulse is applied and a few microseconds later the pixel output is again sampled and stored. The difference between these two stored values depends on the photocurrent and is free from offsets imposed by variations in pixel transistors parameters.

This can be confirmed by means of circuit simulation. Figure 3b shows results from a Monte Carlo analysis when transistor parameters are varied between their corner values.

Clearly, pixel output varies considerably but the difference between the two pixel levels, before and right after the calibration pulse, is constant.

5. Discussion

A pixel structure for a CMOS image sensor with logarithmic response has been proposed. The main feature of a sensor based on this pixel is the low Fixed Pattern Noise due to pixel non-uniformities. This is achieved through on-chip pixel calibration at the expense of an extra transistor on each pixel. The calibration process is performed by applying a pulse on each line of pixels, right after the line selection. Thus, two signals per pixel have to be sampled and stored. Then, their difference has to be calculated.

A sensor based on this pixel has been designed. In this sensor a low FPN is expected not only due to the pixel architecture, but also due to the proper design of the column amplifiers. Indeed, the non-uniform response of the column amplifiers could cancel to a great extend the benefit of the pixel calibration. In this design a column amplifier has been used that is capable of performing the tasks described above without the introduction of offsets.

In this paper the pixel structure has been introduced and assessed by means of circuit simulations. In a future communication the full sensor design will be presented together with the complete characterization.

6. References

[1]. "Active Pixel CMOS Image Sensor with On-Chip Non-Uniformity Correction", N. Ricquier and B. Dierickx, 1995 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors", Dana Point, USA, April 20-22, 1995

[2] "A CMOS Image Sensor with Local Brightness Adaption and High Intrascene Dynamic Range", R. Hauschild, M. Hillebrand, B.J. Hotsicka, J. Huppertz, T. Kneip and M. Schwartz, ESSIRC 1998, p. 308.