P1 A Digital Pixel Image Sensor with 1-bit ADC and 8-bit Pulse Counter in each Pixel

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Abstract

We experimentally fabricated an 8-bit full-digital image sensor in which the signals generated in each pixel are directly converted from analog to digital within the each pixel and then output as 8-bit digital signals. Each pixel consists of a photodiode (PD), a 1-bit A/D converter(ADC) and an 8-bit pulse counter; it is an imaging device which includes a digital accumulation section (Figs. 1 and 2). The number of pulses accumulated during a field period in each pixel is read as parallel digital signals by means of XY addresses.

Because the signal is converted from analog to digital in each pixel, (1) the penetration of noise into the signal during signal readout can be suppressed, (2) a broad dynamic range of signals can be obtained at a low operating voltage and (3) signal processing can be carried out efficiently within the imaging device.

When the level of signal charges accumulated in the PD reaches the threshold, one pulse is generated in the 1-bit ADC and sent to the counter. Simultaneously, the PD is reset to the state of the initial condition, and accumulation of signal charges restarts. By repeating this series of operations for a certain period of time (one field period) automatically, the number of pulses generated during the period is counted. Furthermore, to accommodate inputs which exceed the maximum incident light intensity limited by the counter bit numbers, intrapixel signal processing (knee control) which controls the pulse generation rate of the 1-bit ADC is achieved using the output of the 8th bit.

The device is designed using the 0.35μm CMOS design rule (Fig. 3). The dimensions of each pixel are 50x50μm^2; the area of the PD within the pixel is 13.7μm^2, and the number of pixels is 64x64. The clock rate is 14.3 MHz, the frame rate is 60 Hz, and the device operates by means of a standard TV system. The 8-bit output signals are D/A converted and 2-D real-time images are obtained (Fig. 4).

The result of evaluating the 1-bit ADC, with respect to a unit pixel, showed that the output pulse number was linearly proportional to the number of incident photons in the range of 6×10^3/sec to 2.2×10^9/sec when the operating voltage was 1.3 V, and a dynamic range of approximately 110 dB was obtained (Fig. 5). The number of incident photons required to generate one pulse from the 1-bit ADC was approximately 1000~3000; this number can be controlled by adjusting the voltage setting. The minimum detectable voltage was 10 mV.

With intrapixel signal processing as shown in Fig. 6, when the output from the 8th bit increases to "high", the rate of generated pulses from 1-bit ADC decreases, even if the same amount of incident light is received, thus slowing the operating speed of the counter; in this way we confirmed that the knee control operates effectively.

In the experimentally fabricated device, high levels of random noise and fixed-pattern noise were observed. In particular, the random noise was caused by the erroneous operation of the counter and the unstable reset operation. These problems, however, can be reduced in the future through the optimization of the circuit and layout designs.

References

(1) Patent: "Solid-State Image Sensor" PTC/JP85/00710 or PTC/USA/1986-900,139

(2) K. Tanaka, F. Andoh, K. Taketoshi, I. Ohishi, G. Asari, "Novel Digital Photosensor Cell in GaAs IC Using Conversion of Light Intensity to Pulse Frequency" JJAP, Vol. 32(1993), pp. 5002-5007, Part 1, No. 11A, November 1993

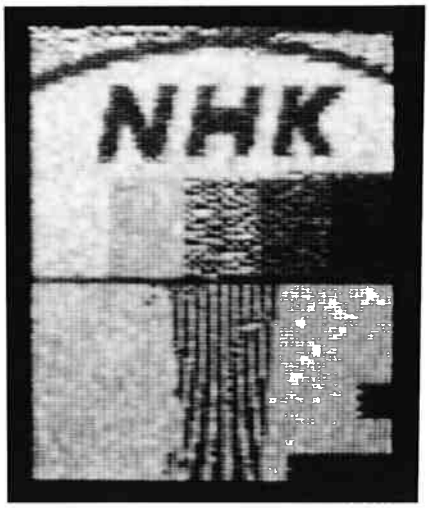

Figure 4 A reproduced image from a device.

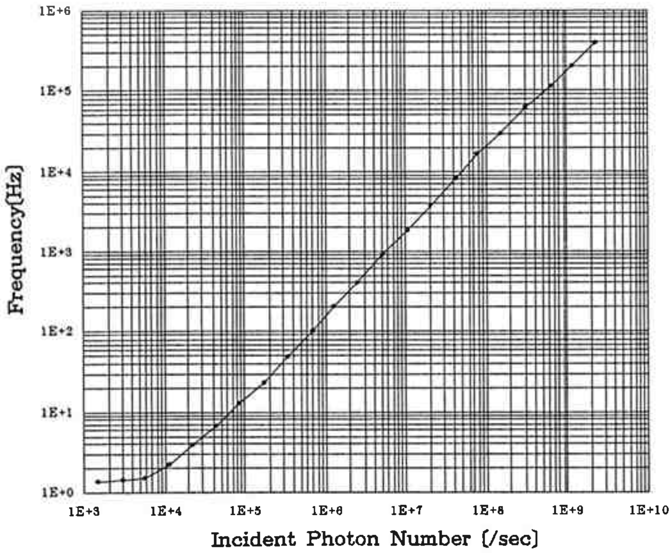

Figure 5 Photoelectric conversion characteristics of a 1-bit A/D converter.

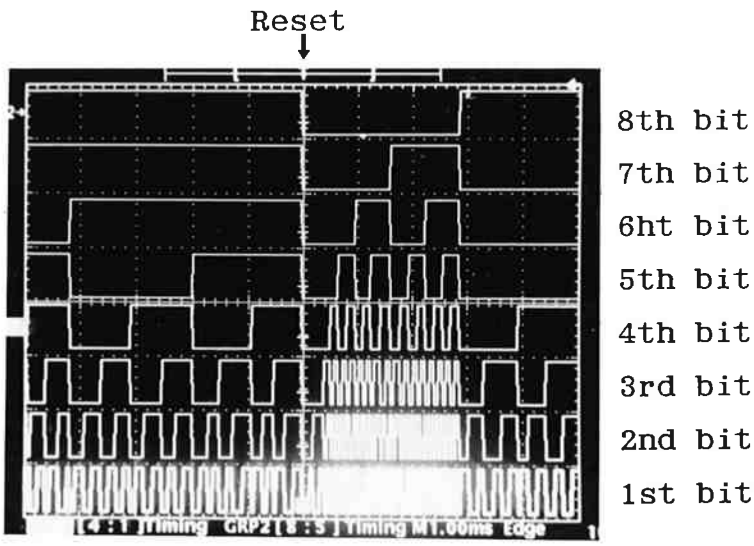

Figure 6 8 bit digital output operated with knee circuit.

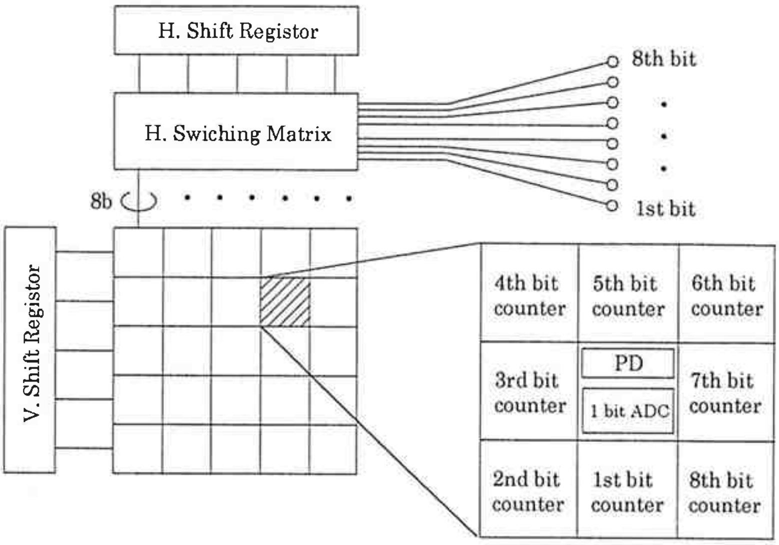

Figure 1. Schematic diagram of a 64x64 image sensor.

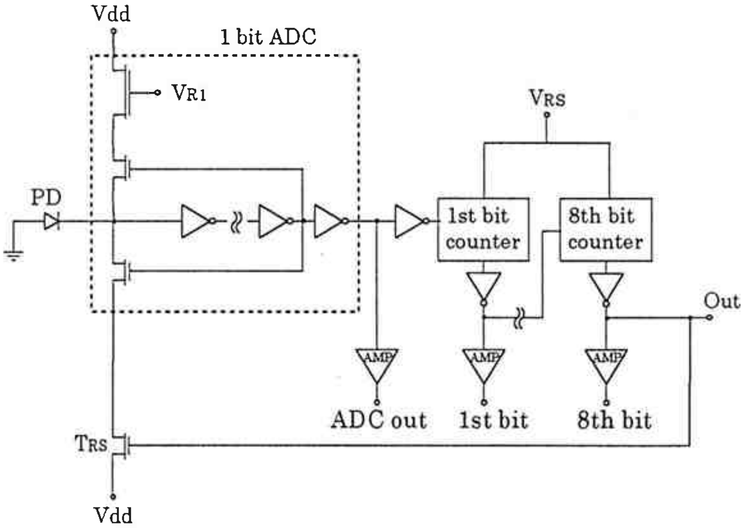

Figure 2 Circuit diagram of a pixel.

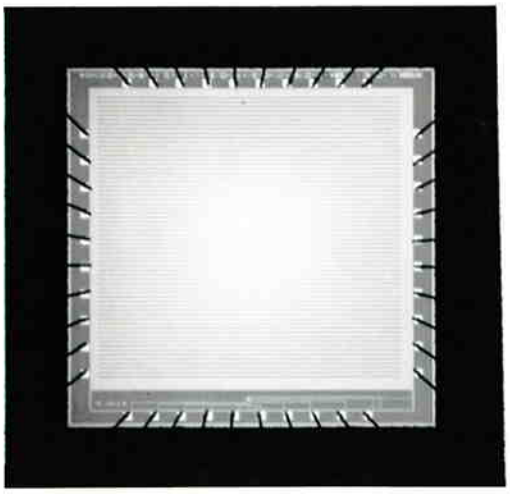

Figure 3 Photograph of a chip.