

Low dark current pinned photo-diode for CMOS image sensor

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Abstract

We have developed CMOS image sensor which has high sensitivity comparable to CCD imagers by realizing a very low leakage photo-diode. A low dark current of $0.1\text{nA}/\text{cm}^2$ in $5.6\text{ }\mu\text{m}^2$ pixel has been achieved by a pinned photo-diode structure and a sensor-specified process for a 1/4-inch 330 K pixel CMOS image sensor. The noise floor of the imager has also been reduced by an appropriate circuit design in the readout path.

Introduction

CMOS image sensor applications are thought to be limited to low-end camera use although its low cost, low power, and on-chip functionality.[1] It is because that CMOS imagers had low sensitivity mainly caused by their large photo-diode leakage current. The photo-diode leakage current origins were the surface damage and the dislocations and defects near LOCOS(LOCAl Oxidation of Silicon) as shown in Fig.1(a). The newly developed pinned photo-diode structure, as shown in Fig.1(b), with a sensor-specified process has drastically reduced the leakage current.

Low dark current for the pixel structure and the processes

CMOS sensor adopts LOCOS for an isolation in pixel which is compatible to standard CMOS process. LOCOS process induces very large stress in the photo-diode and causes the dislocation along the LOCOS. The SEM photograph of pixel in Fig.2(a) shows large etch pits with the conventional process. We have refined our process and added some modification to relieve the stress of LOCOS and other damages. The dislocations in pixel has been disappeared with the modified process as shown in Fig.2(b). The modified process has also reduced the dark current as low as $0.3\text{nA}/\text{cm}^2$ with the conventional photo-diode structure. It is a third of that with the conventional process as shown in Fig.3.

The surface area depletion generates a large dark current because of the surface defect states. The pinned PD has an additionally shallow p+ layer on the deep n-PD diffusion layer.[2][3] The pinned photo-diode structure shields the surface area by the p+ layer. This structure has been built in $5.6\text{ }\mu\text{m}^2$ pixel with using $0.6\text{ }\mu\text{m}$ design rule and the modified

process described above. The dark current has been reduced to the extremely low level of 0.1nA/cm^2 , which is comparable to CCDs' level as shown in Fig.3. Figure 4 shows the reproduced image in the dark for the different processes and structures.

Low dark current for the circuit

All the noises in the readout path has also been successfully suppressed below the CCD sensors' level by the appropriate circuit design. Figure 5 shows the sensor architecture. The noise cancel circuit functions as an off-set cancel of pixel amplifier[5], and a signal charge amplifier. The sufficient large charge gain in the noise cancel circuit enables the noises in the readout path to be below the detection limit. The pixel amplifier has the same noise spectrum as that of CCDs' charge detector in principle. However, the pixel amplifier is operated in column-parallel. The amplifier noise is smaller than that of the CCDs because of its narrower bandwidth. Therefore, we have gotten high sensitivity and high quality image equal to CCD image sensor.

Conclusion

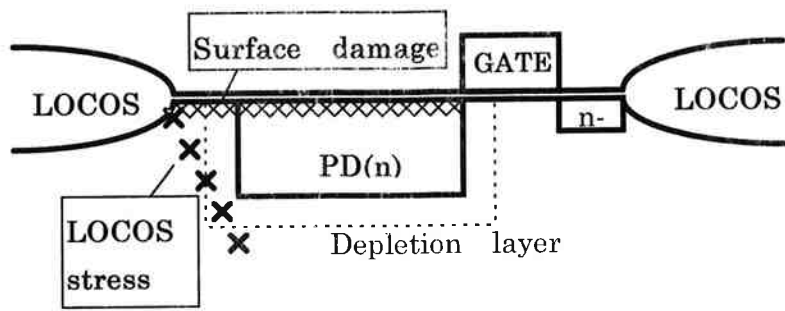
In conclusion, the low dark current of the pinned photo-diode has been developed for the CMOS image sensor using a modified process. The characteristics of pinned photo-diode and the conventional image sensor are summarized in Table I . As a result, a CMOS image sensor has been realized high sensitivity and high quality to compared with CCD image sensor.

Reference

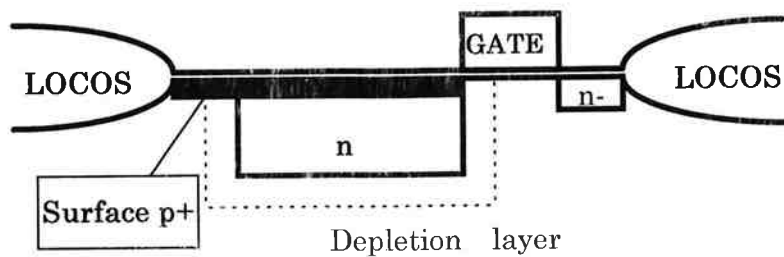
- [1]E.R.Fossum, IEDM. Tech. Dig., p17, 1995
- [2]Teranishi, et al., IEDM. Tech. Dig., p324, 1982
- [3]B.C.Burkey, et al., IEDM. p28, 1984
- [4]R.M.Guidash, et al., IEDM. Tech. Dig., p927, 1997
- [5]Y.Matsunaga, et al.,ITE Technical Report Vol.22, No.3, p7, IPU'98-2 ,Jan, 1998 (in Japanese)

	Conventional photo-diode	Pinned photo-diode
Pixel size	$5.6 \times 5.6 \mu\text{m}^2$	$5.6 \times 5.6 \mu\text{m}^2$
Design rules	$0.6 \mu\text{m}$	$0.6 \mu\text{m}$
Saturation current	45 nA	45 nA
Dark Current at RT	0.3 nA/cm^2	0.1 nA/cm^2
FPN(leak current at RT)	$9 \text{ pA}_{\text{p-p}}$	$3 \text{ pA}_{\text{p-p}}$
Frame rate	30 Hz	30 Hz
Power supply	3.3 V	3.3 V
Power dissipation	30 mW	30 mW

Table I Characteristic of 1/4-inch 330 K pixel CMOS image sensor.



(a)Conventional Photo-Diode



(b)Pinned photo-diode with modified process

Figure 1. Cross-sections of the photo-diodes

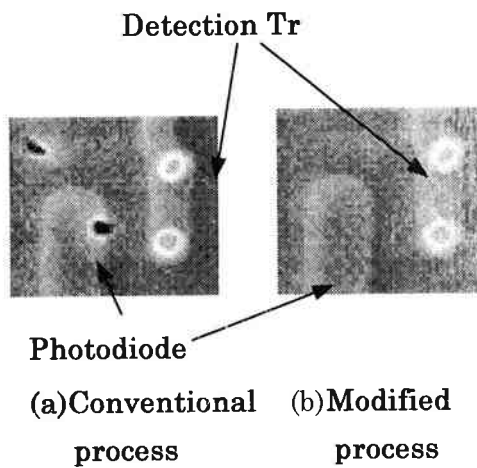


Figure 2 . Etch pit of defect

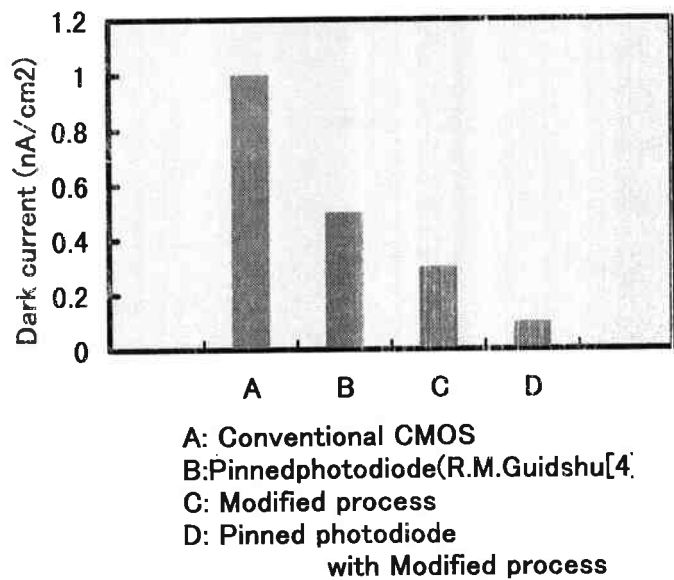
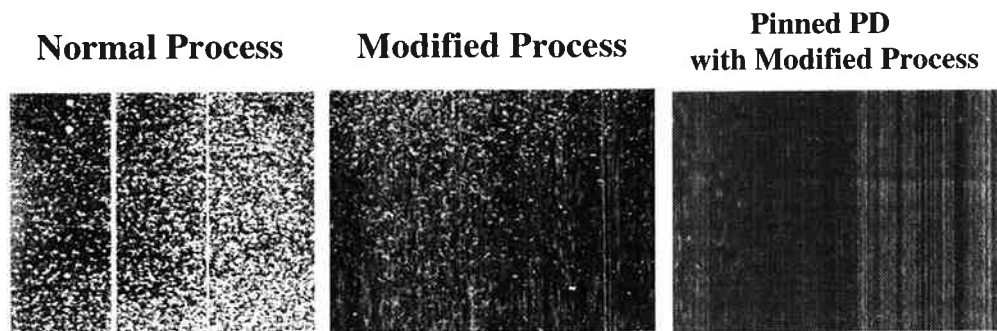


Figure.3 Dark current of the photo-diodes



($0.6\mu\text{m}$ CMOS Process, 60°C , $T_{\text{int}}=1/60\text{s}$)

Figure 4. Reproduced Images under dark conditions

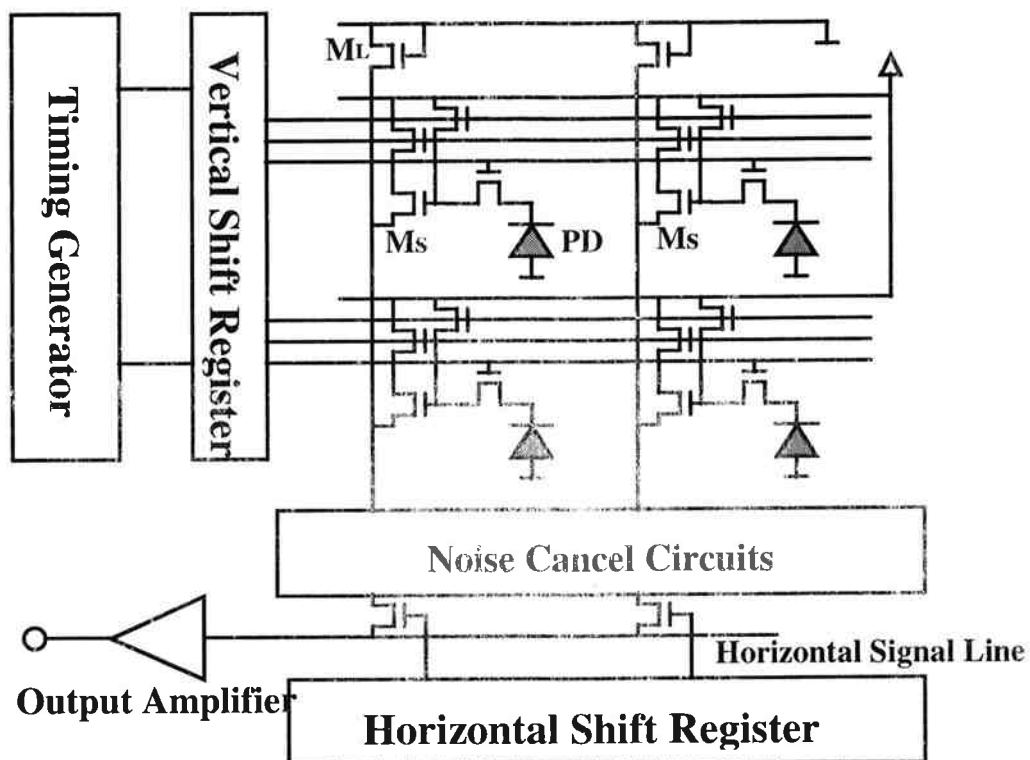


Figure 5. CMOS Sensor Circuit Diagram