

R1 A 2/3-in. 2,200k-pixel FIT-CCD for DTV 1080i

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Abstract

A 2,200k-pixel FIT-CCD image sensor supporting DTV 1080i format has been developed. The frame shift frequency of the device is 1.86 MHz which is about three times higher than conventional Hi-Vision CCDs. Despite the extremely high frame shift frequency, saturation output is larger than the conventional Hi-Vision CCDs by adopting newly-developed three-layer metal wiring structure and thin gate oxide.

1. Introduction

In the professional broadcast camera market, new camera development has been stepped up due to the imminent start of DTV broadcasting. Among the various standards proposed for DTV broadcasting, the 1080i format has the most likely prospect of being adopted as HDTV format by most broadcasting stations. Conventional 2/3-in. Hi-Vision FIT-CCDs with 1,035 vertical lines and a vertical transfer frequency of 714 kHz are not able to support 1080i format cameras, which require 1,080 vertical lines and a frame shift frequency of 1.86 MHz. There has therefore been strong demand for CCDs with a higher frame shift frequency to support for 1080i format cameras.

2. Device structure

Figure 1 shows the schematic diagram of the device. The total valid square pixels are arranged as 1,936(horizontal) x 1,086(vertical), achieving a 16-to-9 aspect ratio. The pixel size is 5.0 μm square. Thin gate oxide, optimized ion implantation and low temperature process technology are used to prevent the pixel performance degradation, such as reduction of sensitivity and dynamic range, which often accompanies high integration.

3. High Speed Vertical CCD (V-CCD) Operation

The higher the vertical transfer frequency is, the larger the voltage drops of the vertical transfer clock signal in the image area, resulting in reduced saturation output voltage and transfer efficiency. The frame shift frequency of conventional Hi-Vision CCDs is 714 kHz, whereas 1.86 MHz is required for CCDs to support the 1080i standard. In this device, we adopt newly-developed three-layer metal wiring structure to minimize the voltage drops of the vertical transfer clock signal. From our simulation results using our standard process parameters, it is obvious that shunting V-CCD gate by Al wire and reducing the resistance of vertical clock bus-lines are effective to improve the saturation output and transfer efficiency at 1.86MHz V-CCD driving. We developed new wiring layout and pixel structure from these results. Figure 2 shows an overview of the wiring layout of the device. Metal1, metal2 and metal3 are formed by WSi (400 nm), AL (500 nm) and AL (900 nm) respectively. Figure 3 shows the horizontal cross-sectional view of new pixel structure. Figure 4 shows pixel layout of newly developed structure. In these structure, Metal1 and metal2 are used for not only shunt line but also photoshield in image area. Metal1 has low reflection characteristic which is suitable for photoshield around photodiodes. On the other hand, metal2 has lower transparency than metal1, so it suppresses high incident

light transmitting to V-CCD through the photoshield formed by Metal1. Metal3 is used for vertical clock bus-line and photoshield in storage area, optical black area and horizontal CCD (H-CCD). As shown in Figure 3 and 4, metal1 connects to poly-Si gate electrodes and metal2 connects metal1. This structure reduces the voltage drops of the vertical transfer clock signal in the image area because of low resistance of metal2. Moreover, vertical clock bus-lines formed by thick Al layer can transmit vertical transfer clock signal to the image area without voltage drops.

As a result, three-layer metal wiring structure prevents the saturation output and the transfer efficiency from degrading at the vertical transfer frequency of 1.86 MHz.

4.Low Driving Voltage and High Speed Operation of 1-ch H-CCD

By adopting a 1-ch high-speed horizontal CCD with the transfer frequency of 74 MHz, the fixed pattern noise due to 2-ch output system has been completely eliminated. It is another remarkable advantage of 1-ch output system that a strong low-pass filter at 37 MHz which is indispensable in 2-ch output system and causes serious decrease of the MTF under 30MHz(bandwidth of 1080i format) is not needed. Moreover, we have achieved a very low driving voltage of 3V in H-CCD at 74MHz by forming deep and low dose P-well.

5.Device Characteristics

Table 1 summarizes the characteristics of the device. Saturation output voltage is 800mV. Adopting thin gate oxide and three-layer metal wiring structure, maximum charges handling capability of V-CCDs is increased by 30%. To achieve the driving voltage of 3V in H-CCDs can suppress increase of the power consumption caused by adopting thin gate oxide and reduce power consumption by 20%. Smear level is -120dB. Furthermore, a 20% sensitivity improvement was obtained by forming an anti-reflection film [1] over the photodiode.

6.Conclusion

A 2/3-inch 2,200k-pixel FIT-CCD supporting for 1080i format cameras has been successfully developed. The device has excellent characteristics such as high sensitivity, low smear, large saturation voltage and high S/N ratio.

7.Acknowledgement

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8.References

[1] I.Murakami et al., "New Technologies of Photo-Sensitivity Improvement and VOD Shutter-Voltage Reduction for CCD Image Sensors", ITE Technical Report, Vol.23, No.30, PP.1-6, 1999.

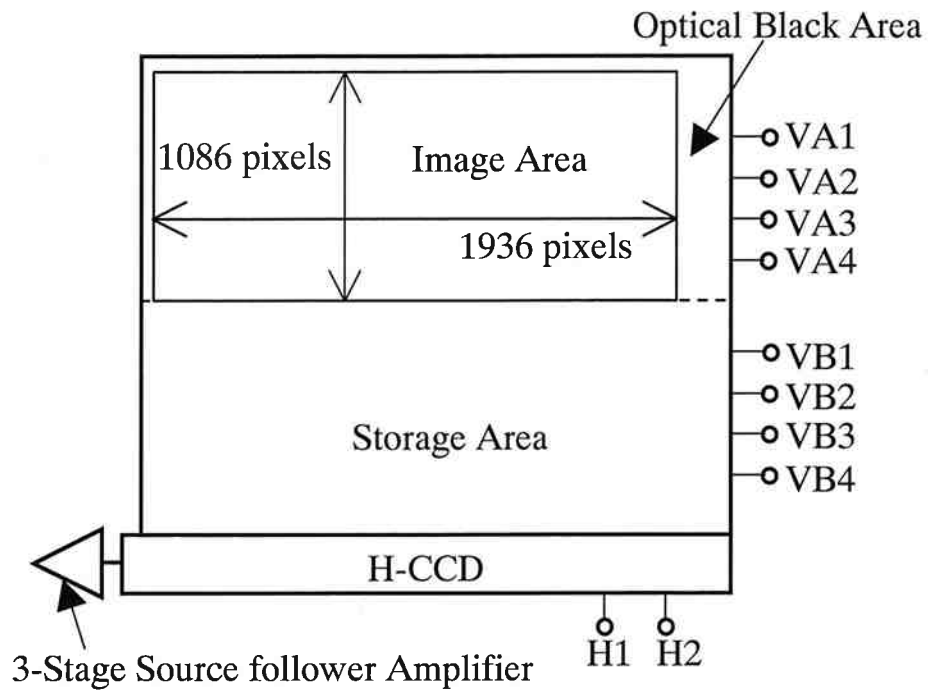


Figure 1. Schematic diagram of the device

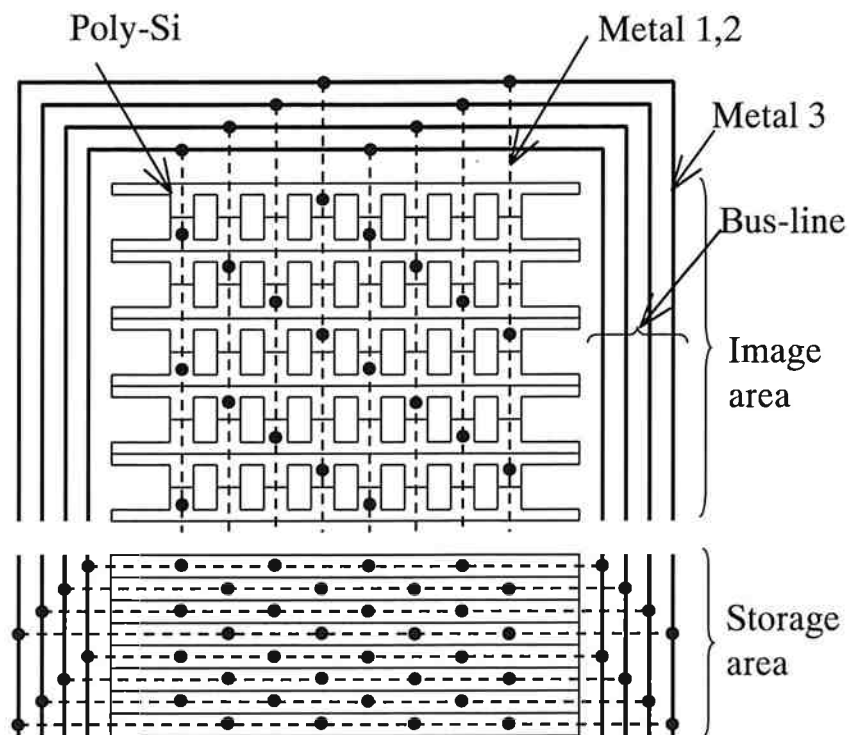


Figure 2. An overview of the wiring layout of the device

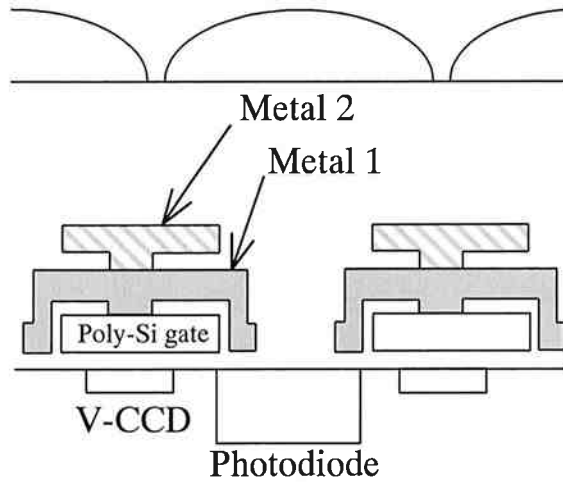


Figure 3. Horizontal cross sectional view of new pixel structure

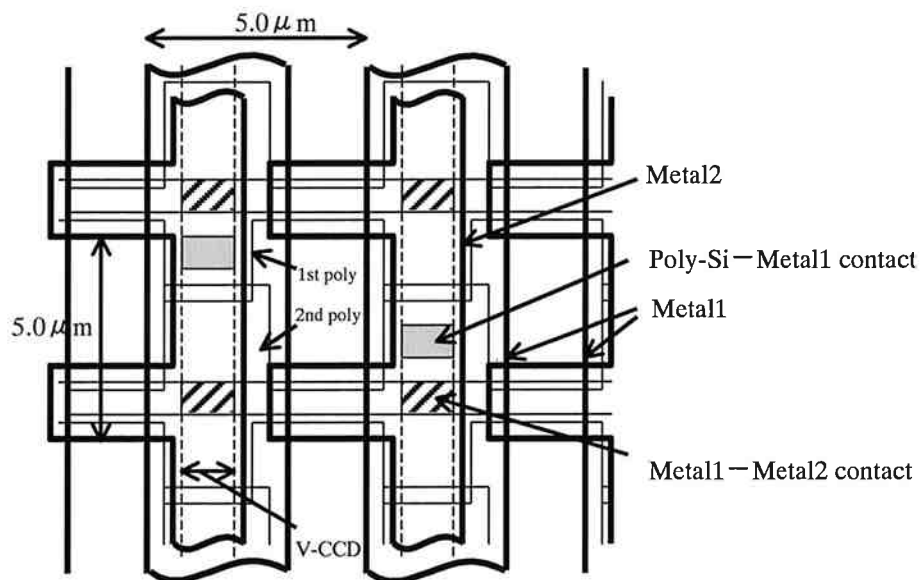


Figure 4. Pixel layout of newly developed structure

Table 1. Device Characteristics

Optical Format	2/3-inch
Effective Pixels	1936(H) × 1086(V)
Pixels Size	5.0(H) μm × 5.0(V) μm
HCCD driving Frequency	74MHz
HCCD driving Voltage	3.0V
Sensitivity	130mV
Saturation Voltage	800mV
Smear (V/10)	-120dB