

## Pixel Parallel and Column Parallel Architectures and their Implementations of On Sensor Image Compression

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### Abstract

We propose a novel integration of compression and sensing in order to augment performance of the image sensor. By integrating compression function onto the sensor focal plane, the image signal that has to be readout from the sensor is significantly reduced. The integration can consequently results in the increasing the pixel rate of the sensor. Thus, the proposed sensors can be potentially applied to high pixel rate imaging such as high resolution image sensing and high frame rate image sensing.

The compression scheme we make use of is conditional replenishment that detects and encodes moving areas. The compression scheme is illustrated in fig.1. In this paper, we introduce design and implementation of two architectures for on sensor compression; one is pixel parallel approach and the other is column parallel approach (fig.2). The former approach is advantageous to higher rate of the processing, and the latter approach is advantageous to higher fill factor of the implementation.

We have designed and prototyped VLSI chips of the proposed sensors based on the both pixel parallel and column parallel architectures (fig.3-7). Some parameters of the prototype are shown in table.1. The detail of the design and the results of the experiments obtained by the prototype chips will be presented in the workshop.

Different from our previous implementation that we presented in the last CCD/AIS, the new prototype of pixel parallel architecture is re-designed and it has complete functions required for compression including global rate control, smart scanning. The column parallel architecture is completely new.

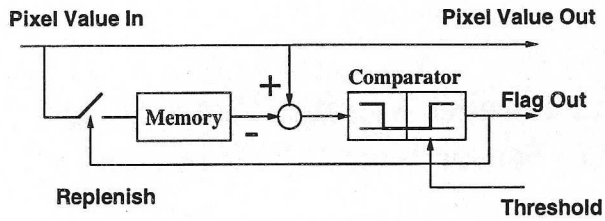


Figure 1. Description of coding algorithm in each pixel by conditional replenishment

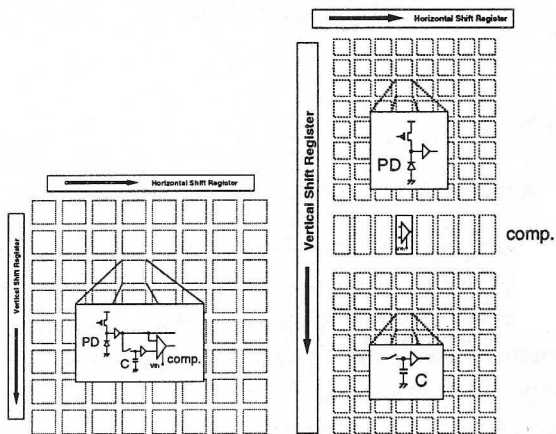


Figure 2. Illustrations of pixel parallel architecture (left) and column parallel architecture (right)

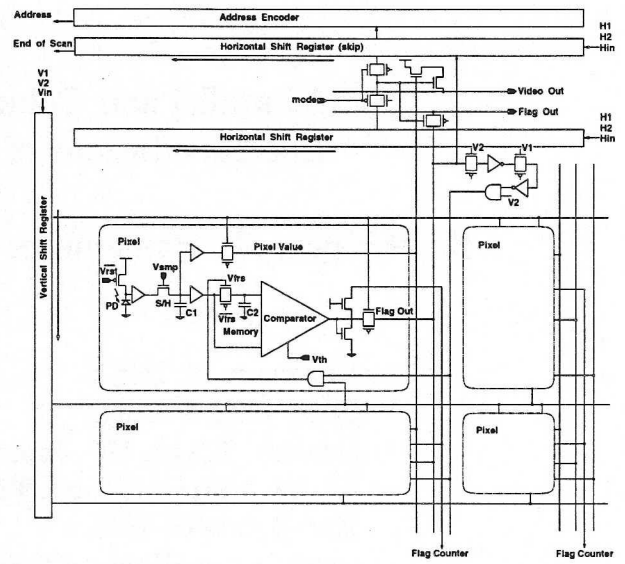


Figure 3. Design of on sensor compression chip by pixel parallel architecture

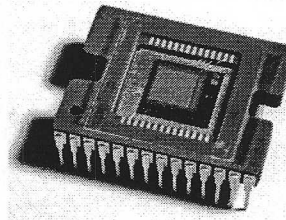


Figure 4. A prototype chip of the pixel parallel compression sensor

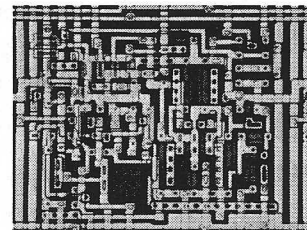


Figure 5. A single pixel of the pixel parallel compression sensor

Table 1. Comparison between Pixel Parallel Architecture (PPA) and Column Parallel Architecture (CPA).

	PPA	CPA
number of pixels	32 × 32	32 × 32
die size	6.7 × 6.4 mm <sup>2</sup>	3.6 × 6.4 mm <sup>2</sup>
pixel size	160 × 160 μm <sup>2</sup>	transducer : 60 × 60 μm <sup>2</sup> /pixel memory : 60 × 65 μm <sup>2</sup> /pixel processing : 60 × 244 μm <sup>2</sup> /column
number of transistor	33 trs. / pixel	transducer : 3 trs. / pixel memory : 10 trs. / pixel processing : 41 trs. / column
fill factor	1.9%	38.5%
power dissipation	0.15mW / pixel	1.5mW / column

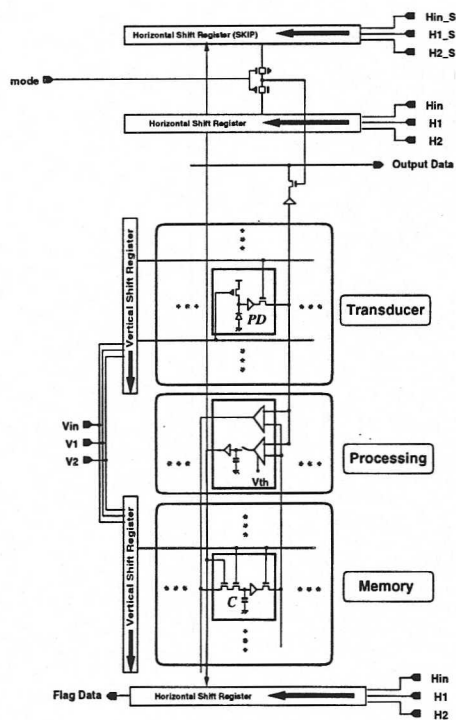


Figure 6. A description of the design of column parallel architecture

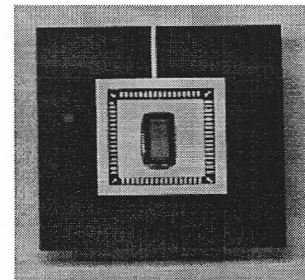


Figure 7. A prototype chip of the column parallel compression sensor

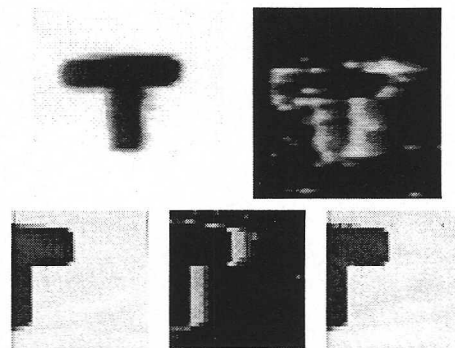


Figure 8. Results obtained by the prototypes for the experimental scene that "T" moves horizontally. (Top) Image and flag by the prototype of pixel parallel architecture, (Bottom) Image, flag and reconstruction obtained by the prototype chip based on column parallel architecture