Comparison of CCD and CMOS Pixels for a Wide Dynamic Range Area Imager

Steven Decker and Charles G. Sodini
MIT Department of Electrical Engineering and Computer Science
Cambridge, MA 02139

1 Introduction

CCD and CMOS designs for a wide dynamic range area imager are compared. Specifications include a 256×256 array, 1000 frames/sec operation, and 10-b column-parallel output with on-chip A/D conversion. One potential application for the imager is as a front end for a stereo vision system for automobiles, where wide dynamic range is required due to the uncontrolled lighting conditions.

1.1 Wide Dynamic Range Technique

Brightness adaptation is provided by a lateral overflow gate, using a technique described by Knight[1] and Sayag[2]. The voltage applied to the overflow gate changes over the integration period, changing the height of the potential barrier to charge flow. At each point in time, photogenerated charge in excess of the limit imposed by the barrier immediately flows over the barrier into a charge sink. Figure 1 shows a sample compression curve $b(t)$ expressed in terms of integrated maximum stored charge. A charge integration curve $q(t)$ shows linear integration for $0 \leq t < t_i$, barrier limited integration for $t_i \leq t < t_d$, and free integration for $t_d \leq t \leq T$. For any I, the charge $Q(I)$ can be separated into a barrier limited component Q_{bl} and a freely integrated component Q_{free}. The corresponding calibration curve $Q(I)$ is shown in Figure 2.

1.2 Design and Operation of CCD, CMOS imagers

Interline transfer (ILT) and frame interline transfer (FIT) formats are logical choices for the wide dynamic range area CCD imager. This pixel is shown in cross-section in Figure 3. The imager is operated in the usual manner, except that the potential on the lateral overflow gate is varied over the integration period to implement the wide dynamic range algorithm.

The CMOS pixels are implemented in a single poly process. The imaging element is an n^+ - p photodiode. The photodiode has superior responsivity, especially in the short wavelengths. A storage region, which is inherent in the CCD pixel, is optional in a CMOS pixel. If it is used, it allows all rows to use the same overflow gate waveform. Otherwise, the overflow gate waveforms must be staggered in time.

The charge readout pixel is shown with a photodiode and storage region in Figure 4. At the end of the integration period, the storage gate goes high to share charge between the photodiode and the storage diffusion. When the pixel is read out, the row select gate goes high, allowing charge to flow onto the column line. The output circuit holds the column line at virtual ground by integrating the charge onto the feedback capacitor C_{fb}. The equivalent circuit is shown in Figure 6a. The CCD pixel uses the same output circuit to convert charge to voltage.

The voltage readout pixel with a photodiode imaging element and without a storage region is shown in Figure 5. The row select signal is timed so that the source follower device in each row is connected to the column line at the end of the integration period. A current source in the output circuit biases the source follower. The equivalent circuit is shown in Figure 6b.

Correlated double sampling (CDS) can be used to reduce offsets and low frequency noise. The use of CDS to remove reset noise in the output diffusion of a CCD imager is well known, but CDS can also be used to eliminate offset in the threshold voltage of the lateral overflow gate by applying a known potential to the gate, performing a fill-and-spill operation with the drain diffusion, and reading out the generated charge packet. Associated problems are the need for extra area in the shift register to store the second packet,

increased shot noise, and the fact that it effectively *adds* an offset when $I < I_{min}$. CDS can be applied to the charge readout pixel in a similar fashion. In the voltage readout pixel, CDS is performed by taking the difference between samples taken at the end of the integration period and after the barrier is lowered to reset the pixel, thereby eliminating the problems discussed above.

2 Performance Measures

In this section, each pixel is evaluated for fundamental device noise, mismatch, fill factor, lag, and crosstalk.

Noise or mismatch can be expressed in terms of a charge-referred error $Q_{n,m}$. The contributions of individual noise and mismatch sources are assumed to be caused by independent, Gaussian distributed processes so that total noise or mismatch is the square root of a sum of squares of individual noises or mismatches. In general, $Q_{n,m}$ depends on both I and the calibration curve $Q(I)$.

Photonic shot noise is caused by the random arrival times of photons, and is intrinsic to all pixels. The associated noise is $Q_{n,phot} = \sqrt{qQ_{free}}$. The noise associated with the barrier limited portion of the charge, $Q_{n,bl}$, can be thought of as the filtering of photonic shot noise with the lowpass filter formed by the photoactive area capacitance and the transconductance of the lateral overflow gate. This situation is similar to the transfer noise in a bucket brigade device [3], and is $Q_{n,bl} = (n/2)\sqrt{kTC}$, where n is the subthreshold nonideality parameter. The noise added by charge transfer depends on whether the transfer is complete. For complete transfer processes, as in the CCD shift register, a fraction ϵ of the charge $Q(I)$ is left behind on each transfer. The noise process on this residual packet is Poisson, and the noise involved in N_{trans} transfers is $Q_{n,trans} = \sqrt{qN_{trans}\epsilon Q(I)}$. In a basic CMOS process, complete charge transfer is difficult to implement. Transfer is usually accompanied by charge sharing between the source and drain diffusions of an MOS transistor, with an associated noise $Q_{n,trans} = \sqrt{kTC}$, where C is the series capacitance of the two diffusions. The conversion from charge to voltage involves MOS transistors, which have $1/f$ and thermal noise. CDS largely removes the $1/f$ noise, but increases the thermal noise. For the output circuit used with the charge readout and CCD pixels, charge referred MOS thermal noise is proportional to the capacitance at the inverting terminal [4]. With CDS, the op-amp thermal noise is

$$Q_{n,MOS} = (C_p + C_{fb})\sqrt{\frac{4}{3}\frac{kT}{\tau g_m}}, \tag{1}$$

where τ is the settling time constant of the circuit, g_m is the transconductance of the input stage of the op-amp, and C_p is the parasitic capacitance at the inverting terminal. For the CCD pixel, C_p is the small output diffusion capacitance. For the charge readout pixel, $C_p = C_{line}$, and is quite large.

Important mismatch sources include photoactive area capacitance mismatch, conversion capacitance mismatch, storage capacitance mismatch, threshold voltage mismatch in the lateral overflow gate, and source follower gain and offset mismatch.

A fractional mismatch $\delta_{c,pa}$ in the photoactive area capacitance produces an effective charge mismatch $Q_{m,c,pa} = Q'(I)I\delta_{c,pa} = Q_{free}\delta_{c,pa}$ in the voltage readout pixel, and an effective mismatch $Q_{m,c,pa} = Q_{bl}\delta_{c,pa}$ in the charge readout and CCD pixels.

The charge signal is converted to voltage by a conversion capacitance. This is the feedback capacitor C_{fb} for the charge readout and CCD pixels. A fractional mismatch $\delta_{c,fb}$ in this capacitance results in an effective charge mismatch $Q\delta_{c,fb}$. In the voltage readout pixel, there is no separate error term because the conversion capacitance is physically the same as the photoactive area capacitance.

Storage capacitance mismatch is important only when charge is shared between a photodiode and a storage diffusion in a CMOS pixel. The photodiode and storage diffusions have nominally equal capacitances with fractional mismatch $\delta_{c,sto}$. The resultant charge mismatch is $Q_{m,c,sto} = \frac{1}{2}\delta_{c,sto}Q$.

Threshold voltage mismatch $\Delta_{vt,log}$ in the lateral overflow gate device results in a charge mismatch $Q_{m,vt,log} = \Delta_{vt,log}C$, where C is the photoactive area capacitance at time t_d (see Figure 1). Note that this mismatch term exists for the CCD pixel only if the charge integration curve intersects the compression curve.

Gain mismatch error in the source follower of the voltage readout pixel produces a charge mismatch

$$Q_{m,sf} \approx \frac{1}{(g_m + g_{mb})r_o}\left(g_{mb}r_o\left(\frac{\Delta g_m}{g_m} + \frac{\Delta g_{mb}}{g_{mb}}\right) + \frac{\Delta\lambda}{\lambda}\right) \tag{2}$$

where λ is the channel length modulation parameter and g_m is the transconductance of the source follower device. Offset $\Delta_{vt,sf}$ in the threshold voltage of the source follower device causes a charge mismatch $Q_{m,vt,sf} = C\Delta_{vt,sf}$ if CDS is not used. The corresponding gain mismatch term for the charge readout and CCD pixels is insignificant because the gain of the output circuit depends only on C_{fb}. The corresponding threshold voltage offset term would be insignificant since CDS would be used in the output circuit.

Charge storage in the imaging array is the major limitation on fill factor. The storage region must have capacitance at least as great as the capacitance of the photoactive area, which puts a lower limit on the size of the charge storage regions. A CCD pixel with photogates can have a fill factor no higher than 33%, while a CMOS pixel with photogates and charge storage can have a fill factor no greater than 50%. The charge readout CMOS pixel of Figure 4 has no inherent fill factor limit, but maximum charge is transfered to the output circuit when the photodiode and storage diffusion have the same size, which gives a fill factor under 50%.

Image lag refers to the corruption of the present value of a pixel by its previous value. The cause is incomplete reset, which could occur because of charge trapping, subthreshold conduction in the reset device, or incomplete settling of the output circuit. The dominant source of lag is incomplete reset of photodiodes in those pixels which use them.

Crosstalk refers to the corruption of a pixel value by other pixel values or signals on the imager. Electrical crosstalk is important for CMOS pixels, while optical crosstalk is important for all pixels. Transfer crosstalk exists in the charge readout and CCD pixels.

Electrical crosstalk arises from two sources. A transient potential drop across the silicon between the output circuit and the photoactive area or storage area will cause an error in the measured charge or voltage. Such a potential drop can be caused by substrate currents induced by transient voltages on the other column lines. Simulation shows that crosstalk due to this effect is minimal. The other source of electrical crosstalk is wires, such as the row select and lateral overflow gate potential, which cross the column lines and have changing voltages during readout. The induced error depends on the line impedance. For the voltage readout pixel, the output impedance is a relatively low $1/g_m$, where g_m is the transconductance of the source follower device. The line impedance of the charge output pixel is high, so that during charge readout all other signals must be held constant. Even the row select line must return to its off potential during the readout of a charge packet.

Optical crosstalk is a serious concern because the wide dynamic range algorithm results in a degradation of the signal-to-crosstalk ratio. Depending on illumination, only a small fraction of the photogenerated charge might be retained as the signal, but crosstalk is proportional to the total number of photogenerated carriers. Crosstalk between photoactive areas is common to all pixels, and generally results in a small fractional increase in the apparent illumination. Crosstalk into a storage area is more serious because the crosstalk charge is unattenuated by compression. The effect can be thought of as adding a linear term to the calibration curve,.limiting the achievable compression ratio. Also, the effect is nonuniform, being more severe for the rows which are read out later. Crosstalk into the vertical shift register [5] is the dominant problem in the CCD imager. This form of crosstalk is particularly problematic since charge packets formed under low illumination may pass by regions of very high illumination.

Transfer crosstalk arises in signal transfer from the pixel to the output circuit. In the CCD imager, charge lost from a packet due to charge transfer inefficiency can enter subsequent packets. In a charge readout or voltage readout pixel, the voltage on the column line never completely settles, so each pixel's output value contains a remnant of the previous pixel value. Crosstalk is worse for images with high spatial frequncy content.

3 Conclusions

The noise and mismatch have been evaluated for CCD, charge readout CMOS and voltage readout CMOS. Plots of the signal-to-noise and mismatch are shown in Figures 7 and 8 assuming a $25\mu m \times 25\mu m$ pixel, using parameters for the $0.8\mu m$ HP n-well CMOS process offered through MOSIS, and the CCD/CMOS process at MIT [6]. A logarithmic compression function

$$Q(I) = Q_{max} \frac{\ln(1 + I/I_0)}{\ln(1 + I_{max}/I_0)} \tag{3}$$

is assumed. Table 1 shows a comparison of several imager parameters. The slope of the signal-to-noise ratio curve for the CCD pixel is only 10 dB/decade at low illumination because the dominant noise sources are transfer noise in the shift register and photonic noise, both of which have $\sqrt{N}$ dependencies.

Crosstalk is a major problem for both the CCD pixel and the charge readout pixel. Optical crosstalk is prohibitively high in the CCD's shift register and limits the achievable compression ratio in the charge readout pixel. Electrical crosstalk in the charge readout CMOS pixel significantly reduces the fill factor and doubles the required sampling rate of the A/D converters, which is unacceptable.

The voltage readout pixel is only minimally affected by optical and electrical crosstalk. No storage area is required, so the fill factor can be relatively high. CDS can be easily used to reduce the effect of offsets and low frequency noise. For these reasons, the voltage readout pixel is chosen as the best implementation for the wide dynamic range imager.

	Interline CCD	Charge Readout	Voltage Readout
random noise	photonic noise charge transfer inefficiency readout noise	photonic noise kTC charge sharing readout noise	photonic noise thermal, 1/f in SF device
mismatch	photoactive area cap output capacitance ΔV_T in barrier	photoactive area cap output capacitance ΔV_T in barrier PD, SD cap mismatch	photoactive area cap ΔV_T in barrier ΔV_T in source follower SF gain error
fill factor	$< 33\%$	$< 50\%$	no limit; 40% in sample layout
lag	none	incomplete PD reset	incomplete PD reset
optical crosstalk	adjacent pixels shift register	adjacent pixels storage diffusion	adjacent pixels
electrical crosstalk	none	high impedance column line	minimal

References

[1] Knight, T.F. "Design of an Integrated Optical Sensor with On-Chip Preprocessing," Ph.D. Thesis, MIT, 1983.

[2] Sayag, Michel. "Non-linear Photosite Response in CCD Imagers," U.S. Patent No. 5,055,667, October 1984.

[3] Buss, Dennis D., *et al.* "Noise in MOS Bucket Brigade Devices," *IEEE Transactions on Electron Devices*, Vol. ED-22, No. 11, November 1975, pp. 977-981.

[4] Stanton, J.C. "A Low Power Low Noise Amplifier for a 128 Channel Detector Read-Out Chip," *IEEE Transactions on Nuclear Science* Vol. 36, No. 1, February 1989, pp. 522-527.

[5] Lavine, James P. *et al.* "Monte Carlo Simulation of the Photoelectron Crosstalk in Silicon Imaging Devices," *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 10, October 1985, pp. 2087-2091.

[6] Keast, Craig L. "A CCD/CMOS Process for Integrated Image Acquisition and Early Vision Signal Processing," S.M. Thesis, Department of Electrical Engineering and Computer Science, MIT, September 1989.

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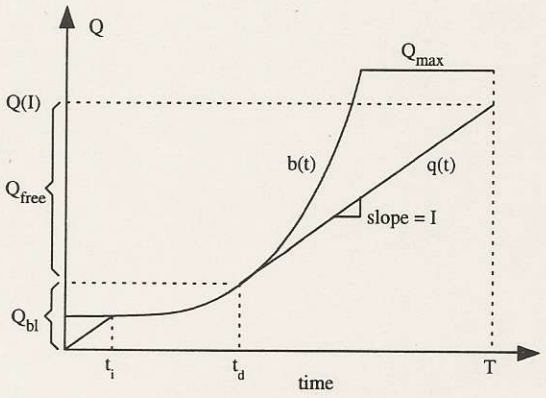

Figure 1: Sample compression curve and charge integration curve.

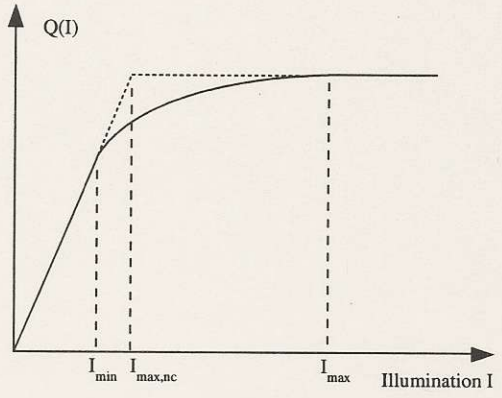

Figure 2: Charge calibration curve. $I_{max,nc}$ is the maximum detectable illumination for a noncompressive pixel.

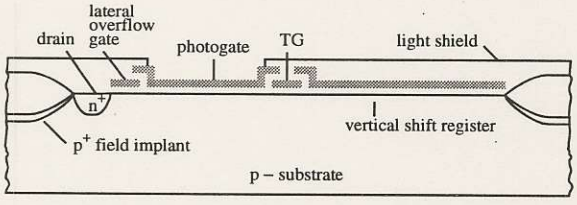

Figure 3: CCD pixel cross section.

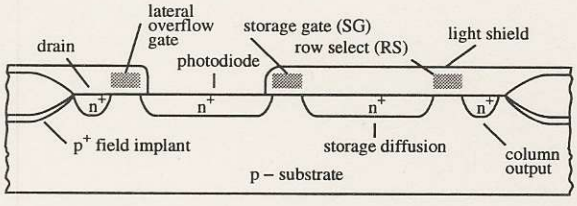

Figure 4: CMOS charge readout pixel cross section.

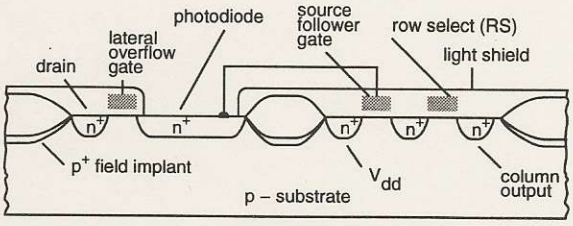

Figure 5: CMOS voltage output pixel cross section.

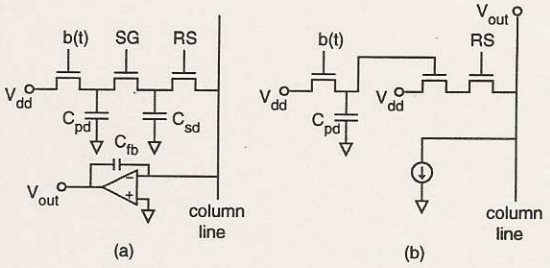

Figure 6: Equivalent circuits for CMOS pixels. (a) Charge readout pixel, (b) Source follower pixel.

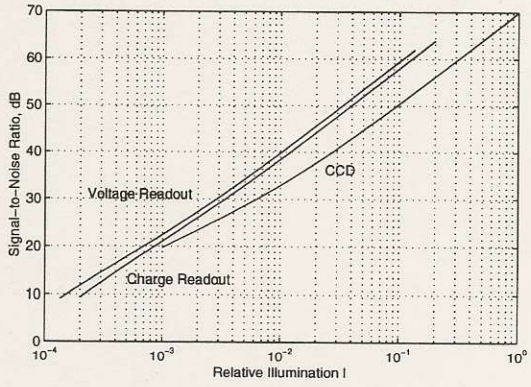

Figure 7: Noise for each pixel.

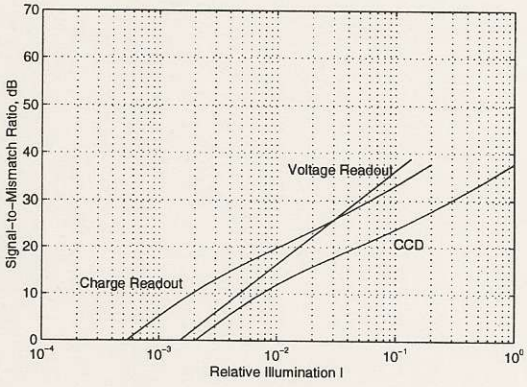

Figure 8: Mismatch for each pixel.