Active Pixel CMOS Image Sensor with On-Chip Non-Uniformity Correction

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abstract
This addressable CMOS imager counts 512 by 512 active pixels on a 6.6 µm pitch. A pixel consists of a photodiode and 3 MOSFETs using a 0.5 micrometer CMOS technology. This architecture allows pixel-by-pixel fixed pattern noise correction, with the analog non-volatile coefficients stored inside the pixel, by degrading the V_{th} of a MOSFET.

1. Active pixel concept

We present an 512 by 512 active pixel imager. The active pixel, shown in fig. 1, is rather compact, containing only a photodiode and 3 MOSFETs. By using 0.5 micrometer DLM CMOS technology we managed to shrink its size to 6.6 micrometer.
The imager has an addressable architecture, i.e. the pixels can be read out in a true random sequence, by applying a column (X) and a row (Y) address. The Y-address is decoded to activate only one row through a common gate electrode (fig. 1) ([1]). The signals of this row are fed to the common column buses. At the edge of the imaging plane these signals are again multiplexed using the decoded X-address.

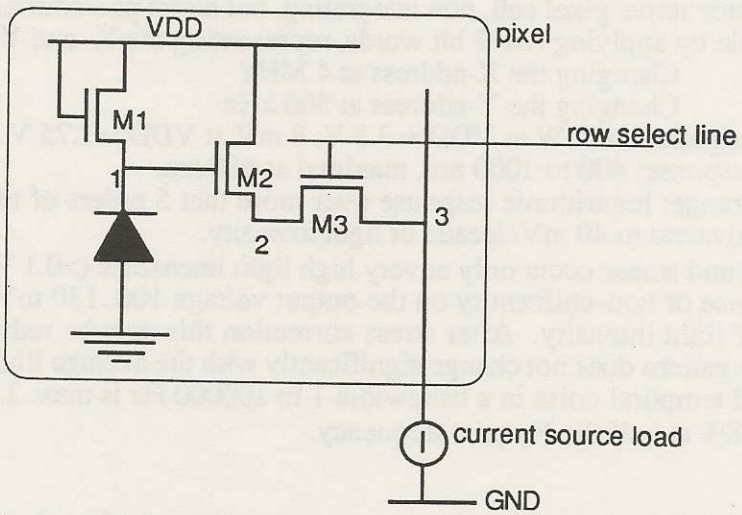

Figure 1 : Schematic representation of the pixel structure

The detected charge or photocurrent is continuously converted to a low impedance voltage signal within the pixel, so as to make the signal immune to external crosstalk. As the load MOSFET (M3) in the scheme operates in weak inversion, the photocurrent to voltage conversion is logarithmic. Note that this concept of continuous (= instantaneous) readout is different from the light integration that is usually found in CCDs and other MOS cameras.
As the address pulse timing does not have to synchronize to some integration time, the imager can be truly random addressable.
The pixel described above was implemented on a square grid with a pitch of 6.6 µm in a 512 by 512 image array. The total number of transistors amounts to about 808000. The fill factor is only 15 %. By virtue of the loagrithmic response, the small photosensitive area of this type of pixels (compared to the integrating type of imagers) does not degrade the speed performance. The nominal supply voltage is 3.3V, but it appears to work with no performance degradation between 1.7 V and 5 V. The device was processed with a surprising yield of 80% (allowing for defect columns).

As the principle of integration is abandoned, the signal to noise ratio of such pixels is far below the performance of high-end integrating sensors as CCDs. However the main disadvantage of this type of pixel is its extreme high non-uniformity due to the V_{th} thresholds in the pixel.

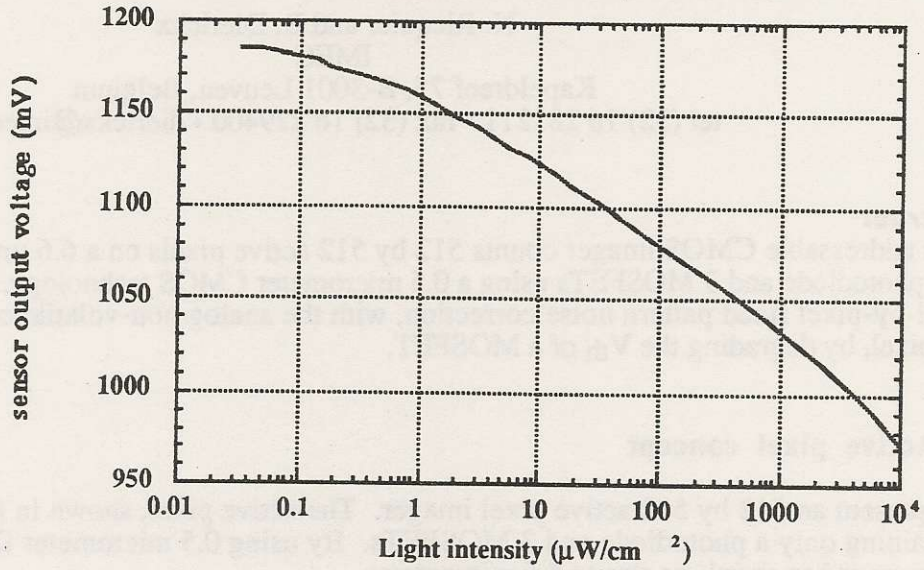

Figure 2 : Typical response curve

2. Imager specs (FUGA15a)

-512 by 512 pixels on a 6.6. μm pitch, die size: 3.9 x 3.9 mm^2
-a 3 transistor active pixel cell, non integrating, but direct photocurrent sensing
-addressable by applying two 9 bit words, representing the X- and Y-position
-speed: Changing the X-address at 4 MHz
Changing the Y-address at 500 kHz
-power dissipation: 45mW at VDD = 3.3 V; 8 mV at VDD = 1.75 V.
-spectral response: 400 to 1000 nm, maximal at 600 nm.
-dynamic range: logarithmic response over more that 5 orders of magnitude of illumination (fig.2). This is equivalent to 40 mV/decade of light intensity.
-blooming and smear occur only at very high light intensities (>0.1 W/cm^2)
-spatial noise or non-uniformity on the output voltage 100..130 mV p/p. This is about equal to two decades of light intensity. After stress correction this may be reduced below 5 mV p/p. The non-uniformity pattern does not change significantly with the average illumination level.
-Integrated temporal noise in a bandwidth 1 to 100000 Hz is max. 2.8 mV_{RMS}.
-MTF is 38% at half the Nyquist frequency.

3. Non volatile pixel offset correction by hot carrier degradation

The pixel structure inherently suffers from a large non-uniformity, caused by the distribution of the threshold voltages (V_{th}) of the MOSFETs in fig. 1. The actual non-uniformity is the sum of three V_{th} distributions. The situation is unfavourable as these MOSFETs have sub-micron effective sizes, which enhances the geometry dependent non-uniformity. For an acceptable image quality, the output signal must be offset corrected pixel by pixel, e.g. by using an external frame memory, or by software (the picture in fig. 3 is obtained in this way). This jeopardises the possibility of self-contained single chip smart vision systems. We found a solution that corrects the offsets internally in the pixel itself, without increasing the pixel or imager, and neither needs (external) memory, or software overhead.

We use the hot carrier degradation of MOS transistors, which is normally considered as a detrimental effect in semiconductor devices, to our advantage (ref. [2]). Degradation experiments indicated that to

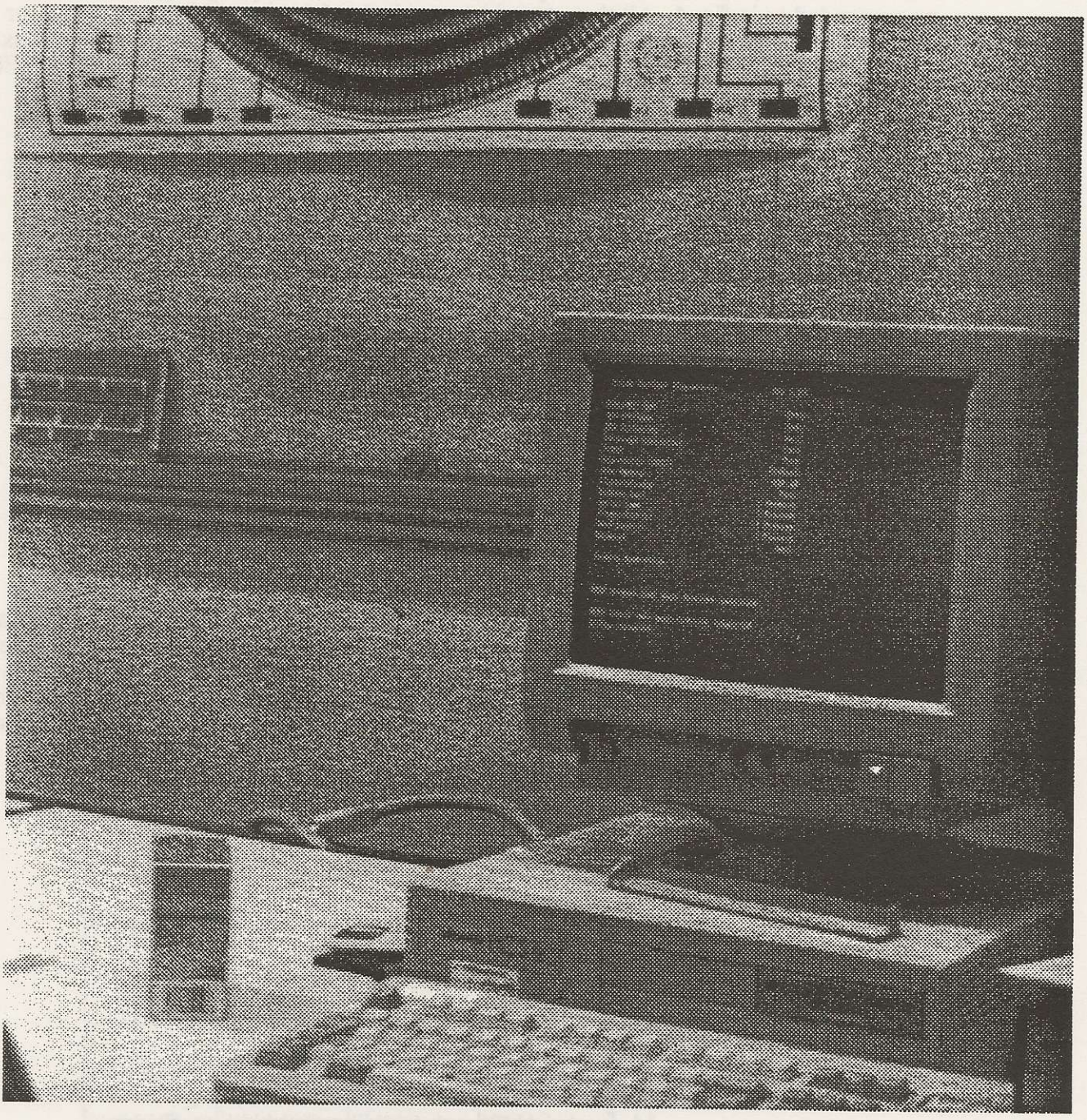

Figure 3 : Impression of the image quality of the 512*512 imager

a first approach only threshold voltages were affected, while the other transistor parameters such as the transconductance still remained quite stable. Therefore the periphery of the sensor architecture was extended as in fig. 4. All three transistor terminals of the source follower transistor in the pixel of choice can now be driven separately. This slightly modified architecture was used as the base of an experimental 256*256 imager which was processed in a 2.4 µm CMOS technology (FUGA12b).

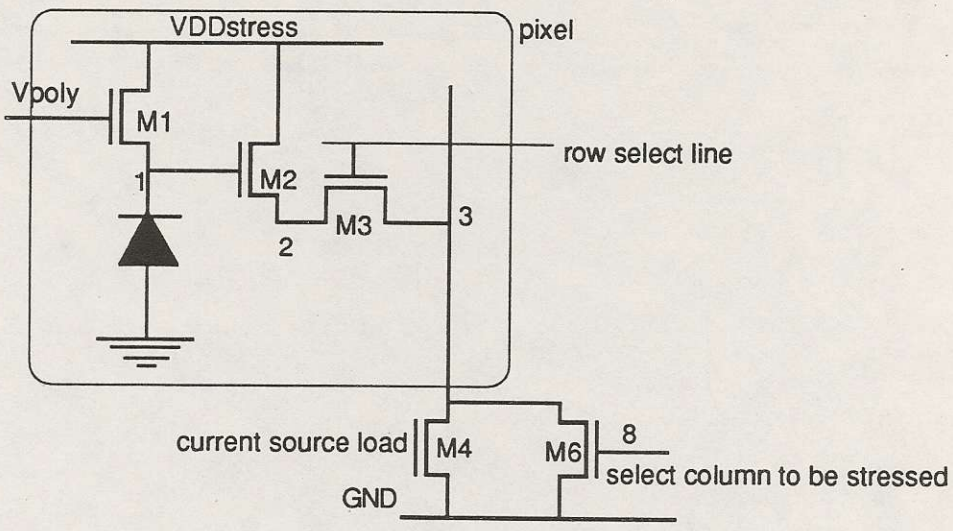

Figure 4 : Hot carrier degradation structure

In the actual structure, programming voltages of 16V at the VDDstress terminal and 9V for the Vpoly voltage of the load transistor, produced voltage shifts of 200 mV in about 10 minutes. Figure 5 illustrates that the stress operation can be performed without flattening the logarithmic response curve. We noted a relaxation effect that occurs after the stress operation. Therefore it is necessary to stress the pixel in consecutive iterations. In this way the non-uniformity of the response was reduced to the level of the temporal noise (5 mV p/p).

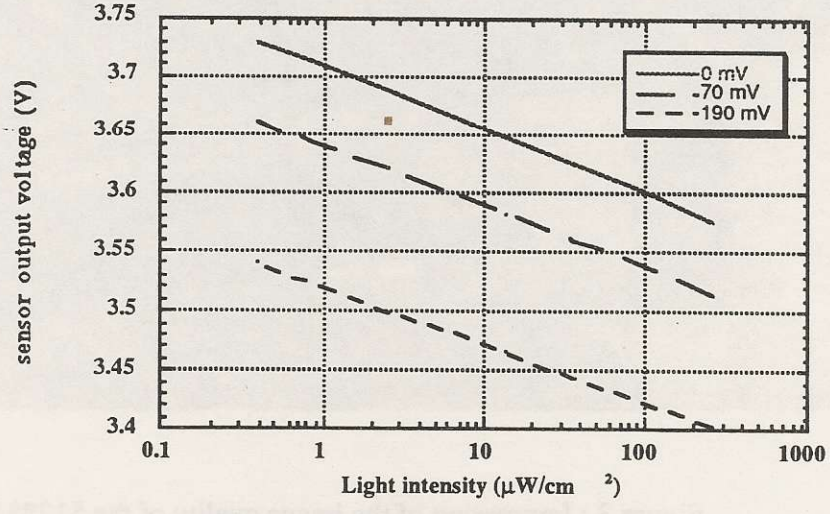

Figure 5 : Shift in response curve caused by the stress operation

The relaxation effect is only partly reproducible and not fully understood. Probably it can be explained by charge migration or by the local heating of the silicon during stress (partial self-anneal).

As we need some 10 minutes per pixel to calibrate, we have validated this hot carrier based calibration method only for small subwindows of the imager, with some 100 pixels in it, which can be stressed overnight or during a weekend. In principle the stressing time of a single MOSFET can be reduced to seconds or below, as demonstrated previously in [2]. But in the present architecture many MOSFETs are tied to the same bus lines. It turned out that leakage currents through the not-

selected branches cause a significant power dissipation when we wanted to increase the stressing voltages beyond the values that are quoted here.

Further effort will be devoted to improving the sensor architecture so that it allows higher stressing voltages, and pixel calibration on a parallel row by row basis, reducing the overall calibration time to an acceptable value.

4. Application area and conclusions

The imagers described above are at first intended for very compact, low cost, but high performance smart visions systems for industrial imaging purposes. For this purpose they should offer an acceptable image quality, which should however not rival the quality of high-end CCD. The device concept allows co-integration with digital logic, in order to build monolithic smart vision systems. Useful features for machine vision are: random access combined with the asynchronous readout allow to update information from any part of the scene at any time. The logarithmic response causes this sensor to respond to almost any illumination condition, with nearly perfect anti-blooming performance.
Finally we demonstrated that the impediment of the unacceptably large fixed-pattern noise can be solved by storing the offset coefficient inside the pixel.
In principle this method could also be used as a non-volatile analog frame memory, for template images, correlation and filter coefficients.

references

[1] N. Ricquier and B. Dierickx, "Pixel structure with logarithmic response for intelligent and flexible imager architectures", Microelectronics Engineering, vol. 19, p.547-550 (1992).
[2] H. Akimoto and B. Dierickx, "Study of a PROM used in a smart imager", IEICE Technical Journal, Japan (1993).

Figure 6 : photograph of the FUGA15a imager on the wafer