

A Switched CCD Electrode Programmable Photodetector

Bill Washkurak and Savvas Chamberlain
DALSA INC., 605 McMurray Rd.
Waterloo, Ontario, CANADA, N2V 2E9
(519) 886-6000 FAX (519) 886-8032

A new programmable photodetector that gives operator control over responsivity, and dynamic range through adjustment of a switched CCD electrode structure is presented. A series of three electrodes adjacent to a photocollection well forms a CCD implementation of a switched capacitor network. Beyond a given light intensity, the switched CCD network discards a fraction of the photogenerated signal charge into a drain, reducing the responsivity. The fraction of electrons discarded and thus, responsivity, is controlled by the rate of pulsing of the switched CCD electrodes. The light intensity level at which responsivity is reduced is controlled by the depth of the collection well potential beyond the switched CCD network potential. These two externally controlled features permit operator adjusted responsivity. By reducing the responsivity at brighter light intensities, the dynamic range is increased.

A potential well diagram and cross-section of the photodetector is shown in Figure 1. The switched CCD network consists of three adjacent gate electrodes, SC1, BIAS and SC2. The photogenerated signal charge collection well is formed with the PCK and SCK electrodes. The TCK electrode is used to transfer the signal charge into the readout CCD shift register. The drain discards the current that flows through the switched CCD electrode network. Photogenerated signal charge at low light levels collects entirely in the PCK/SCK collection well for maximum photosensitivity. At higher light levels, the signal charge overflows the PCK/SCK collection well into the switched CCD electrode network. SC1 and SC2 are pulsed such that with each cycle of the SC electrodes, a charge packet proportional to the number of electrons in the PCK/SCK collection well is discarded into the drain diffusion. Equilibrium between charge photogeneration and charge removal is reached at a level of charge in the collection well proportional to the incident light intensity. At the end of the integration period, SC1 is turned 'off', isolating the switched CCD electrode network, and PCK, SCK and TCK are sequentially collapsed transferring the signal charge into the CCD readout shift register. Figure 2 shows a top view of the photodetector layout. The device organization is suitable for implementation with CCD processes.

Figure 3 shows the measured response of a photodetector implemented in a long linear CCD image sensor array, given a 150 μ s integration time with 760 nm wavelength illumination. Note the two regions of operation and the effect of the switched CCD electrode clock period on the responsivity. Figure 4 shows a linear-logarithmic plot of the photodetector response illustrating the extended dynamic range.

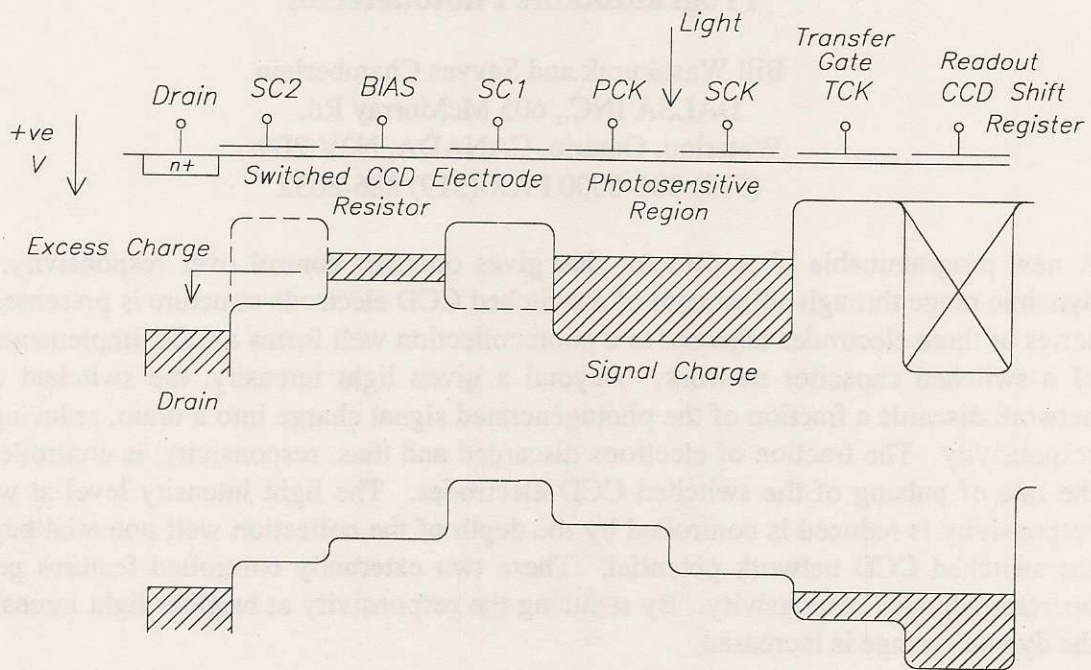


Figure 1: Photodetector cross-section along with two different potential well diagrams showing integration and readout.

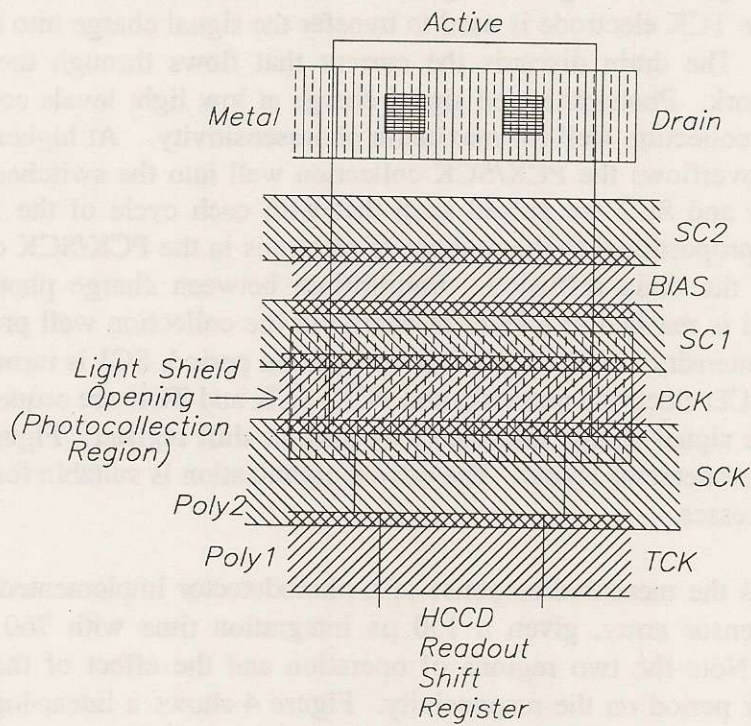


Figure 2: Top view of the photodetector layout. The multiple electrode organization of the layout lends itself to easy implementation with a CCD process.

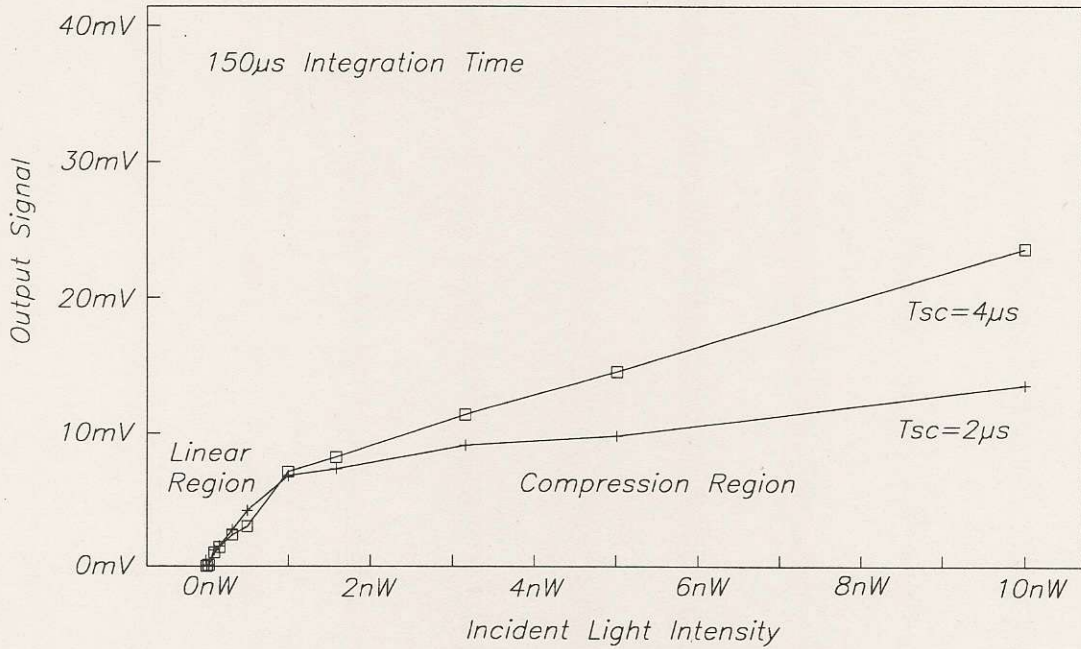


Figure 3: Measured response of the photodetector showing two distinct regions of operation. Reduced switched CCD network clock period reduces the responsivity of the device.

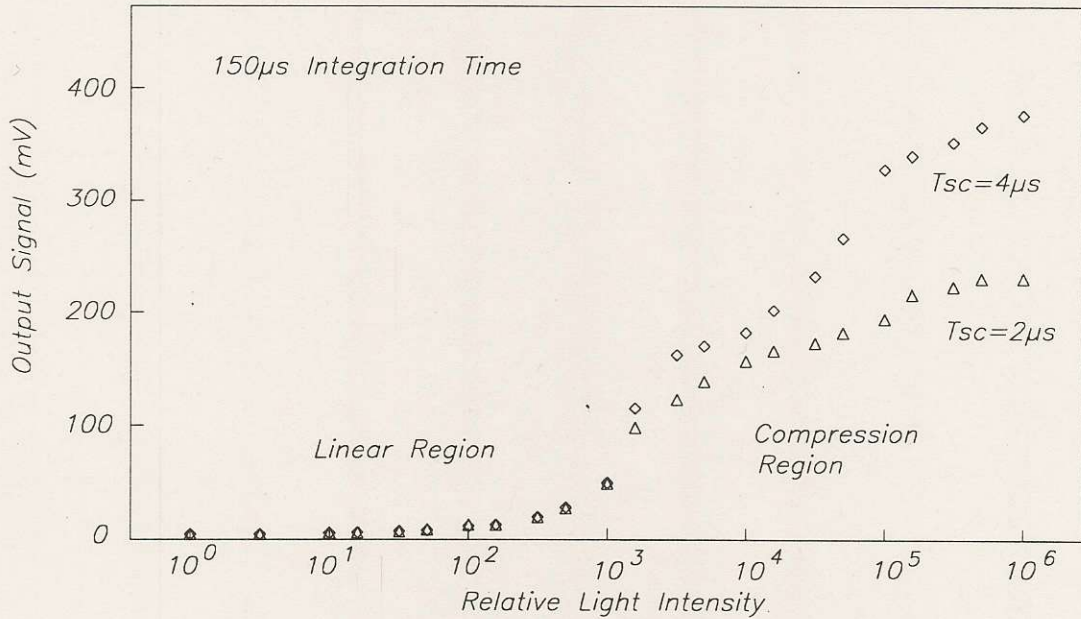


Figure 4: Measured response of the photodetector illustrated on a linear-logarithmic graph showing the extended dynamic range.