

Design of a CMOS/CCD High-Speed Memory for use in Parallel/Pipelined
Sampled-Analog Signal Processing

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A high-speed SPS memory is the crucial element needed to convert a wide-bandwidth sequential process into a moderate-bandwidth parallel process. This presentation will review the development of a 150MSPS/128Ks monolithic memory for fabrication in a 2 μ m n-well CMOS/CCD process. In addition to the design of the CCD structure, the design of a myriad of analog and digital circuitries will be discussed. The memory is self-sufficient in that all high-speed signal conditioning and non-5V clocking circuitry has been incorporated into a user-friendly device.

OUTLINE

- 1) CCD-based Sampled-Analog Signal Processing Overview
- 2) SPS Review and Monolithic Memory Architecture
- 3) Design of the CCD structure
- 4) Design of high-speed and MPP clock drivers
- 5) Design of peripheral CMOS analog circuitry
- 6) Review of test results