

# A FAST FRAMING 512(H) x 512(V) CCD IMAGE SENSOR

Steve Strunk, Pao Chen, and Hsin Fu Tseng, EG&G RETICON

The authors have developed a fast framing CCD image sensor for high speed photographic applications. The design of the 1/2-inch format 262k (512 x 512) pixel array, is constructed on a 16 $\mu$ m square pixel pitch and features 1kHz frame rate, lateral antiblooming (2000x), a windowing function for tracking applications, and 67 dB dynamic range. Sixteen parallel outputs operating at 20MHz and a split frame transfer architecture are used to achieve the high frame rate. Processing is based on a triple poly, triple metal process.

The lateral antiblooming structure uses the buried drain concept [1]. Our modification relies on a 2 micron wide surface channel barrier, adjacent to a 2 micron wide implanted drain. These run parallel to the CCD column, to define the vertical channel stops. This structure is formed using a single mask, to achieve small feature sizes and minimize loss in sensitivity. The buried drain has been also implemented in the horizontal CCD to allow a sub-framing mode of operation. Sub-frame readout is useful in high speed tracking applications, and is effected by dumping unwanted lines of data without clocking the horizontal shift register. Because of the fixed barrier potential associated with this structure, one horizontal shift sequence is needed to clear the CCD before reading valid data.

Pixel unit cell capacitance of 20fF and poly resistance of 25 $\Omega/\square$ , result in an RC time constant of 100ns, when vertical clock lines are driven from both ends. This results in the line shift frequency of 2.5MHz, consuming 200 $\mu$ s for combined frame shift and line shift operations. Sixteen output taps operating at 20MHz requires an additional 660 $\mu$ s from the desired frame time of 1 millisecond; the combined time for frameshift and readout is 860 $\mu$ s. Use of the efficient split storage scheme yields a 90% duty cycle for integration at a frame rate of 1kHz.

Output buffer amplifiers have been designed for high data rates: the measured -3dB point is 90MHz, with 11pF load capacitance. This is comfortable margin for the designed data rate of 20MHz. Noise characteristics of the output amplifier include the  $f^{-1}$  corner frequency of 500kHz and white noise component of 9nV/ $\sqrt{\text{Hz}}$ . A moderately high corner frequency results from use of enhancement mode transistors yielding good linearity and reduced bias requirements. This value is not significant at the intended data rate and is lower than reported buried channel designs using LDD implants [2,3].

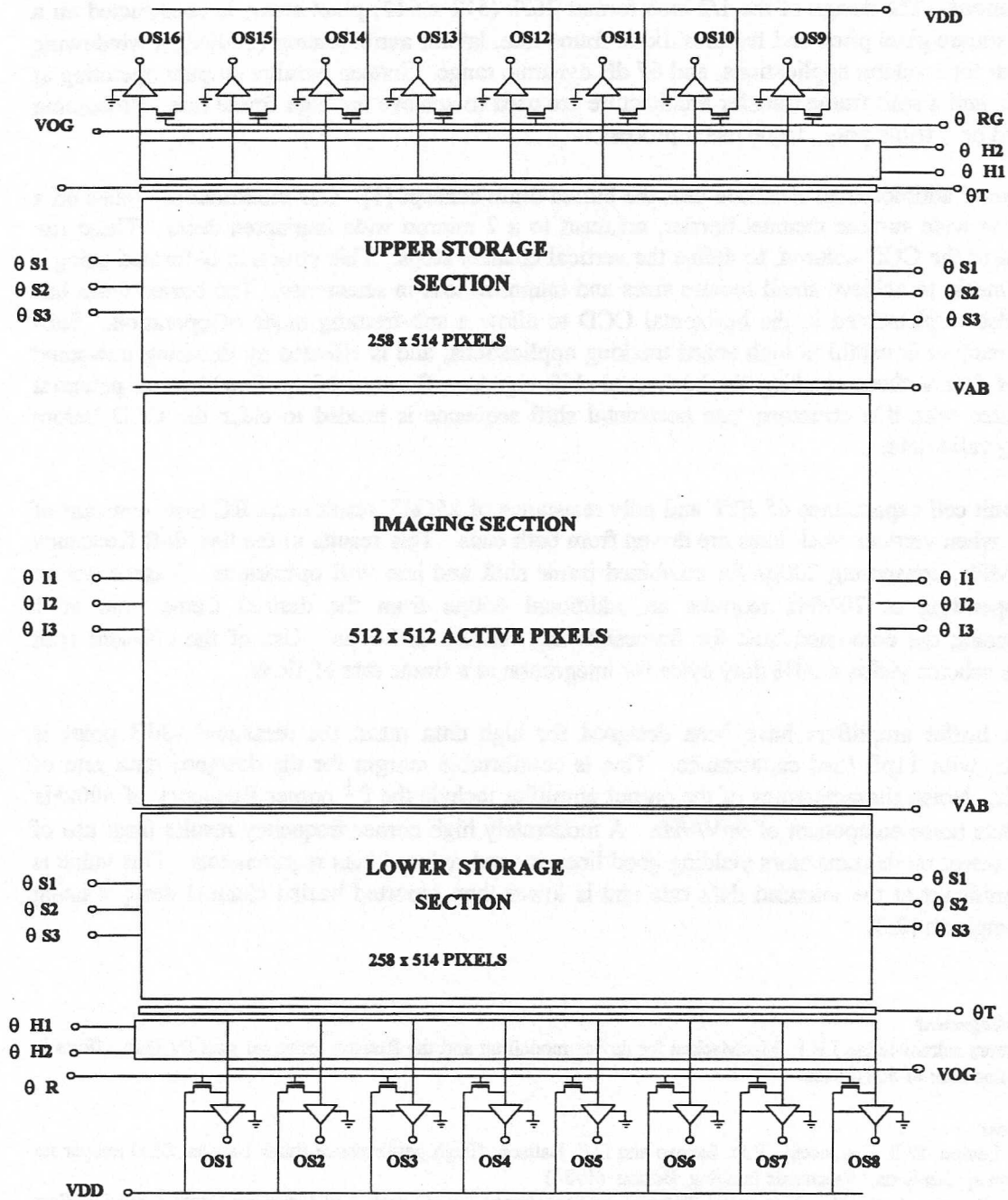
## *Acknowledgement*

The authors acknowledge J.R.F. MacMacken for device modelling and the Reticon technical staff for their efforts in the development of this device.

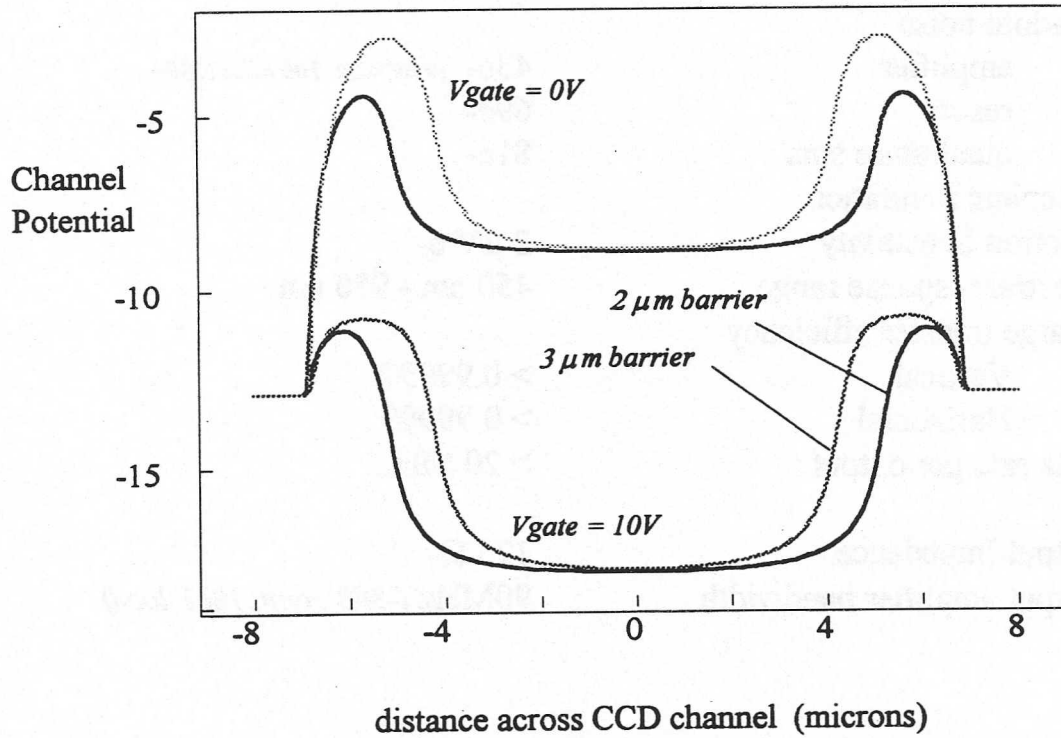
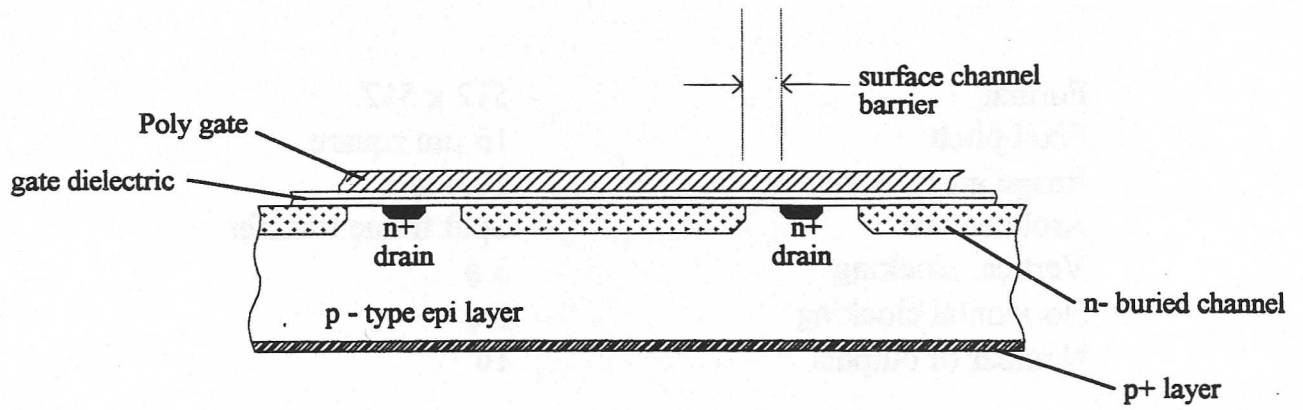
## *References*

1. P.A. Levine, W.F. Kosonocky, E.D. Savoye and D.F. Battson, "High performance frame transfer CCD imager for television applications," Electronic Imaging, Boston (1984)
2. E.G. Stevens, et. al., "A 1-Megapixel, Progressive Scan Image Sensor with Anti-blooming Control and Lag-Free Operation," Trans. Elec. Devices, ED-38, No. 5, May 1991
3. B.E. Burke, et. al., "An Abutable CCD Image Sensor for Visible and X-Ray Focal Plane Arrays," Trans. Elec. Devices, ED-38, No. 5, May 1991

# Device Architecture Schematic

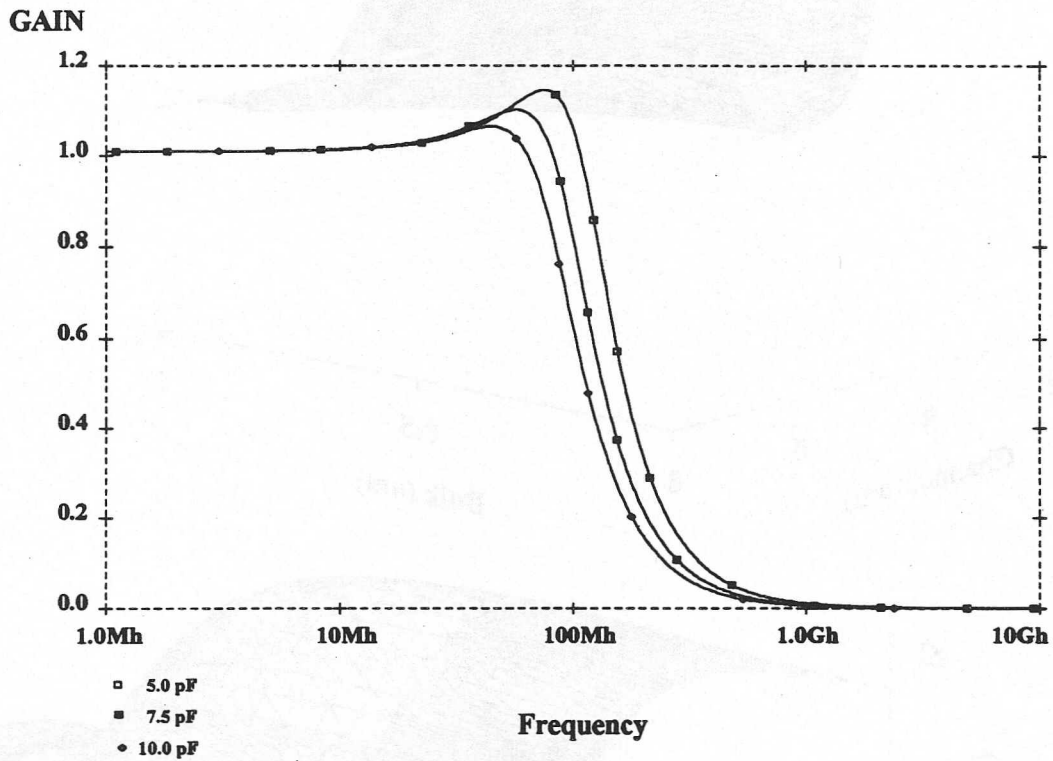


### Cross-section and potential profile of the anti-blooming structure

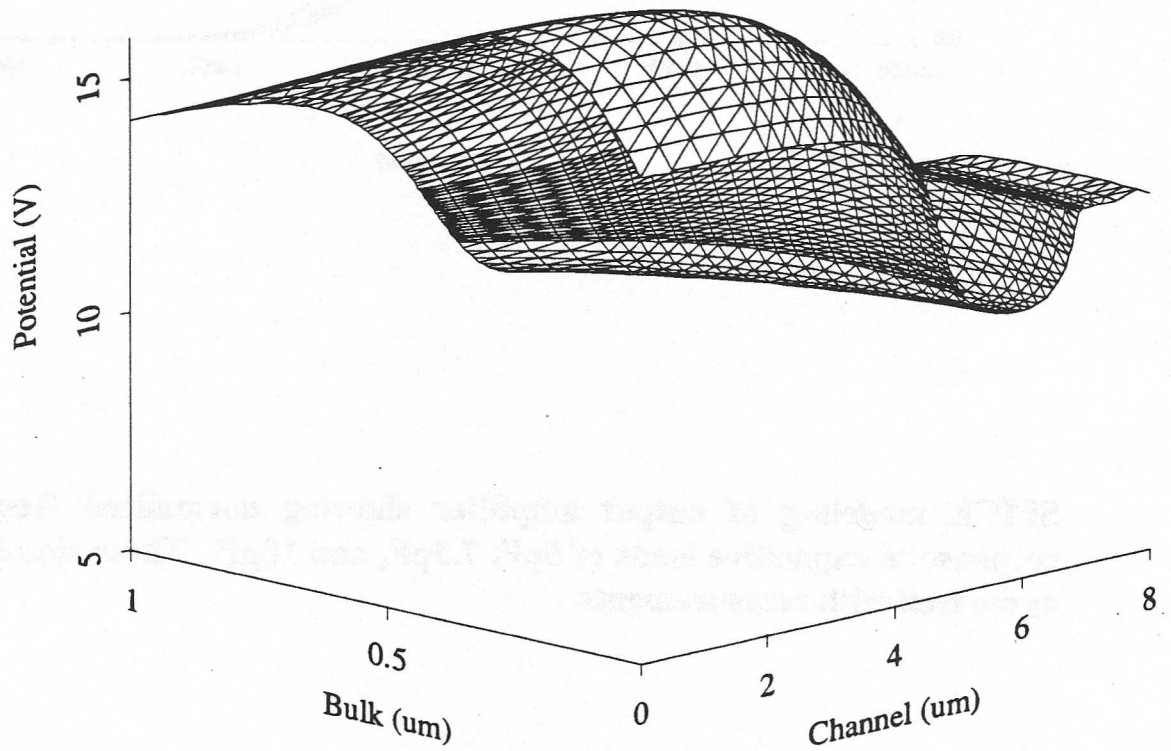
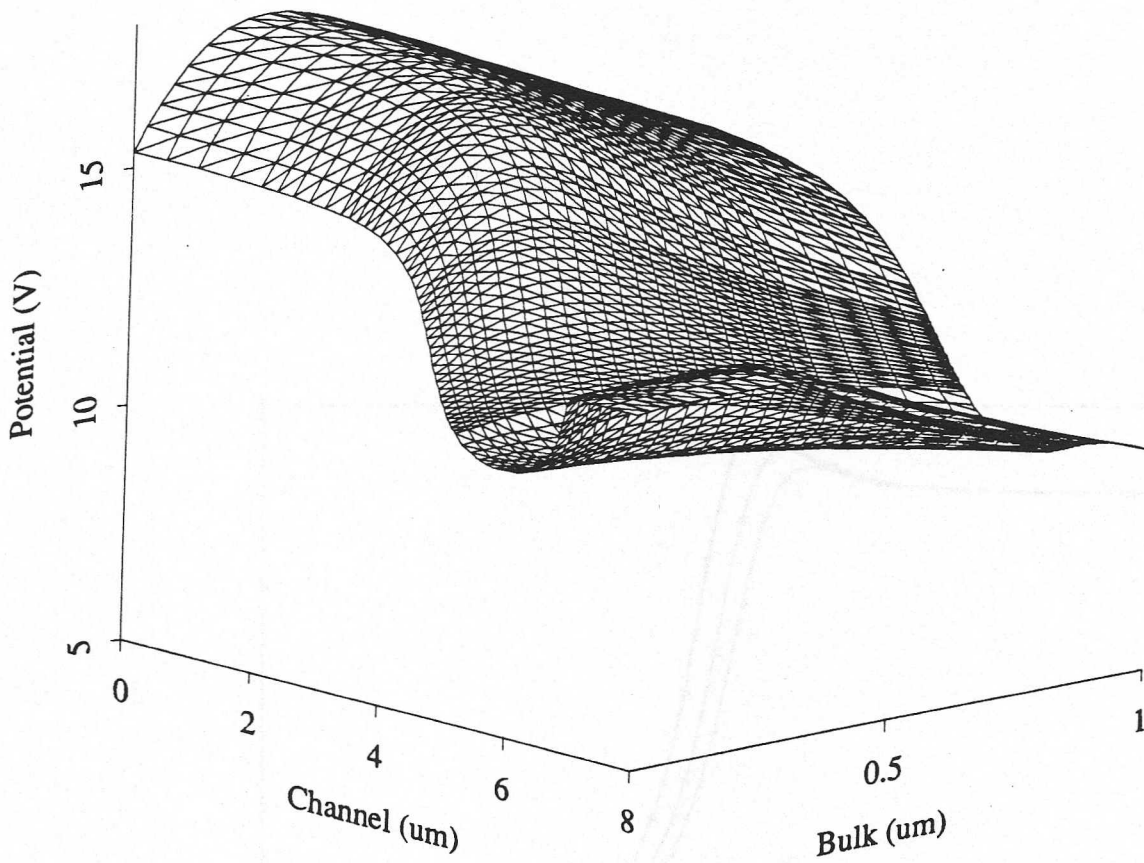


## Physical and Performance Specifications

Format	512 x 512
Pixel pitch	16 $\mu\text{m}$ square
Image area diagonal	11.6 mm
Architecture	Split frame transfer
Vertical clocking	3 $\phi$
Horizontal clocking	2 $\phi$
Number of outputs	16
Frame rate	1,000 fps
Anti-blooming capacity	2,000x
Dynamic range	67 dB (10 bits)
Readout noise	
amplifier	43e- ( <i>9 nV/<math>\sqrt{\text{Hz}}</math>, 100 MHz NBW</i> )
reset	69e-
quadrature sum	81e-
Faceplate Saturation	
Electron Sensitivity	2 $\mu\text{V}/\text{e}^-$
Spectral response range	450 nm - 950 nm
Charge transfer efficiency	
Vertical	> 0.99999
Horizontal	> 0.99999
Data rate per output	> 20 MHz
Output Impedance	175 $\Omega$
Output amplifier bandwidth	90MHz ( <i>-3dB point, 10pF load</i> )



**SPICE modeling of output amplifier showing normalized frequency response to capacitive loads of 5pF, 7.5pF, and 10pF. These simulations agree well with measurements.**



**Modelling of the anti-blooming structure in two spatial dimensions. Channel potential contours are shown on the z-axis. The x and y axes correspond to device physical dimensions perpendicular to the channel and into the bulk.**