Time Delay and Integration (TDI) Charge Coupled Device (CCD) – Device Design and Applications

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Outline of this talk

1. Introduction
2. TDI Operation Principles, Examples, Advantages
3. Device Design
4. Comparison with Photodiode Linear Arrays
5. TDI CCD Design Case Study
6. Future Trends and Major Development Issues

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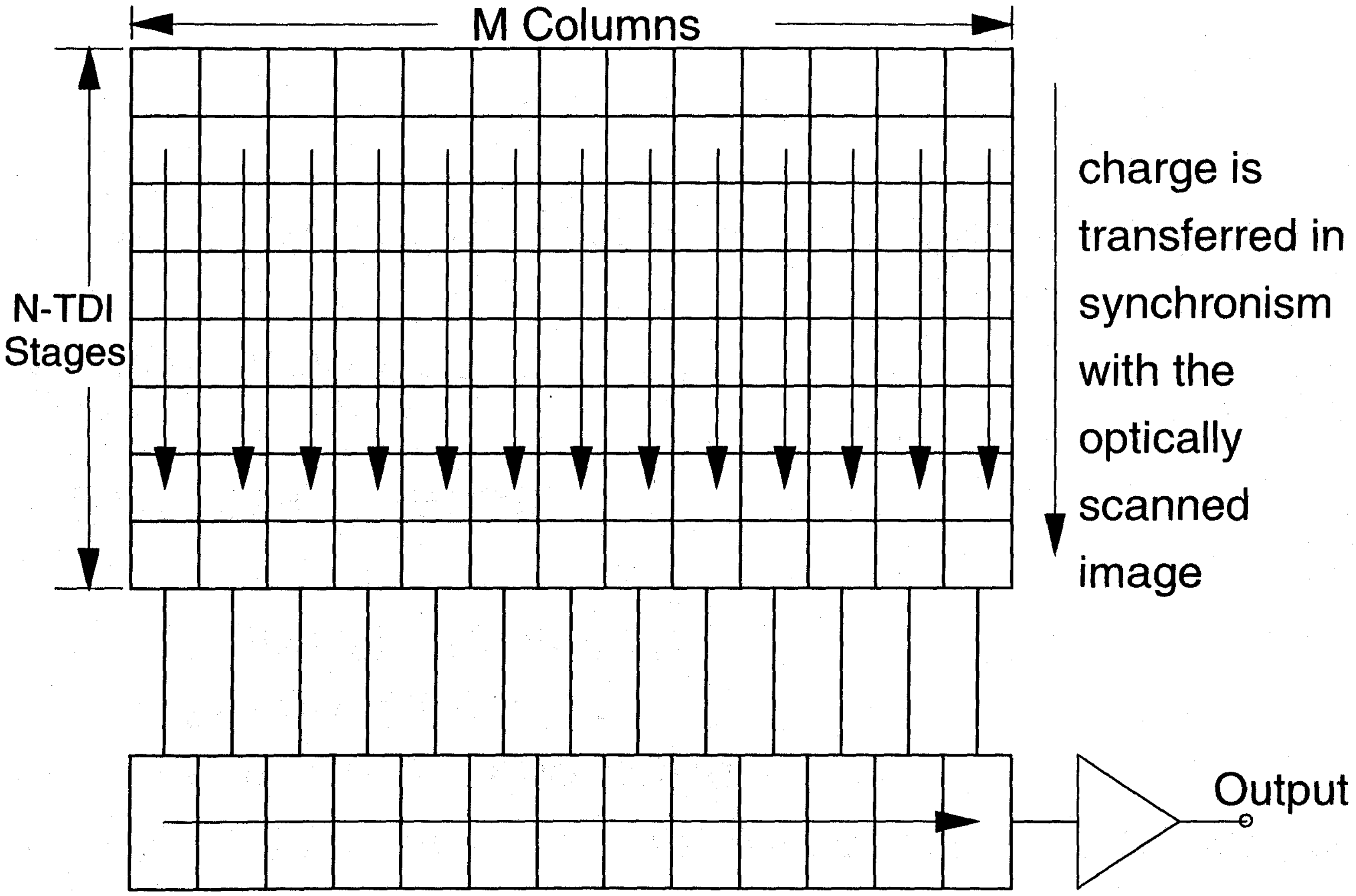


Time-Delay-and-Integration (TDI) Mode of Operation

Why TDI CCD ?

Advantages:

1. Enhanced photo–sensitivity without sacrificing output data rate
2. Increased signal–to–noise ratio
3. Photo–response uniformity ← averaging
4. Dark current uniformity ← averaging
5. Electronic exposure control

Disadvantages:

1. Complex drive circuitry (parallel clocks)
2. Large chip (device yield)
3. Spectral response: low blue response,
   non–uniform response

TDI Implementation Examples

Visible:

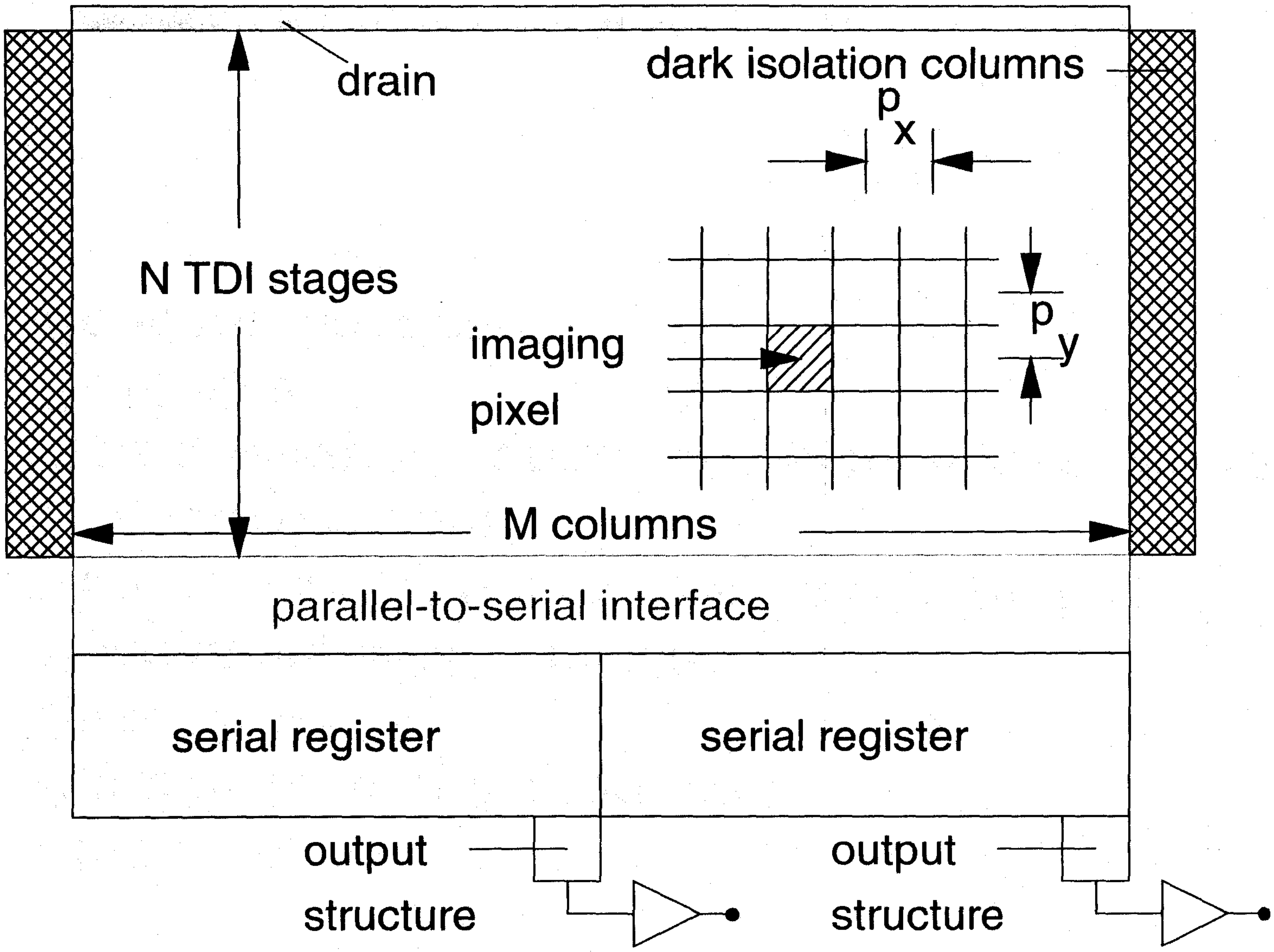
1. Airborne reconnaissance
2. Astronomy, satellite
3. Document scanning ← this talk

Infra–red:

1. Hybrid TDI
2. Monolithic TDI IR focal plane

Others:

1. X–ray
2. Sonar beam steering



Time-Delay-and-Integration Charge Coupled Device (TDI CCD) Architecture

TDI CCD Device Design

1. Parallel array
2. Parallel–to–serial interface
3. Serial Register
4. Resolution, MTF, clocking
5. Number of TDI stages, sensitivity, and
   exposure control
6. Noise, dynamic range, and signal–to–noise ratio
7. Pixel size
8. Spectral response

TDI CCD Parallel Array Design

- Imaging area
  - MOS polysilicon photo–gates
- Surface channel
  - large charge capacity
- Buried channel
  - low noise
  - high speed
  - no interface states interaction
  - saves one mask

TDI CCD Parallel Array Design

- Number of columns >> number of rows
  → high chip aspect ratio

- Problems of large arrays:
  1. Lithography (discussed later)
  2. RC charging time of polysilicon electrodes
     a. distributed RC transmission line
     b. limits maximum line scan time
     c. drive parallel clock electrode at multiple locations
     d. smaller pixel size
     e. fringing field capacitance

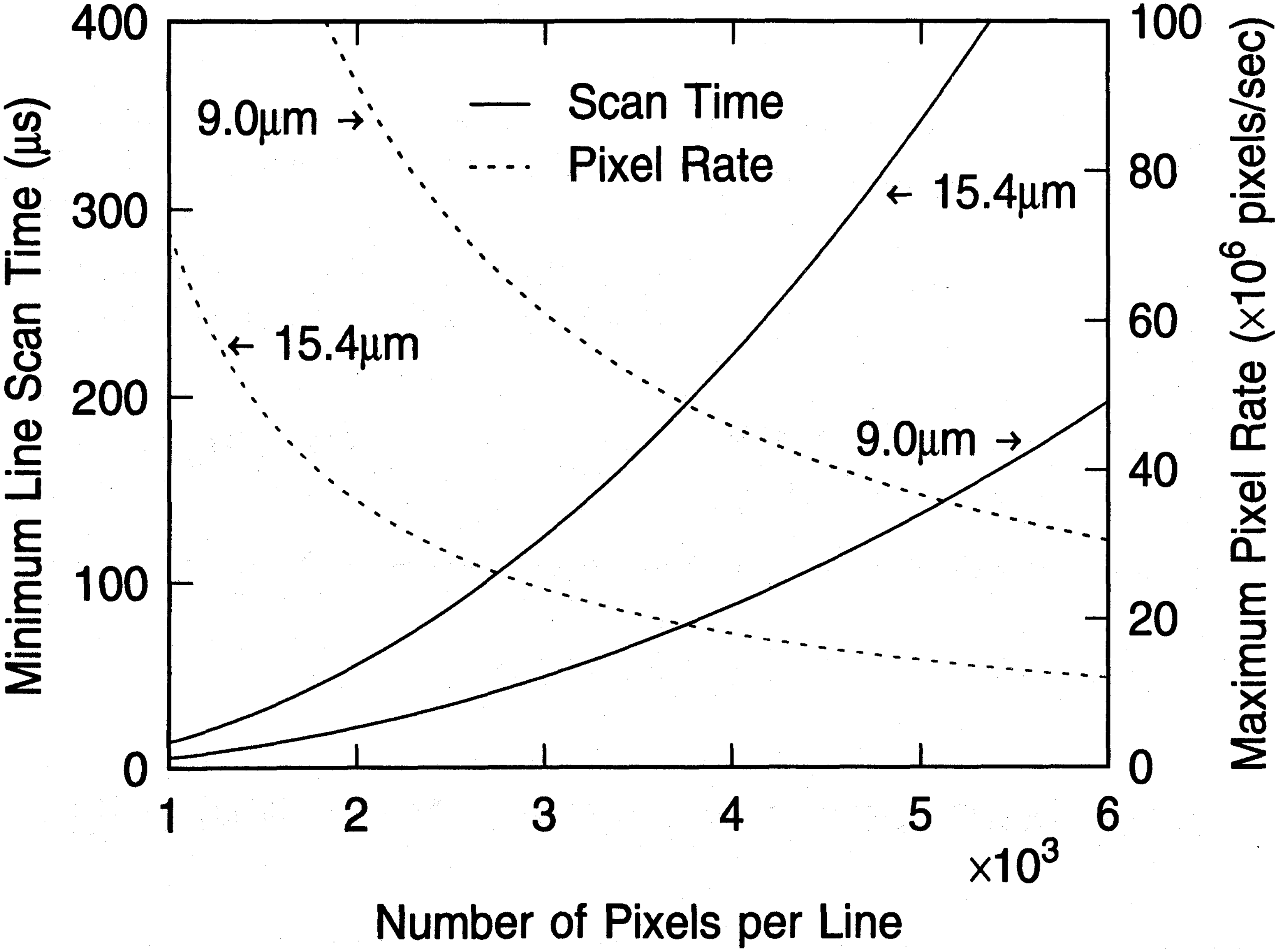
Distributed RC Limits Maximum Line Time

$$R = R_s \frac{L_{electrode}}{W_{electrode}} \tag{1}$$

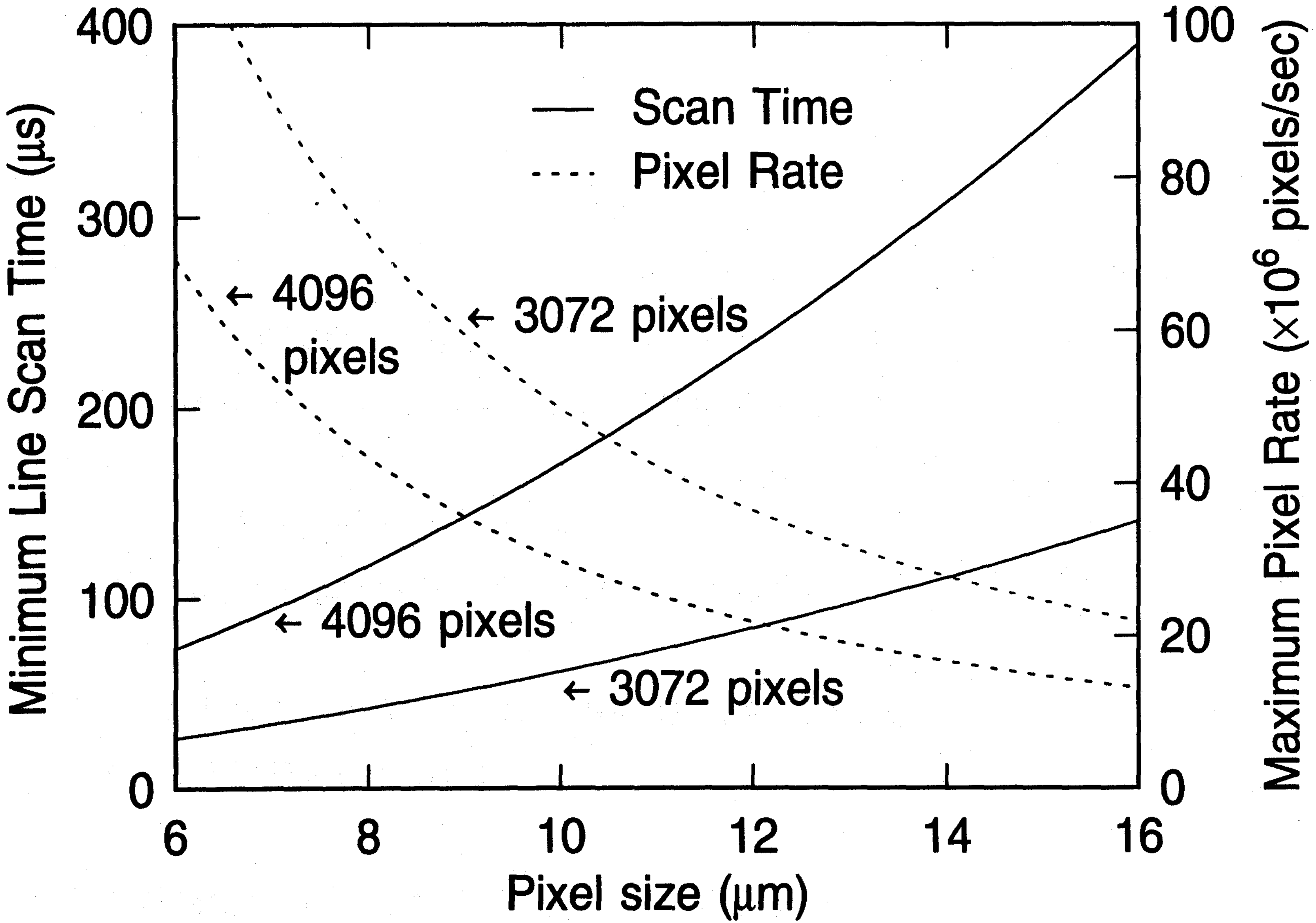
$$C = C_{area} \times (L_{electrode} W_{electrode}) + C_{perimeter} \times L_{electrode} \tag{2}$$

$$t_{line\,-\,scan} = N_{clock}\, R_s\, (C_{area} + \frac{C_{perimeter}}{p_y / N_{electrode}})\, (\frac{Mp_x}{2})^2 \tag{3}$$

p_x = pixel center spacing in x-direction
p_y = pixel center spacing in y-direction
$L_{electrode} \simeq Mp_x/2$
$W_{electrode} \simeq p_y/Nelectrode$ (assume equal width, no overlap)
N_{clock} = Number of clock transitions per TDI stage transfer



Minimum Line Scan Time (μs)
400
300
200
100
0
Maximum Pixel Rate (×10^6 pixels/sec)
100
80
60
40
20
0
1
2
3
4
5
6
×10^3
Number of Pixels per Line
Scan Time
Pixel Rate
9.0μm →
← 15.4μm
← 15.4μm
9.0μm →



Minimum Line Scan Time (µs)
0
100
200
300
400
Maximum Pixel Rate (×10^6 pixels/sec)
0
20
40
60
80
100
Pixel size (µm)
6
8
10
12
14
16
Scan Time
Pixel Rate
← 4096 pixels
← 3072 pixels
← 4096 pixels
← 3072 pixels

Parallel–to–Serial Interface

- 90 degrees turn:
  imaging area to serial register

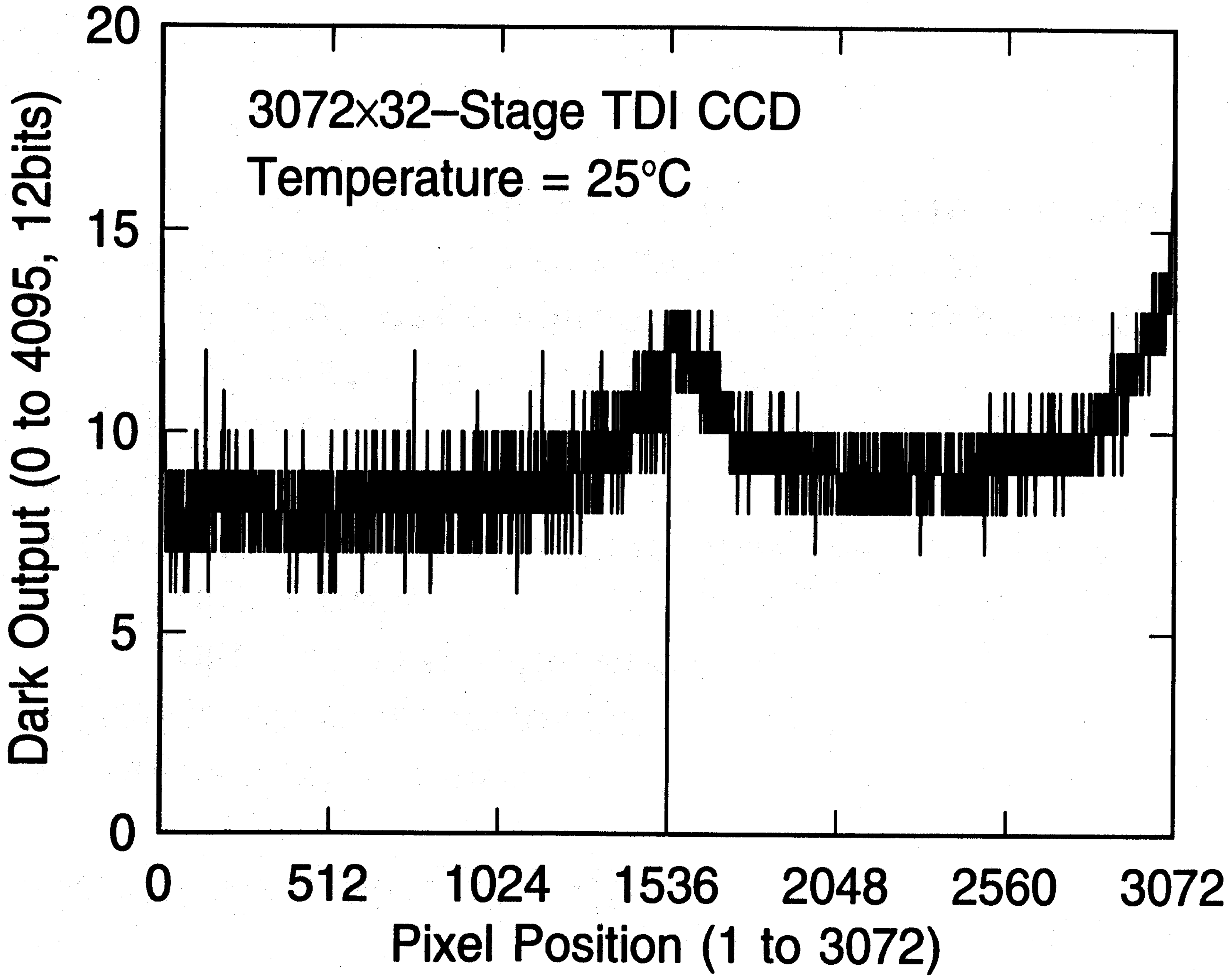
- Potential barrier at the corner

  [Chamberlain, *CICC,* 1982]

- Common problem as other CCD
  architectures

Serial Register Design

- Long serial register
- Buried channel required
  - high transfer efficiency
  - high speed
- Multiplexed serial register [Angle, *Conf. CCD Appl.* 1978]
- In–line output tap
  - a. reduce number of transfers
  - b. increase effective data rate
  - c. fit final stage within one CCD stage length
  - d. limited choice of output structures
  - e. local power dissipation → local temp. rise


3072x32–Stage TDI CCD
Temperature = 25°C
Dark Output (0 to 4095, 12bits)
Pixel Position (1 to 3072)
20
15
10
5
0
0
512
1024
1536
2048
2560
3072

Resolution, MTF, Clocking

- Finite sampling aperture (H,V)
- Velocity mis–match (V)
- Discrete charge motion (V)
- Angular mis–alignment (H)
- Transfer inefficiency (H,V)
- Carrier diffusion (H,V)

[Barbe, in *Solid Stage Imaging,* 1975]

Modulation Transfer Function (MTF)

$$MTF_y = MTF_{aperture,y} \times MTF_{velocity} \times MTF_{discrete} \times MTF_{transfer,y} \qquad (4)$$

$$MTF_x = MTF_{aperture,x} \times MTF_{alignment} \times MTF_{transfer,x} \qquad (5)$$

MTF of a Sampling Aperture

$$MTF(f) = \frac{\sin(\pi f L)}{\pi f L} \tag{6}$$

$$f_N = 1/2p \tag{7}$$

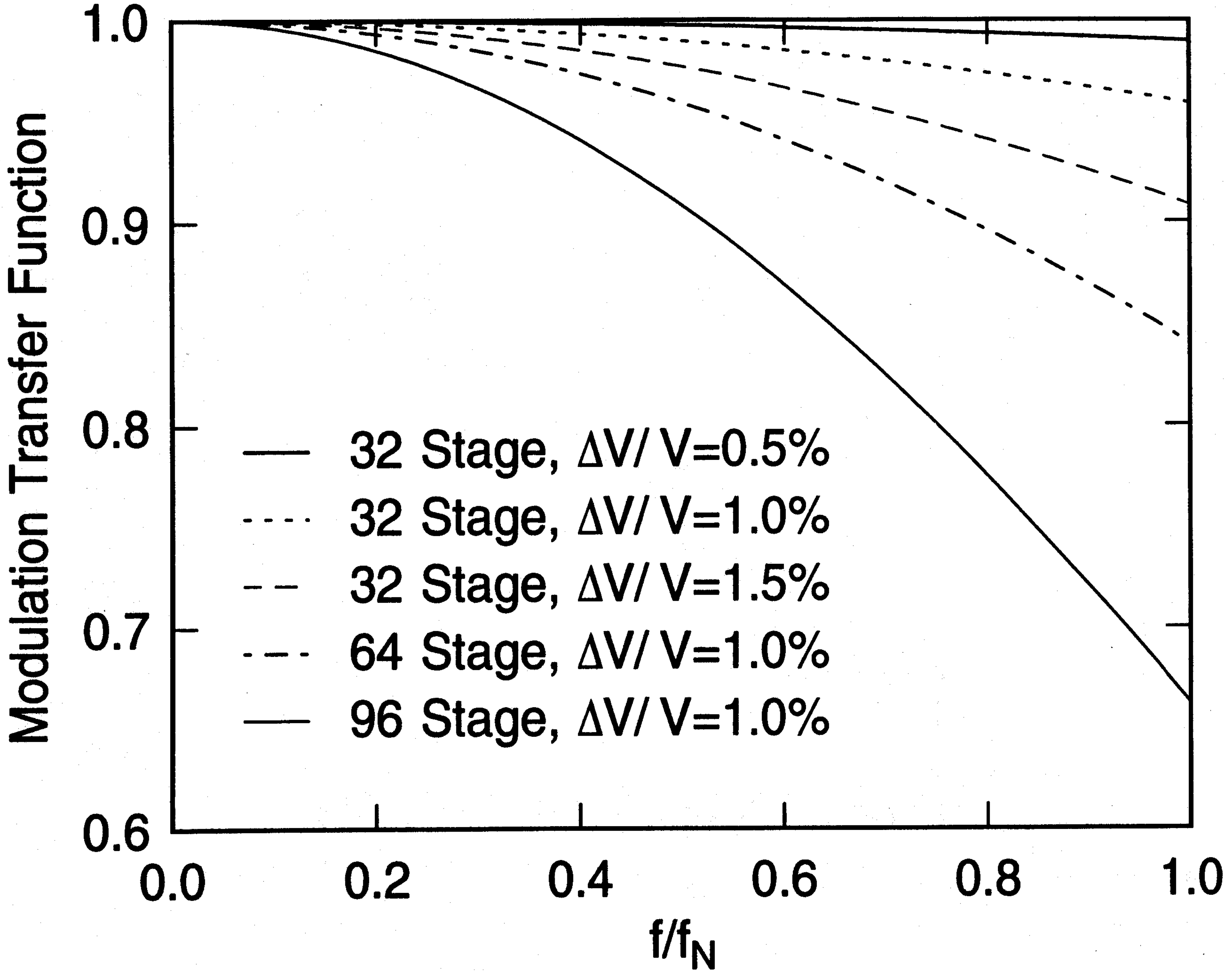
$$MTF(f) = \frac{\sin(\frac{\pi}{2}\frac{f}{f_N}\frac{L}{p})}{\frac{\pi}{2}\frac{f}{f_N}\frac{L}{p}} \tag{8}$$

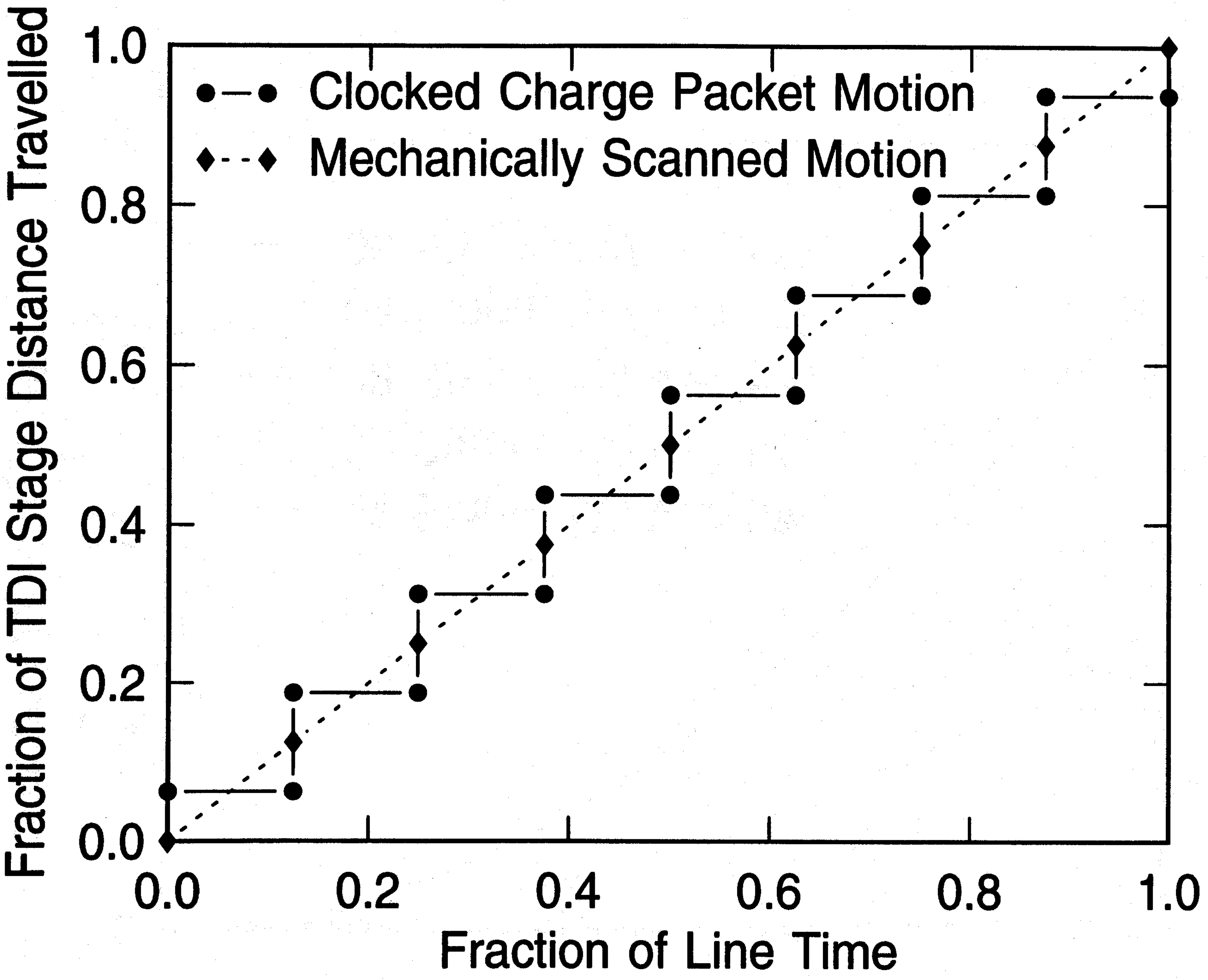
p = pixel center spacing
L = effective width of sampling aperture
f = spatial frequency
f_N = Nyquist frequency

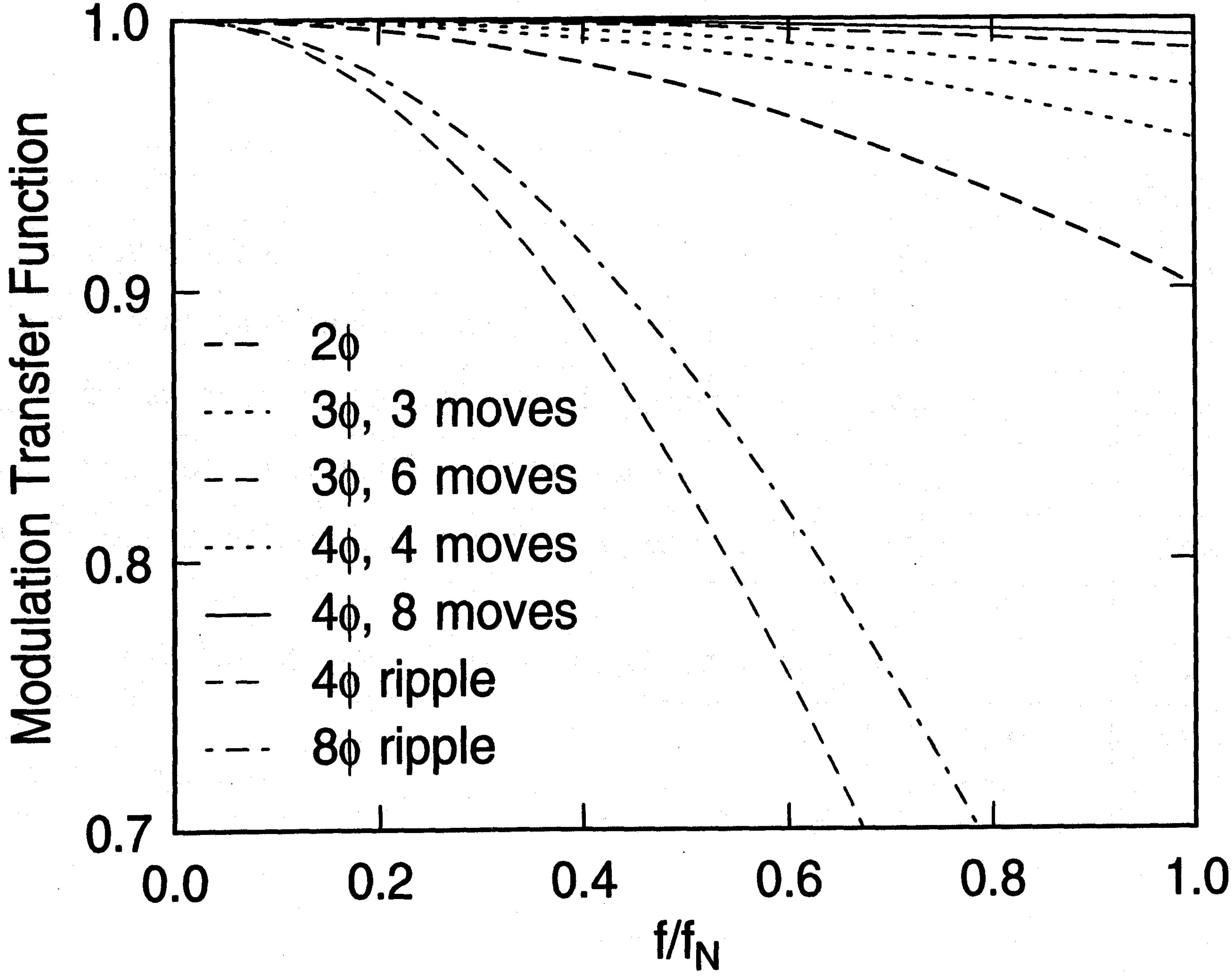
MTF Loss due to Velocity Mis-Match

$$MTF_{velocity}(f) = \frac{\sin(\pi f \frac{Np_y \Delta V}{V})}{\pi f \frac{Np_y \Delta V}{V}} = \frac{\sin(\frac{\pi}{2} \frac{f}{f_N} \frac{N\Delta V}{V})}{\frac{\pi}{2} \frac{f}{f_N} \frac{N\Delta V}{V}} \qquad (9)$$

ΔV = difference in velocity
V = scanning velocity
N = Number of TDI stages
p_y = pixel center spacing in the y-direction


Modulation Transfer Function
1.0
0.9
0.8
0.7
0.6
0.0
0.2
0.4
0.6
0.8
1.0
f/f_N
32 Stage, ΔV/ V=0.5%
32 Stage, ΔV/ V=1.0%
32 Stage, ΔV/ V=1.5%
64 Stage, ΔV/ V=1.0%
96 Stage, ΔV/ V=1.0%

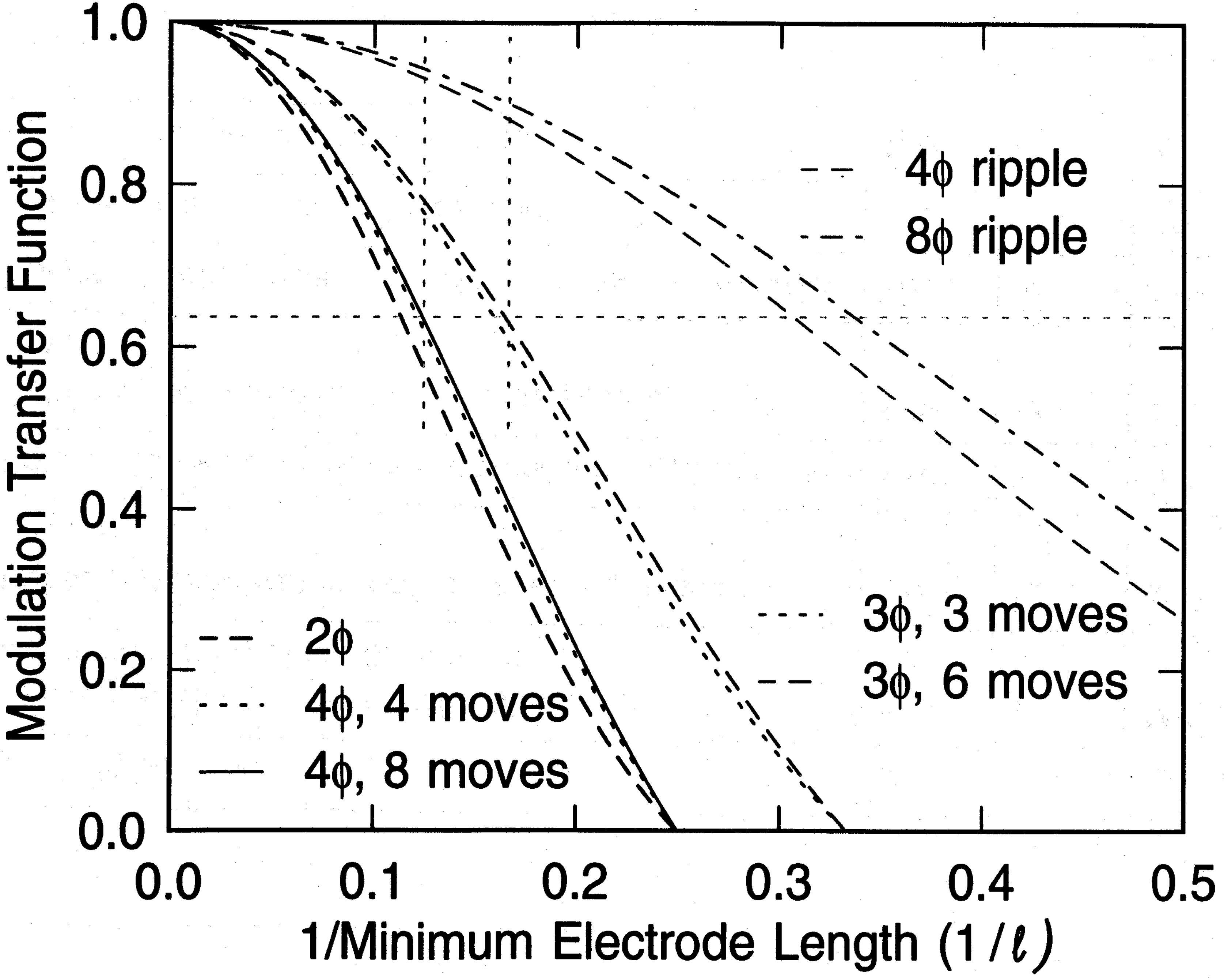

Clocked Charge Packet Motion
Mechanically Scanned Motion
Fraction of TDI Stage Distance Travelled
Fraction of Line Time
0.0
0.2
0.4
0.6
0.8
1.0
0.0
0.2
0.4
0.6
0.8
1.0



Modulation Transfer Function
1.0
0.9
0.8
0.7
0.0
0.2
0.4
0.6
0.8
1.0
f/f_N
2ϕ
3ϕ, 3 moves
3ϕ, 6 moves
4ϕ, 4 moves
4ϕ, 8 moves
4ϕ ripple
8ϕ ripple

Clocking Method	Effective Aperture *L*	MTF at Nyquist
Two phase, overlapping or non-overlapping clock (2 moves)	*p*/2	0.900
Three phase, non-overlapping clock (3 moves)	*p*/3	0.955
Three phase, overlapping clock (6 moves)	*p*/6	0.989
Four phase, non-overlapping clock (4 moves)	*p*/4	0.974
Four phase, overlapping clock (8 moves)	*p*/8	0.994
Four phase, ripple clock	4*p*/3	0.413
Eight phase, ripple clock	8*p*/7	0.543

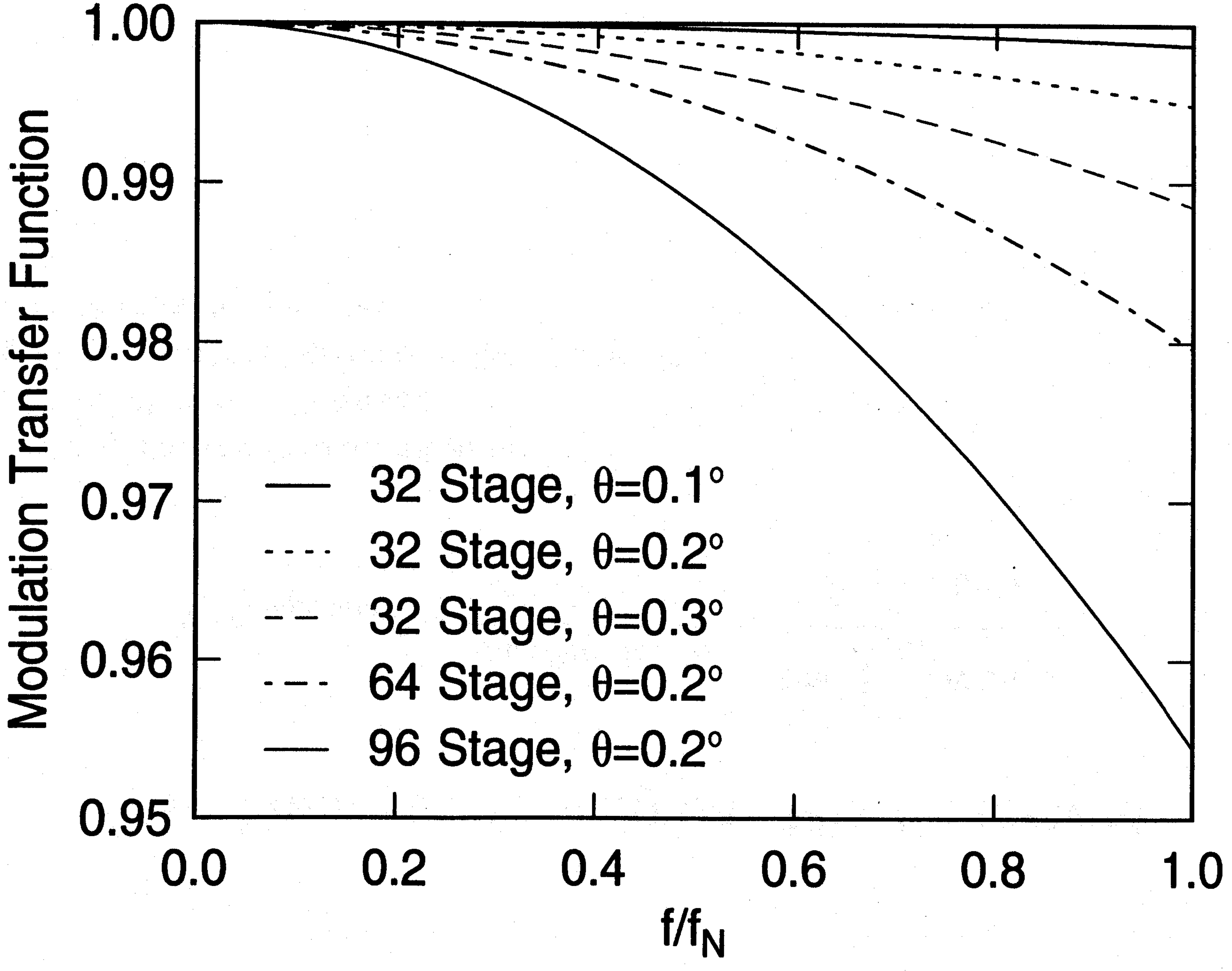
Clocking Method	f_N	$L_{aperture}$	$L_{discrete}$
2 phase, 4 electrodes, overlapping or non-overlapping clock (2 moves)	$1/8\ell$	4ℓ	$4\ell/2$
3 phase, 3 electrodes, non-overlapping clock (3 moves)	$1/6\ell$	3ℓ	$3\ell/3$
3 phase, 3 electrodes, overlapping clock (6 moves)	$1/6\ell$	3ℓ	$3\ell/6$
4 phase, 4 electrodes, non-overlapping clock (4 moves)	$1/8\ell$	4ℓ	$4\ell/4$
4 phase, 4 electrodes, overlapping clock (8 moves)	$1/8\ell$	4ℓ	$4\ell/8$
4 phase, 8 electrodes, ripple clock	$1/2\ell$	ℓ	$4\ell/3$
8 phase, 16 electrodes, ripple clock	$1/2\ell$	ℓ	$8\ell/7$


Modulation Transfer Function
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.1
0.2
0.3
0.4
0.5
1/Minimum Electrode Length (1 / ℓ)
4ϕ ripple
8ϕ ripple
2ϕ
4ϕ, 4 moves
4ϕ, 8 moves
3ϕ, 3 moves
3ϕ, 6 moves

MTF Loss due to Angular Mis-Alignment

$$MTF_{alignment}(f) = \frac{\sin(\pi f N p_x \tan\theta)}{\pi f N p_x \tan\theta} = \frac{\sin(\frac{\pi}{2}\frac{f}{f_N} N \tan\theta)}{\frac{\pi}{2}\frac{f}{f_N} N \tan\theta} \qquad (10)$$

θ = angular mis-alignment angle
N = number of TDI stages
p_x = pixel center spacing in the x-direction
f_N = Nyquist frequency


Modulation Transfer Function
1.00
0.99
0.98
0.97
0.96
0.95
0.0
0.2
0.4
0.6
0.8
1.0
f/f_N
32 Stage, θ=0.1°
32 Stage, θ=0.2°
32 Stage, θ=0.3°
64 Stage, θ=0.2°
96 Stage, θ=0.2°

Choice of Clocking Method

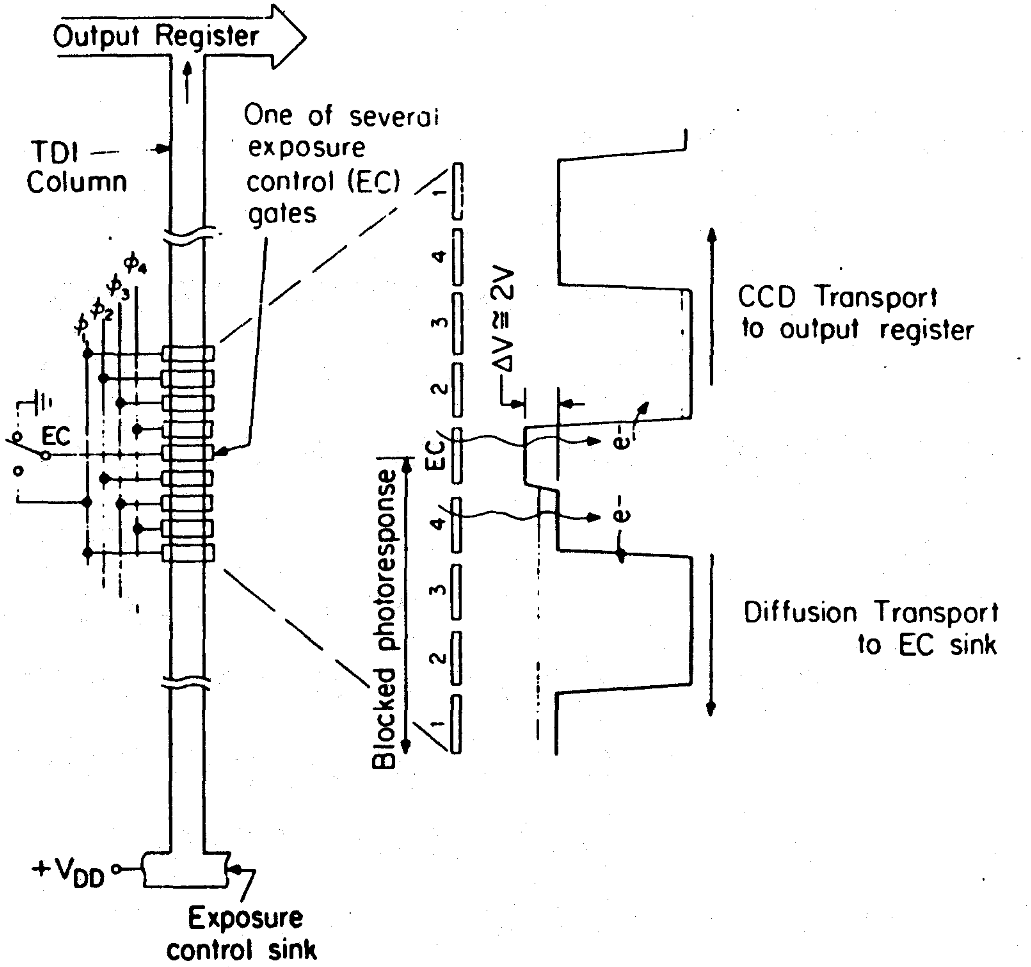
- Charge capacity [Barbe, *IEEE Proc.* 1975]
  - 4 phase, largest capacity
- MTF loss [Farrier & Dyck, *IEEE–ED,* 1980]
  - 4 phase, 8 moves
- Ripple clock [Angle, *Conf. CCD Appl.* 1978]
  - high Nyquist frequency
  - discrete charge motion
  - higher speed in parallel array required
  - metal–to–poly contact in imaging array
- Technology dependent
  - double or triple poly
  - design ground rule

Sensitivity, Exposure Control

- N–stage TDI increases sensitivity N times

- Electronic exposure control
  - extends dynamic range
  - extra voltage barrier required at exposure control electrode → lose charge capacity
  - diffusive transport of un–used signal limits maximum imaging flux

[Farrier & Dyck, *IEEE–ED,* 1980]



Farrier and Dyck, IEEE ED-27, p.1688 (1980)

Noise, Dynamic Range, S/N Ratio

Parallel array:

1. Interface states trapping noise (SCCD)
2. Bulk trapping noise (BCCD)
3. Dark current shot noise
4. Transfer inefficiency shot noise
5. Photon shot noise

Serial register:

1. Interface states trapping noise (SCCD)
2. Bulk trapping noise (BCCD)
3. Dark current shot noise
4. Transfer inefficiency shot noise

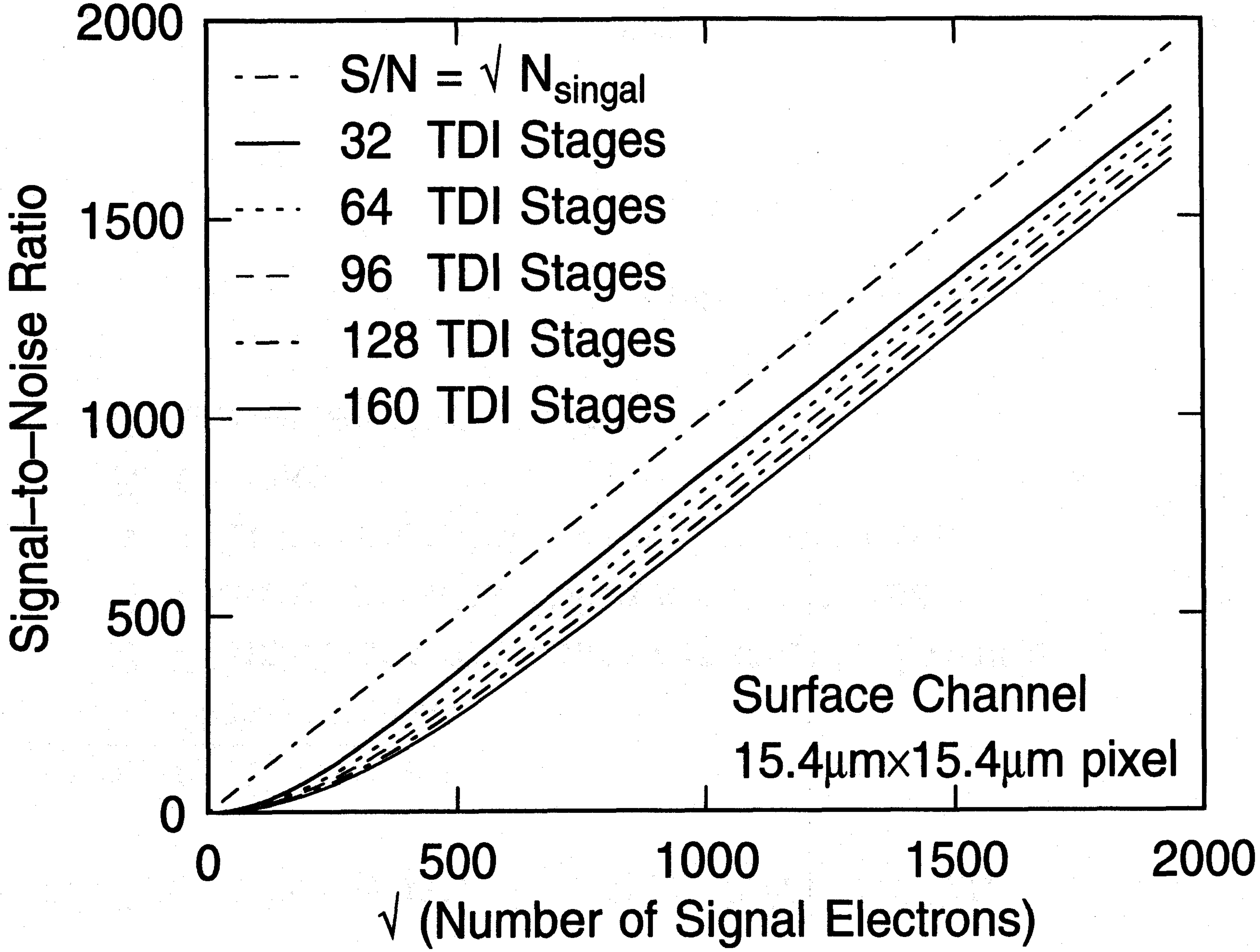
[Carnes & Kosonocky, *RCA Review,* 1972]

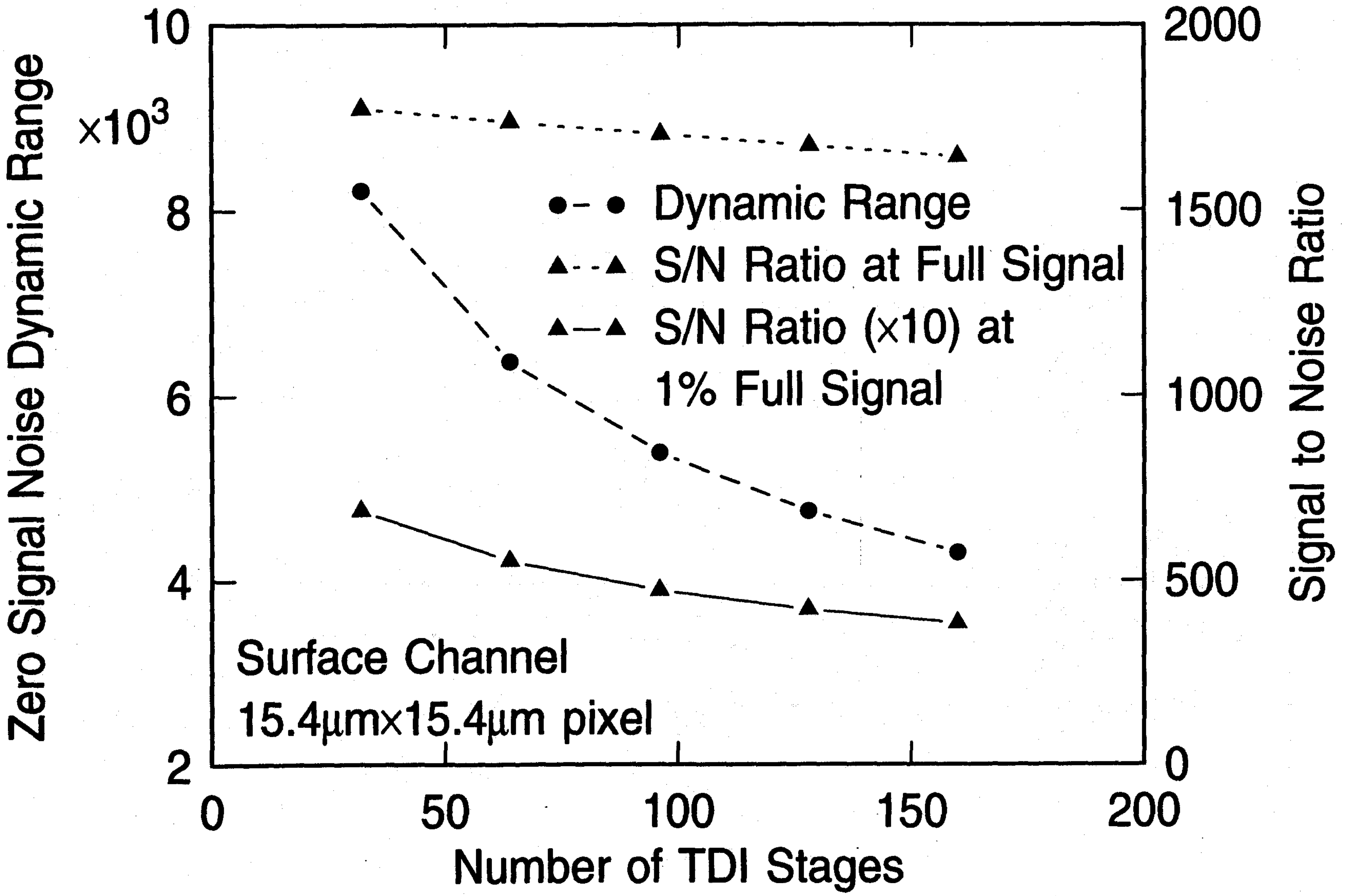
Noise, Dynamic Range, S/N Ratio

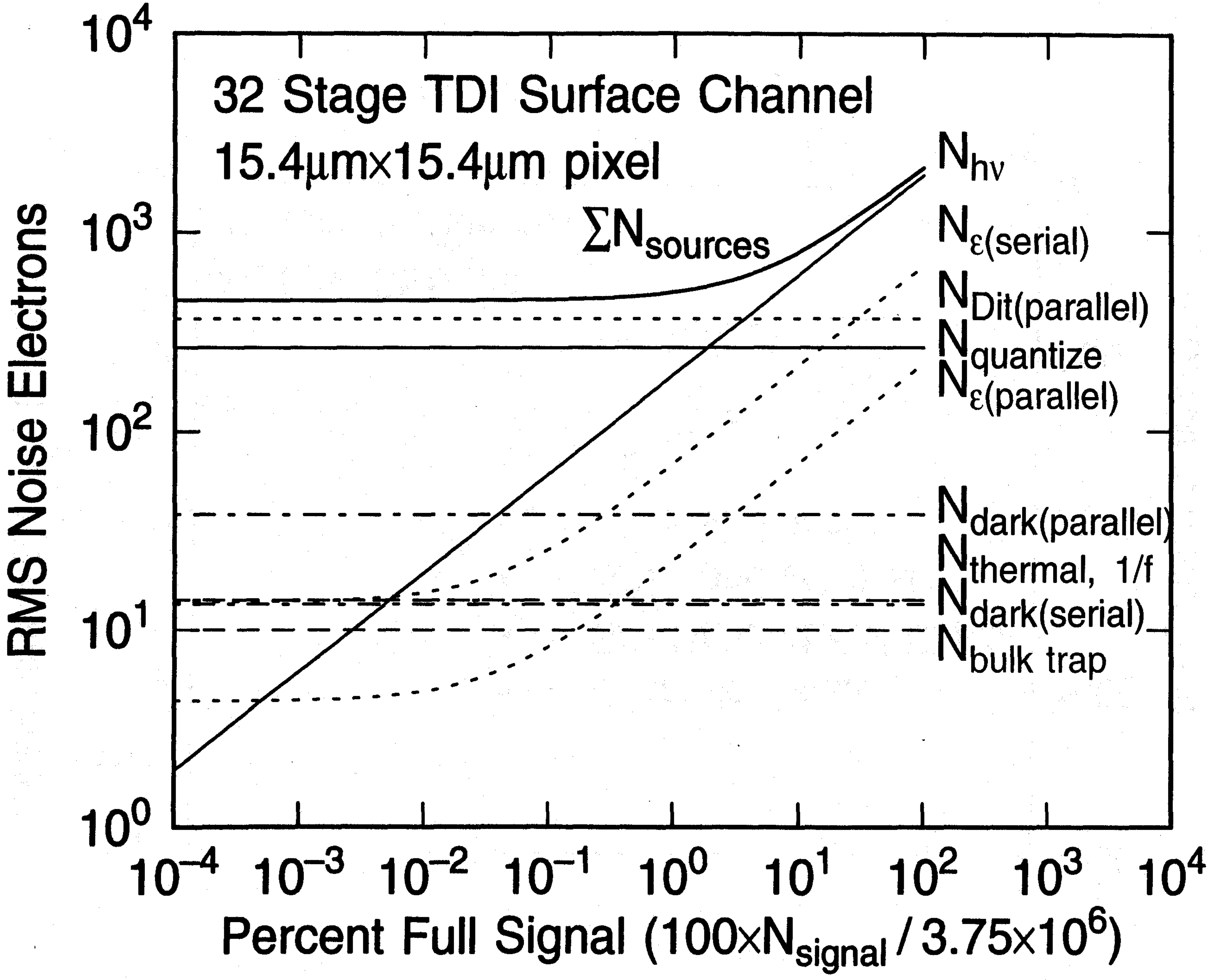
Output structures:

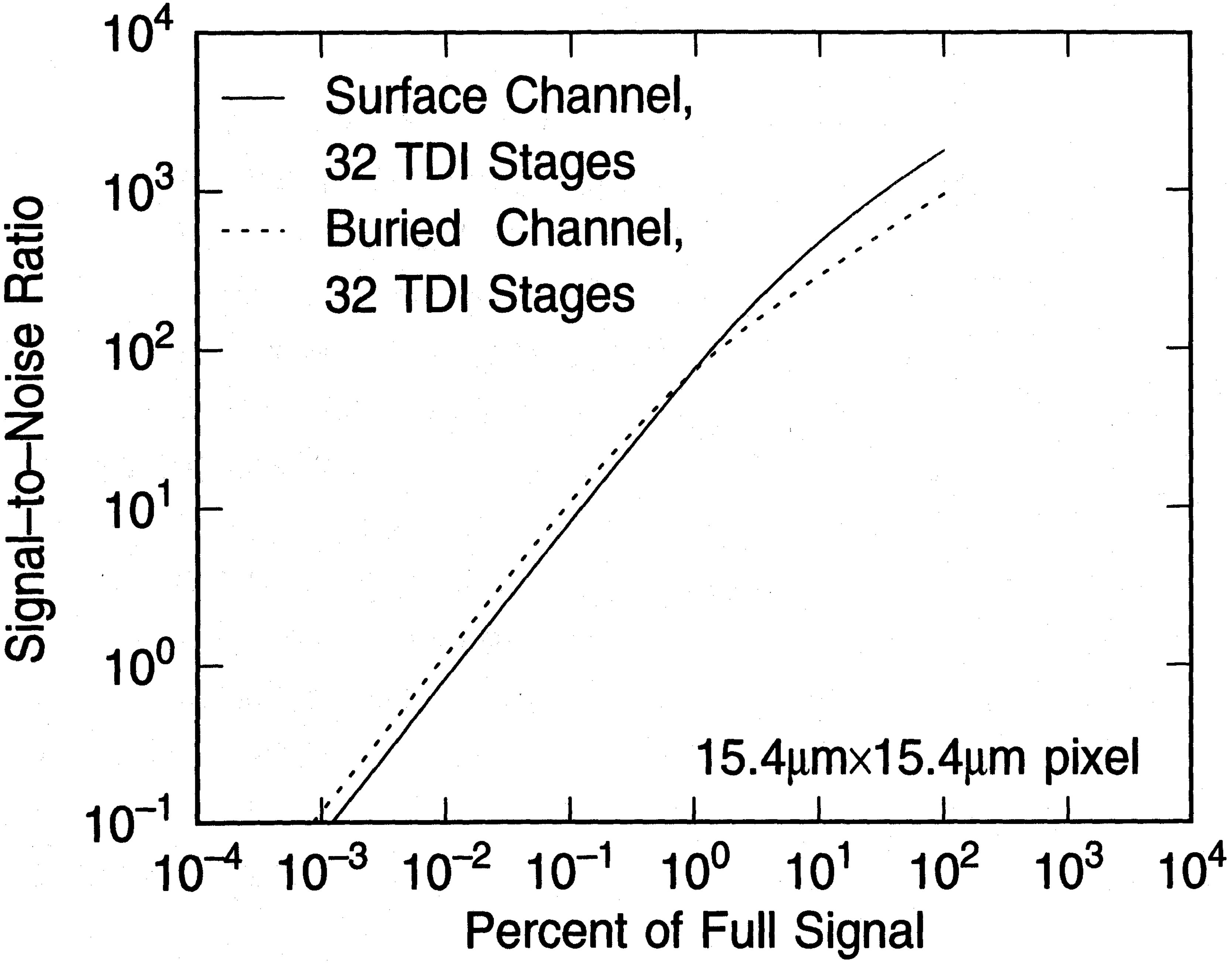
1. Reset noise
2. Output source follower thermal noise
3. Output source follower 1/f noise
4. A/D conversion quantization noise
5. Clocks
6. Other system noise

[White, in *Solid Stage Imaging,* 1975]


2000
1500
1000
500
0
Signal-to-Noise Ratio
0
500
1000
1500
2000
√ (Number of Signal Electrons)
S/N = √ N singal
32 TDI Stages
64 TDI Stages
96 TDI Stages
128 TDI Stages
160 TDI Stages
Surface Channel
15.4μm×15.4μm pixel

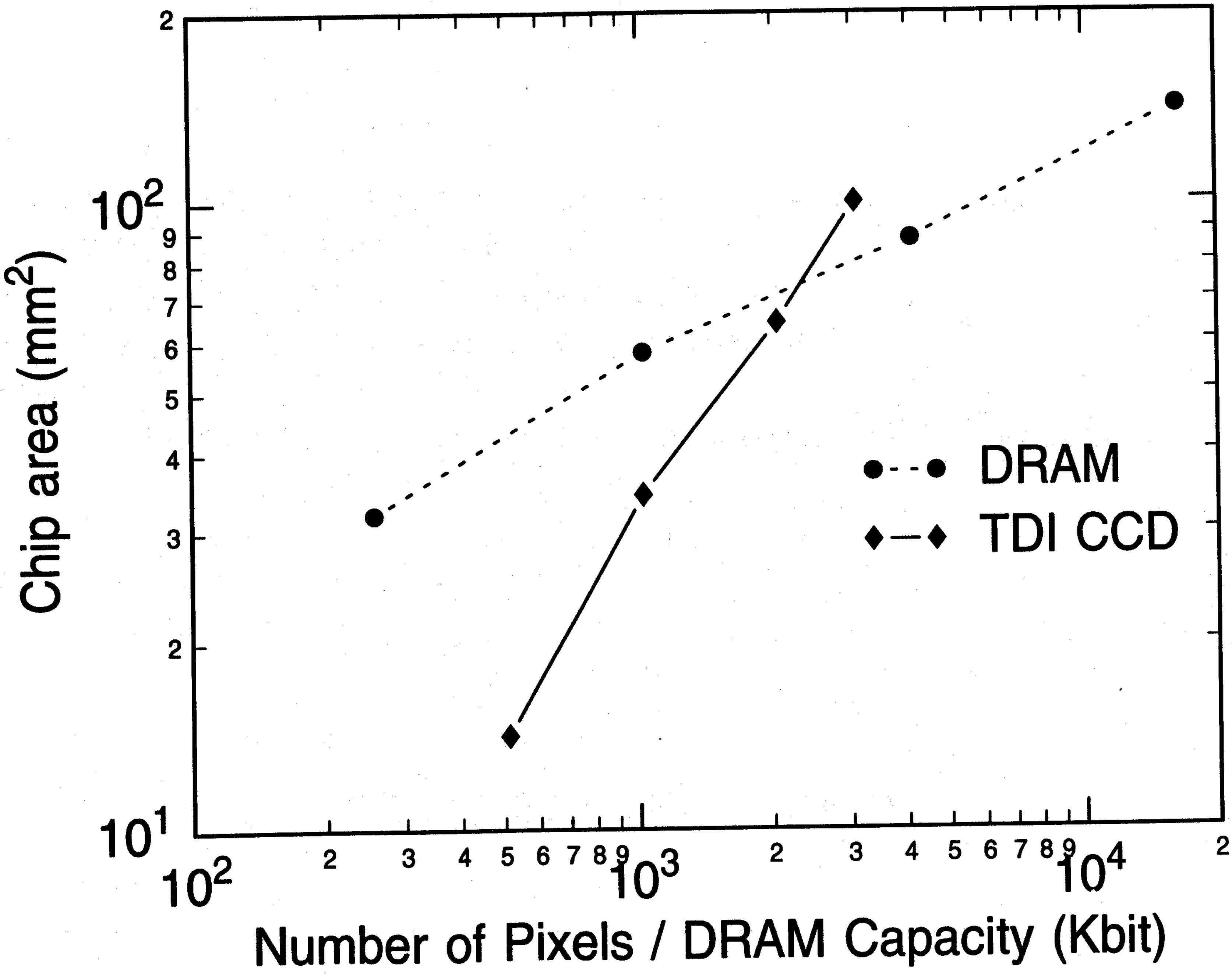

Zero Signal Noise Dynamic Range
×10^3
10
8
6
4
2
Signal to Noise Ratio
2000
1500
1000
500
0
0
50
100
150
200
Number of TDI Stages
●- - ● Dynamic Range
▲- - -▲ S/N Ratio at Full Signal
▲—▲ S/N Ratio (×10) at 1% Full Signal
Surface Channel
15.4µm×15.4µm pixel


32 Stage TDI Surface Channel
15.4μm×15.4μm pixel
$\Sigma N_{sources}$
$N_{h\nu}$
$N_{\varepsilon(serial)}$
$N_{Dit(parallel)}$
$N_{quantize}$
$N_{\varepsilon(parallel)}$
$N_{dark(parallel)}$
$N_{thermal,\ 1/f}$
$N_{dark(serial)}$
$N_{bulk\ trap}$
10^4
10^3
10^2
10^1
10^0
RMS Noise Electrons
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^0
10^1
10^2
10^3
10^4
Percent Full Signal ($100 \times N_{signal} / 3.75 \times 10^6$)


10^4
10^3
10^2
10^1
10^0
10^−1
Signal–to–Noise Ratio
Surface Channel, 32 TDI Stages
Buried Channel, 32 TDI Stages
15.4μm×15.4μm pixel
10^−4
10^−3
10^−2
10^−1
10^0
10^1
10^2
10^3
10^4
Percent of Full Signal

Pixel Size

- Large pixel
  - charge capacity
  - signal–to–noise ratio
  - carrier diffusion MTF loss
  - MTF of optics
- Small pixel
  - chip size, yield
  - mechanical, handling
  - compact optical system
  - RC charging time
  - limited stepper field size (~ 25–30 mm) → 1X lithography ←→ relaxed ground rules



Chip area (mm^2)
2
10^2
9
8
7
6
5
4
3
2
10^1
10^2
2
3
4
5
6
7
8
9
10^3
2
3
4
5
6
7
8
9
10^4
2
Number of Pixels / DRAM Capacity (Kbit)
●- - -● DRAM
◆—◆ TDI CCD

Spectral Responsivity

$$\begin{aligned} R(\lambda) &= \frac{q\eta(\lambda)}{hc/\lambda} \quad [A/W] \\ &= \frac{q\eta(\lambda)}{hc/\lambda} \times \beta_v \times A_p \quad [VJ^{-1}cm^{-2}] \end{aligned} \tag{11}$$

hc/λ ($\simeq 1.24154 \times 10^{-6} q/\lambda$, where $q =$ electron charge) $=$ energy per photon

h ($= 6.62617 \times 10^{-23} J\, s$) $=$ the Planck's constant

c ($= 2.99792 \times 10^{10} cm\, s^{-1}$) $=$ velocity of light

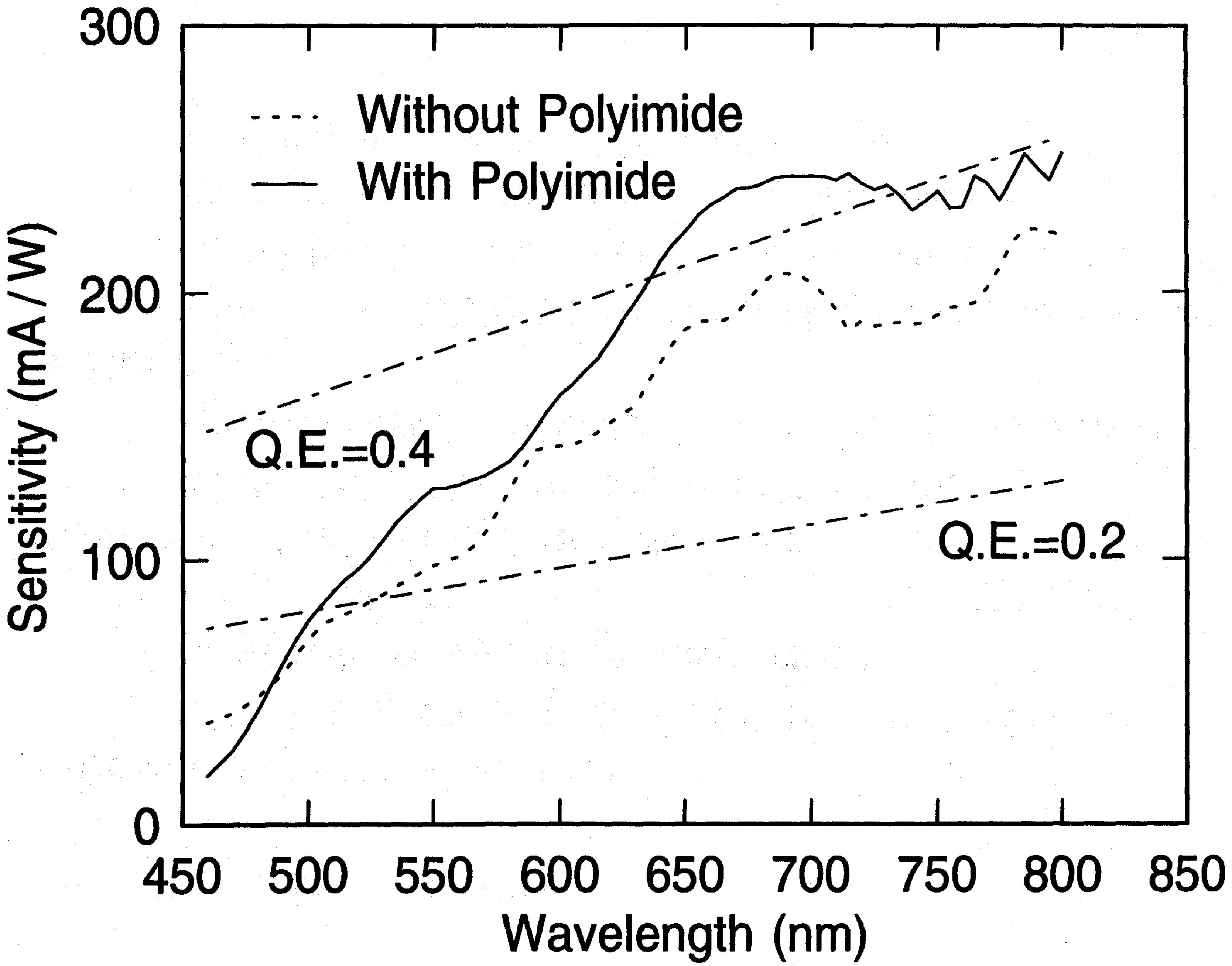
λ is the wavelength of light ffl$[m]$

β_v is the conversion coefficient of the output detection node $[V/C]$

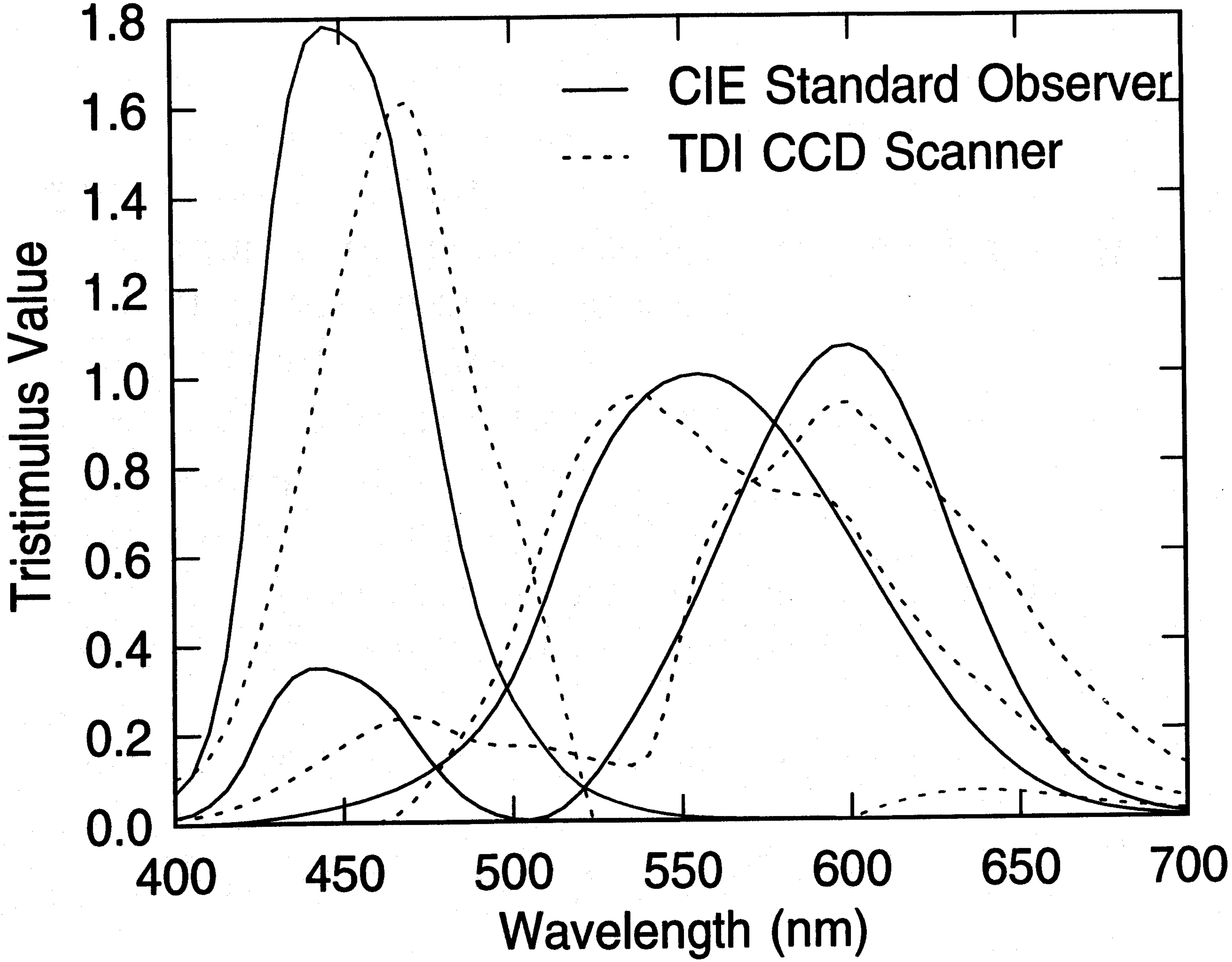
$A_p =$ photo-element area $[cm^{-2}]$

Spectral Response

- Low quantum efficiency
  - $\eta(\lambda) \sim 0.2$ to 0.4 for $400\text{nm} < \lambda < 700\text{nm}$
  - absorption by polysilicon gate ($\lambda < 500\text{nm}$) [Lee, *IEDM*, 1983]
- Non–uniform spectral response
  - multiple dielectric layer reflection, interference effects [v.d. Wiele in *Solid State Imaging*, 75]
- Solutions:
  - tailor dielectric layer material refractive index and thickness, $\eta \sim 0.5$ [Dyck & Wight, *IEEE–ED*, 1977]
  - thin polysilicon gate [Anagnostopoulos, *CICC*, 1980]
  - indium tin oxide (ITO) gate [Thompson, *IEEE–ED*, 1978]



Without Polyimide
With Polyimide
Q.E.=0.4
Q.E.=0.2
Sensitivity (mA / W)
300
200
100
0
450
500
550
600
650
700
750
800
850
Wavelength (nm)



CIE Standard Observer
TDI CCD Scanner
Tristimulus Value
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
400
450
500
550
600
650
700
Wavelength (nm)

Comparison with Photodiode Array

- Similar applications and system design

Photodiode Linear Array Advantages:

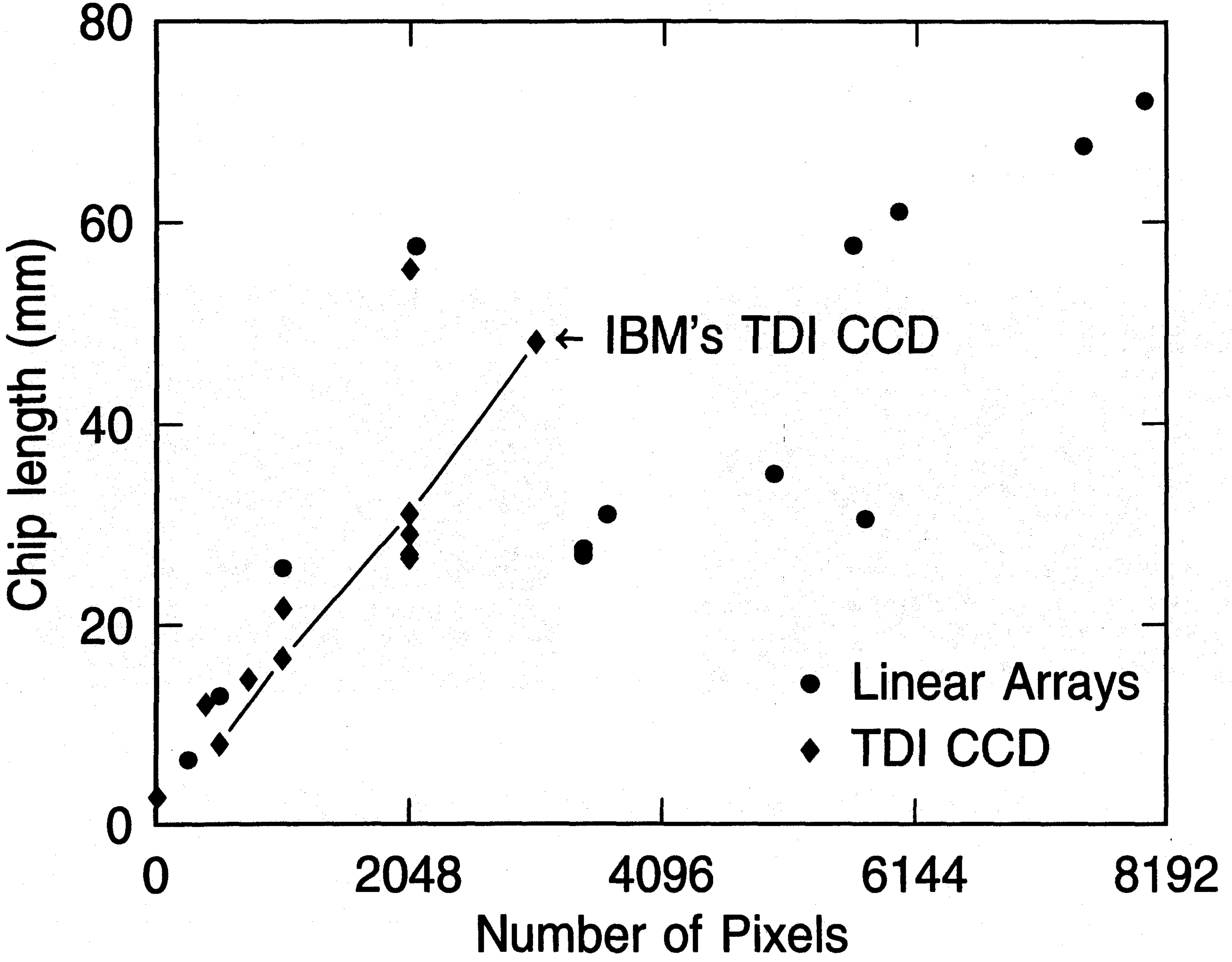
1. bilinear architecture → more pixels/line
2. smooth spectral response
3. smaller chip size
4. stop–and–scan possible

TDI CCD Advantages:

1. uniform pixel responsivity
2. high sensitivity: high speed, low illumination

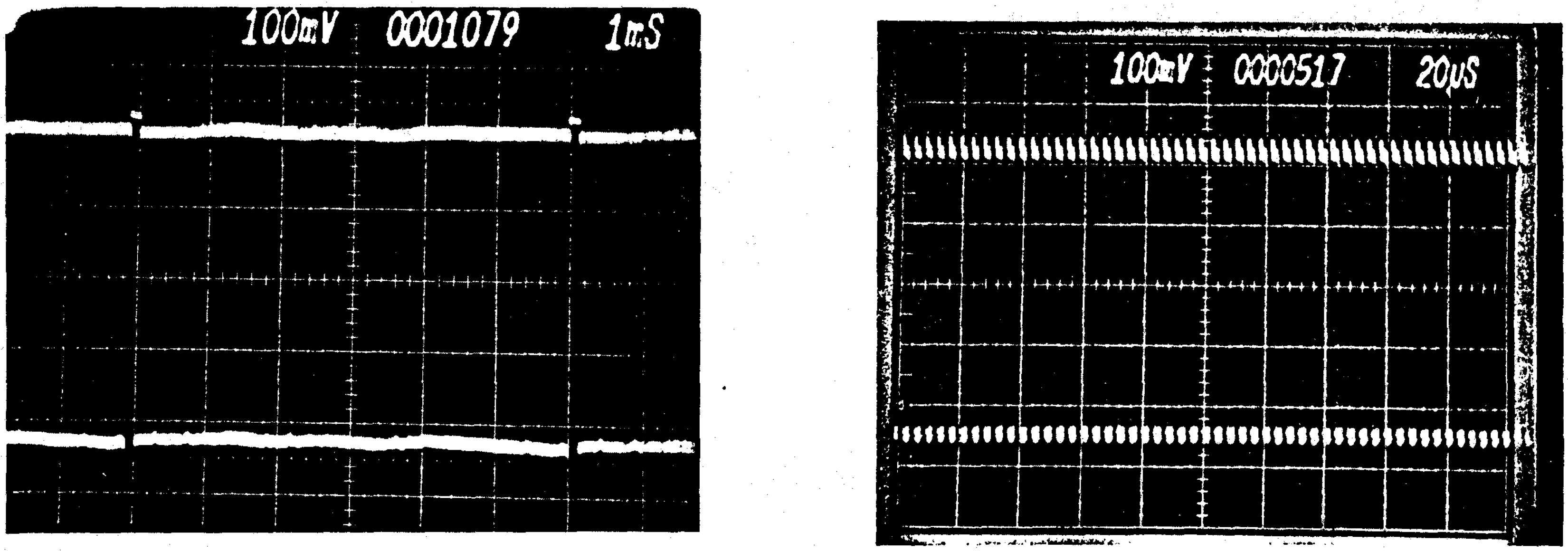
Speed comparison:

1. irradiance required for fixed S/N & line time
2. line time required for fixed S/N & irradiance



80
60
40
20
0
Chip length (mm)
0
2048
4096
6144
8192
Number of Pixels
← IBM's TDI CCD
● Linear Arrays
♦ TDI CCD

TDI CCD Photoresponse Uniformity

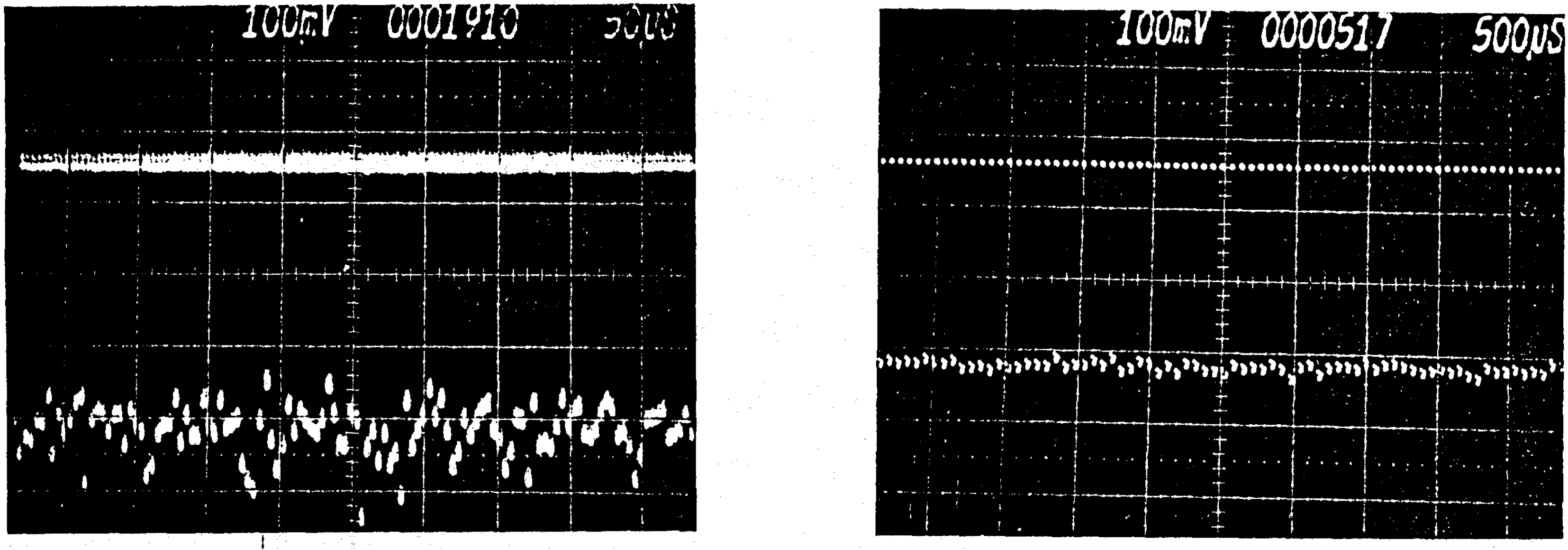


(a) Full scan line

(b) Detail of about 50 cycles

Schlig, IBM J. Research and Development, (1991)

TDI CCD Dark Current Uniformity



(a) Frame transfer mode

(b) TDI mode

Schlig, IBM J. Research and Development, (1991)

IBM's Family of TDI CCD

- Parallel array: surface channel
  - max. charge capacity, S/N at moderate signal
- Serial register: buried channel
  - speed, transfer efficiency
- Four phase, 8 moves clock
  - max. charge capacity, min. MTF loss
- In–line tapped output
  - increase effective data rate
- Floating diffusion output
- 32 to 64 TDI stages
  - ~ 10X to 20X sensitivity improvement
  - maximize MTF and device yield

Device	Architecture	Features and Applications
TDI-2S	512 × 32-stage, 1 output port, 20MHz pixel rate.	10-15 sec./page, office ambient illumination, for optical character recognition.
TDI-2	2048 × 32-stage, 1 output port, 20MHz pixel rate.	0.8 to 1.5 sec./page, flat-bed scanner, 240 pels/inch for A4 document.
TDI-3	1024 × 32-stage, 8 output ports, 96MHz pixel rate, electronic exposure control of 1*X* and 32*X* sensitivity.	350 document-inch/sec (40 Federal Reserve Bank Cheques per second) at 250W, f/2.8, 240 pels/inch.

TDI-4	3072 × 32-stage, 2 output ports, 24MHz pixel rate	1-2 page/sec., camera type scanner for museum artwork and high resolution scanning.
TDI-5	3072 × 64-stage, 2 output ports, 24MHz pixel rate	1-2 page/sec., camera type scanner for museum artwork and high resolution scanning.

Table 3. Device characteristics of the family of TDI CCD designed and fabricated at IBM.

Trends, Major Development Issues

- More pixels/line, high resolution
- 400 pel/in for A4 size → 3456 pixels
- Lithography, chip size
- Small pixel vs. charge capacity
- Color imaging
- Colorimetric ← smooth spectral response
- One–pass color scan, on–chip color
- Blue scan too slow

Conclusions

- TDI CCD device design and applications reviewed

- TDI CCD complements photodiode linear array

- New applications requires TDI CCD
  - high speed batch scanning (banking)
  - low illumination scanning (museum art object)
  - high uniformity, high S/N for good gray scale required for subsequent color processing