

**A Review
of
Photo Detector Elements
for
Interline CCD**

**T. H. Lee and B. C. Burkey
Eastman Kodak Company
Rochester, NY 14650-2008**

Outline

Introduction

Photo Capacitor

np Junction Photodiode

Photoconductor Layers

p+np Multiple Junction Photodiode

Problems and Issues of Photo Detector Elements

Lag

Charge Capacity

Photo Response

Blooming control

Electronic Shutter

Crosstalk and Smear

Non-linearity

Dark current and Noise

Operation of p - n Junction Photodetectors in a Photon Flux Integrating Mode

GENE P. WECKLER, MEMBER, IEEE

Abstract—A technique for operating a p - n junction photodiode in a photon flux integration mode is described. In this mode the p - n junction is charged to a reverse voltage (less than its breakdown voltage) and then open-circuited. The voltage across the junction, with zero incident illumination, will decay at a rate that is independent of junction area. Time constants in the order of seconds may be achieved with silicon planar structures at room temperature. Under illumination, the rate of decay of charge depends linearly on the intensity of the incident illumination, so that the total charge removed is proportional to the time integral of illumination.

Operation of p - n junction photodiodes is analyzed for this mode and boundary conditions are established. A practical structure utilizing this mode of operation is discussed. This structure makes use of the nearly ideal switch characteristics of an insulated gate field-effect transistor to periodically sample a photodiode. Advantages offered by this device structure include 1) linear dependence of signal charge on light intensity over several orders of magnitude; 2) electronically controllable sensitivity; 3) ease of integration into arrays for image sensing.

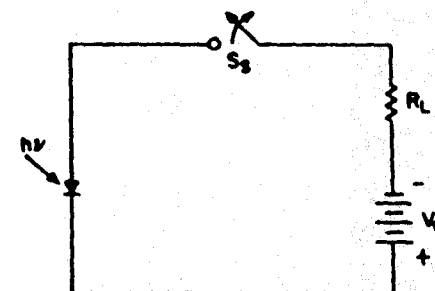


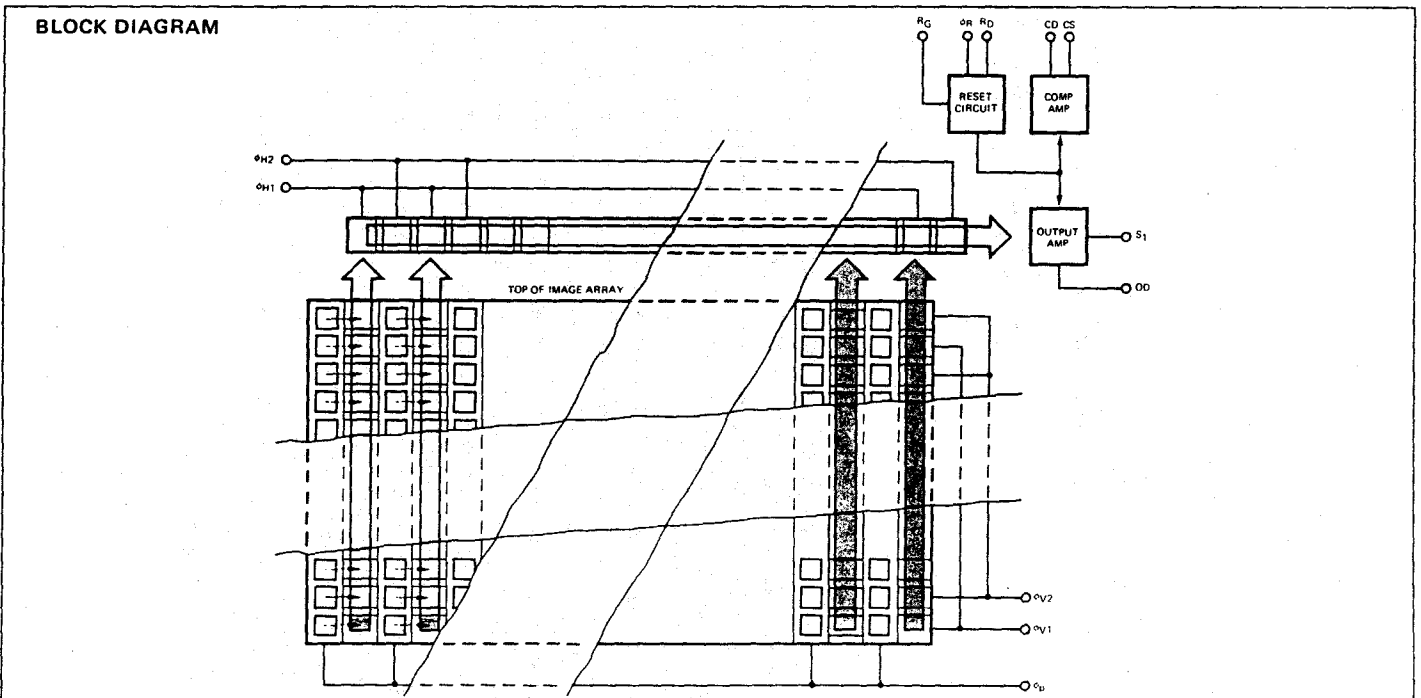
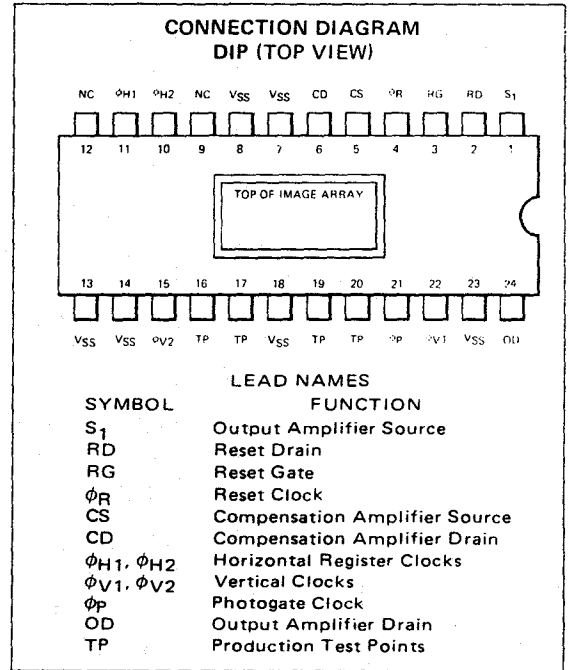
Fig. 1. An idealized circuit for analyzing storage mode operation of a p - n junction diode.

GENERAL DESCRIPTION - The CCD201 is a 2-Phase 10,000-Element Self-Scanning Image Sensor. It uses charge coupled technology with buried channels and ion-implanted barriers. The light sensitive area is a 100 x 100 array of photo elements which provide an image aspect ratio of 4 x 3. The image sensing elements are 1.2 mils x 0.8 mils located on 1.2 mil vertical centers and 1.6 mil horizontal centers.

In addition to the image sensing array, the CCD201 chip includes: 100 columns of 2-phase analog shift registers interdigitated in the photosensor array, a 102-element 2-phase analog output shift register, an output detector/preamplifier and a compensation output amplifier.

The device is packaged in a 24-lead Dual In-Line package with an optical glass window.

- 2-PHASE CLOCK OPERATION
- 100 x 100-ELEMENT ARRAY ON A SINGLE CHIP
- INTERLACED SELF SCANNING
- ALL OPERATING VOLTAGES UNDER 20 V
- ON-CHIP VIDEO PREAMPLIFIER AND COMPENSATION CIRCUIT
- LOW POWER 50 mW TYP
- PACKAGED IN 24-LEAD DIP WITH OPTICAL GLASS WINDOW



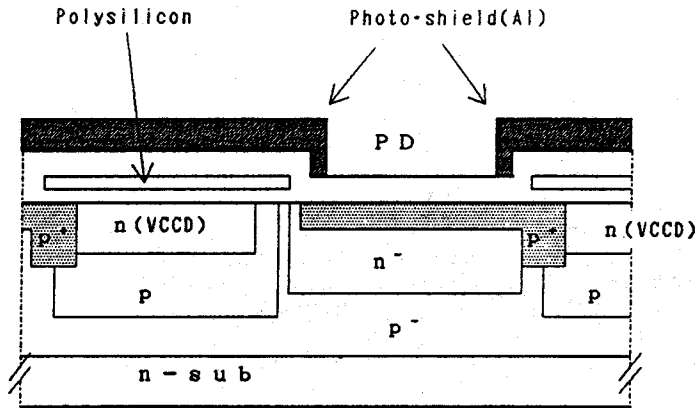


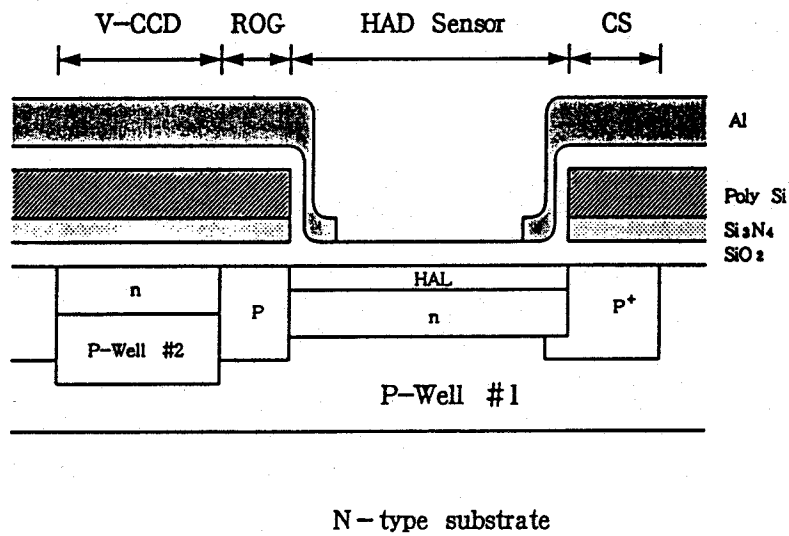
Fig. 5. Cross-sectional view of a unit cell.

Kuriyama et al

IEEE Trans

ED-38

May 1991



Hojo et al

IEEE Trans

ED-38

May 1991

Fig. 3. Schematic cross-sectional view of the unit cell.

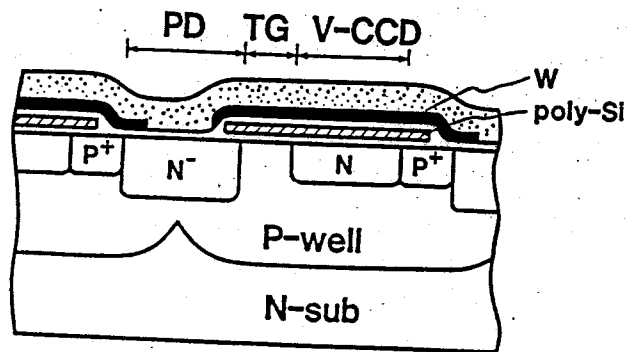


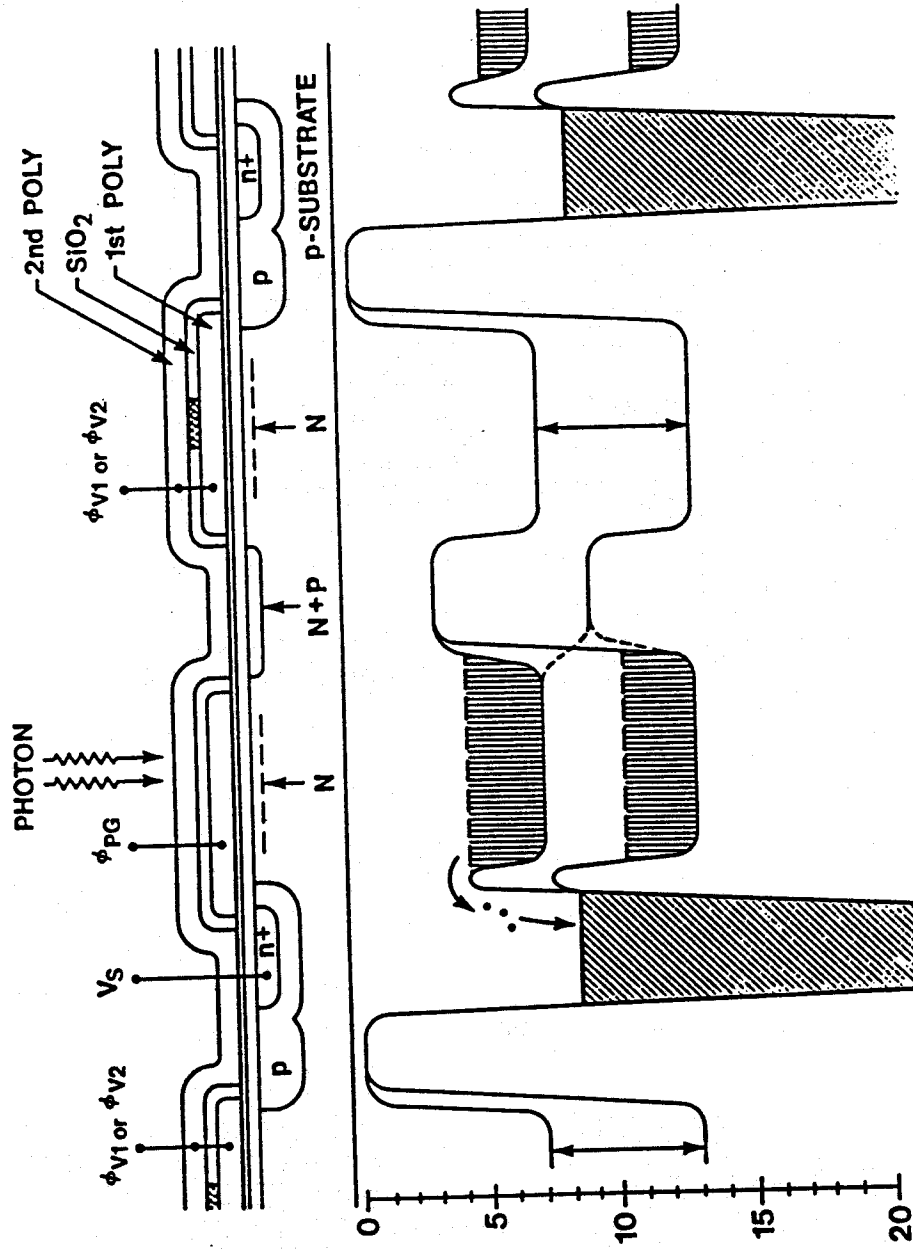
Fig. 5. Cross-sectional view of a unit pixel.

Toyoda et al

IEEE Trans ED-38

May 1991

FIG. 2. PHOTOCELL CROSS-SECTION



TOP AND CROSSSECTIONAL VIEWS OF THE CCD IMAGER

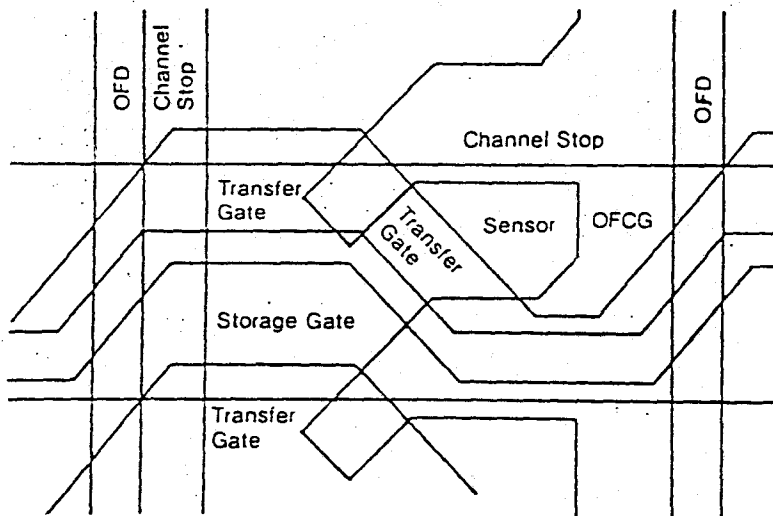


FIG. 5-1 TOP VIEW

OFD: Overflow Drain
 OFCG: Overflow Control Gate

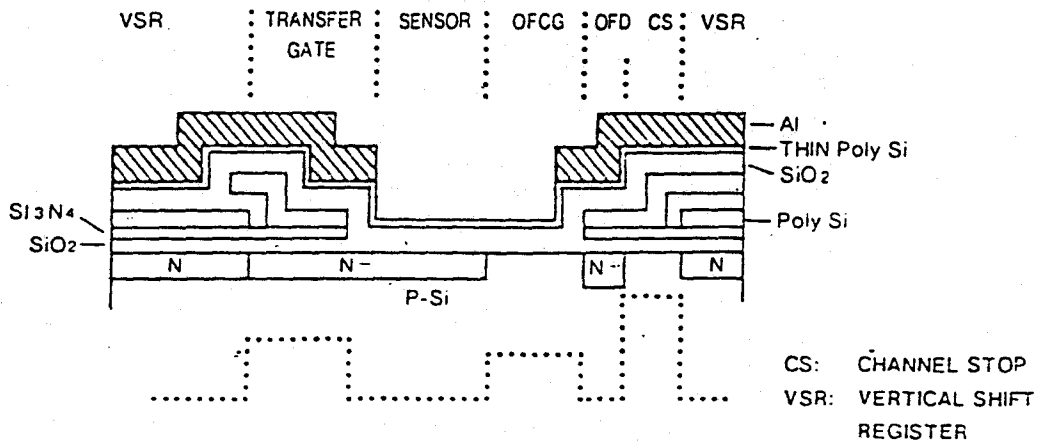


FIG. 5-2 CROSSSECTIONAL VIEW

CS: CHANNEL STOP
 VSR: VERTICAL SHIFT REGISTER

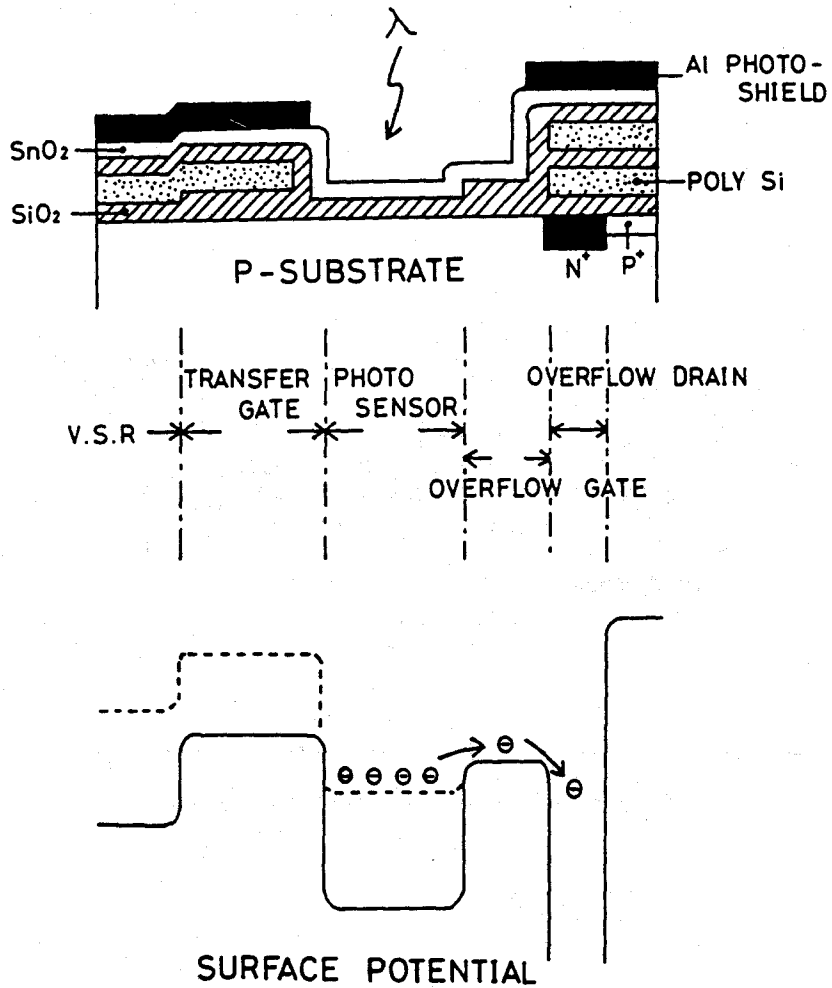


FIGURE 3—Cross sectional view and surface potential of antiblooming system.

Matsumoto et al / SONY

ISSCC 1978

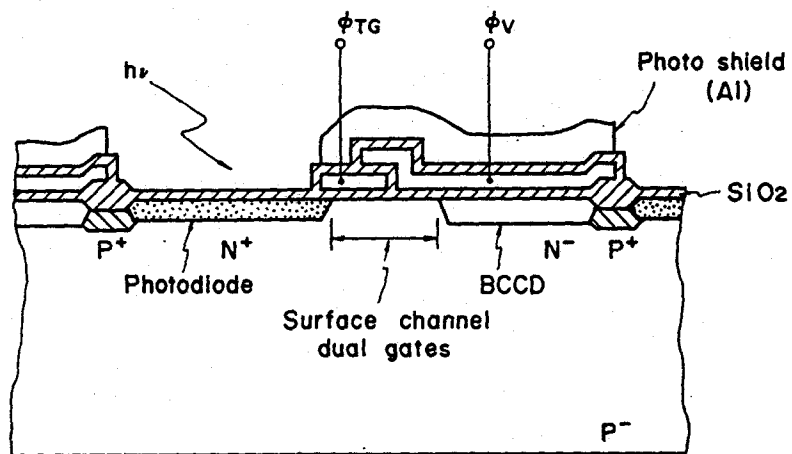
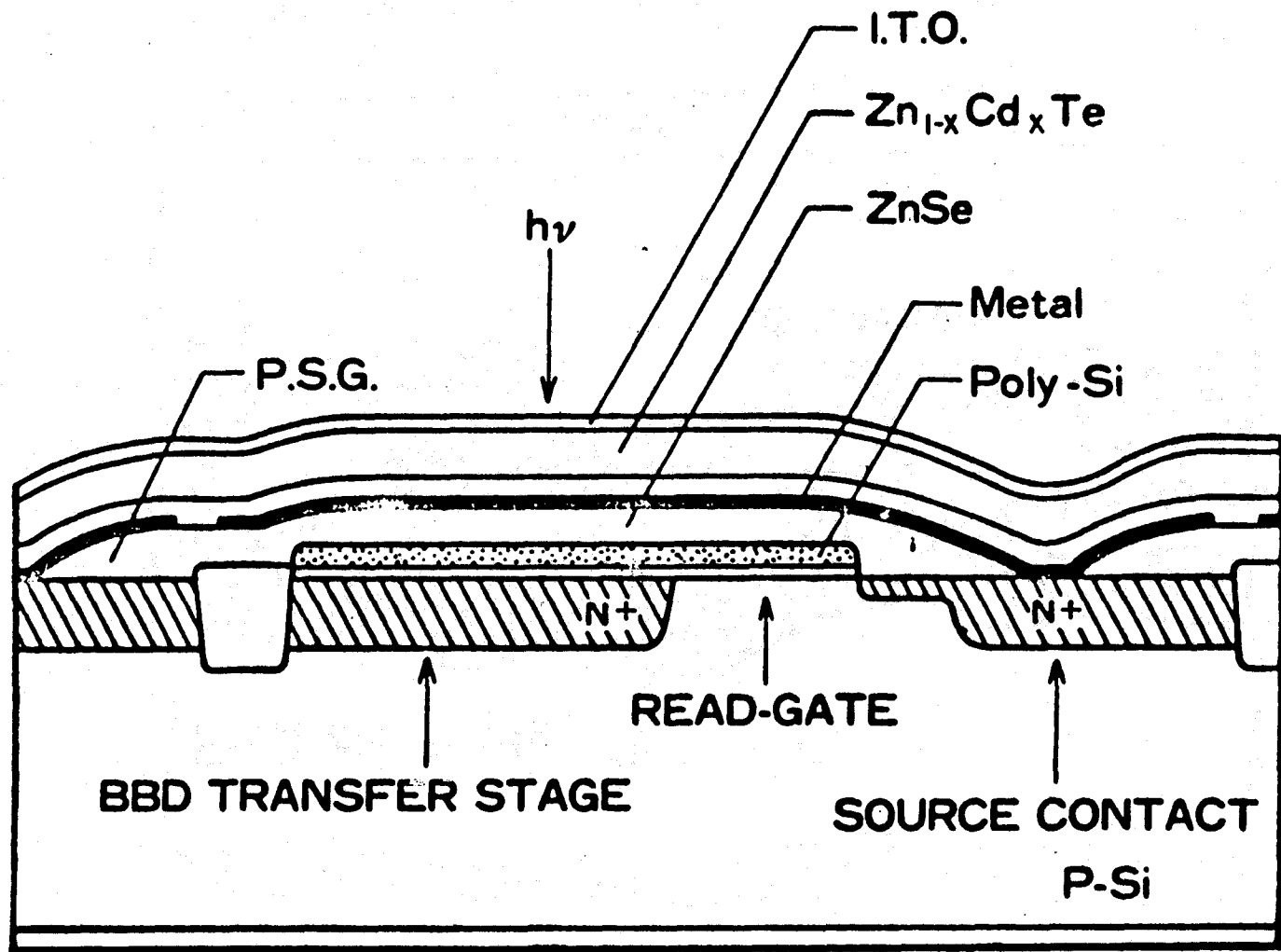


FIGURE 2—Cross sectional view of a unit cell.

Ishihara et al

ISSCC, 1980



Ref. Terui et al
 ISSCC Tech. Digest
 1980 p.34

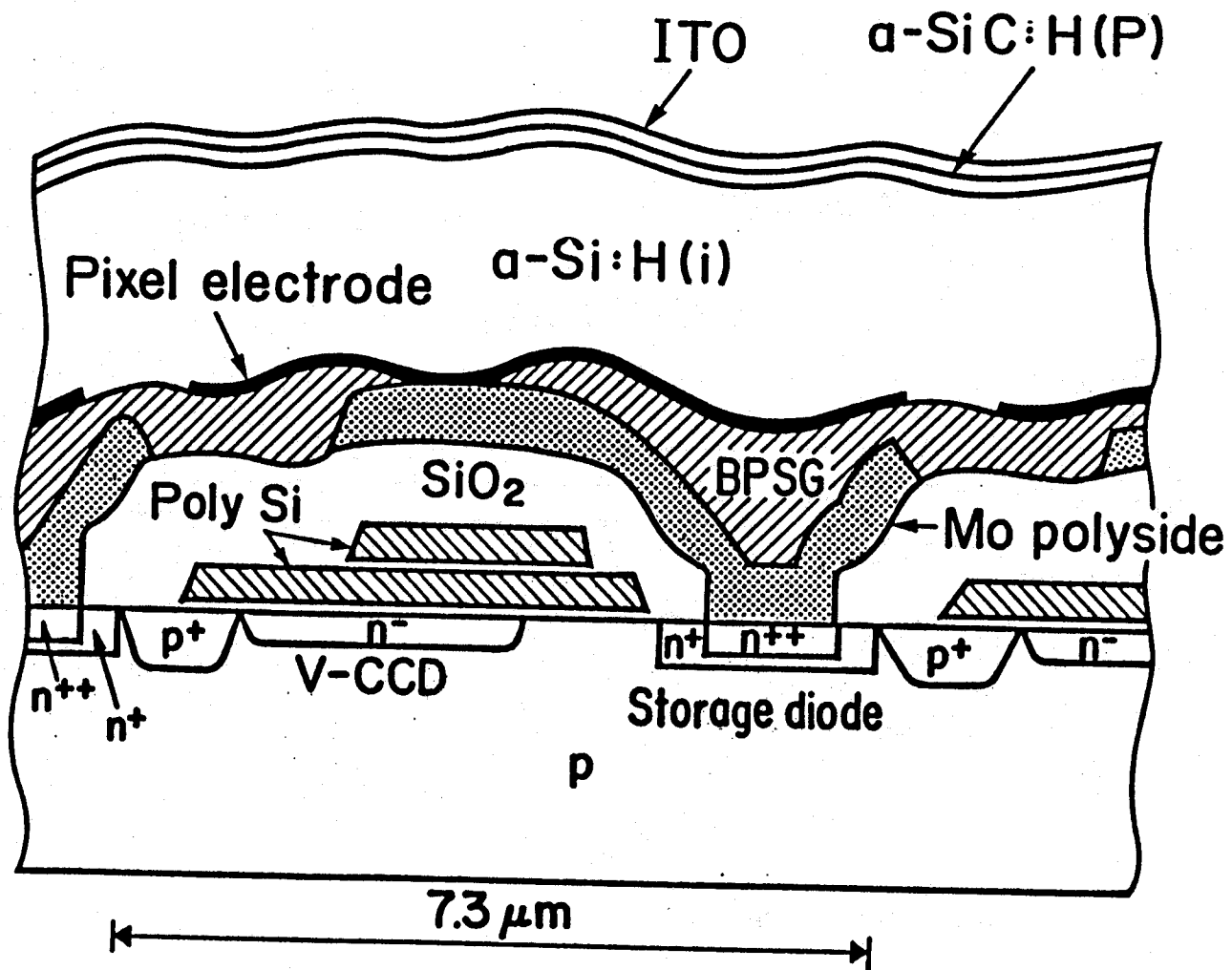
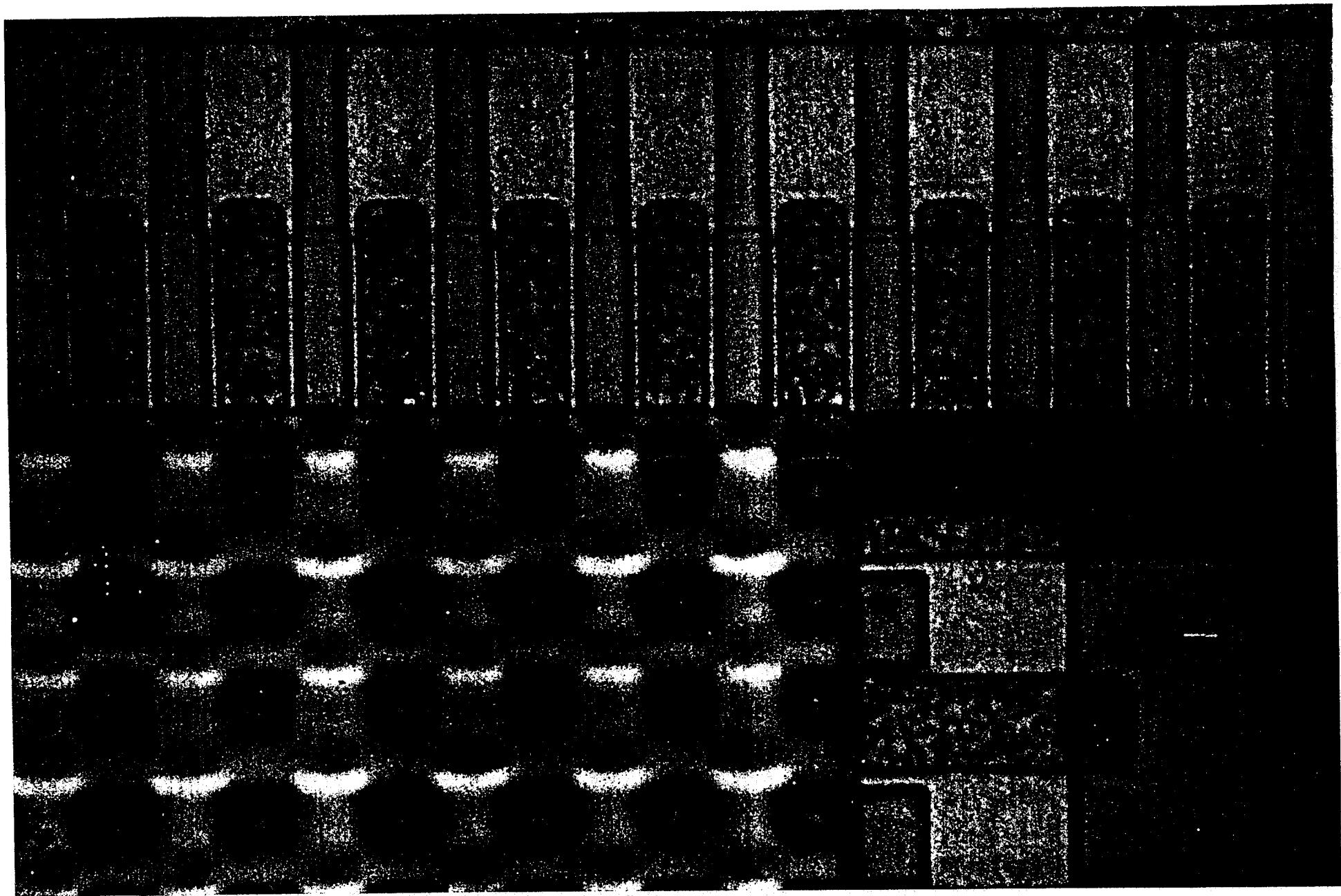
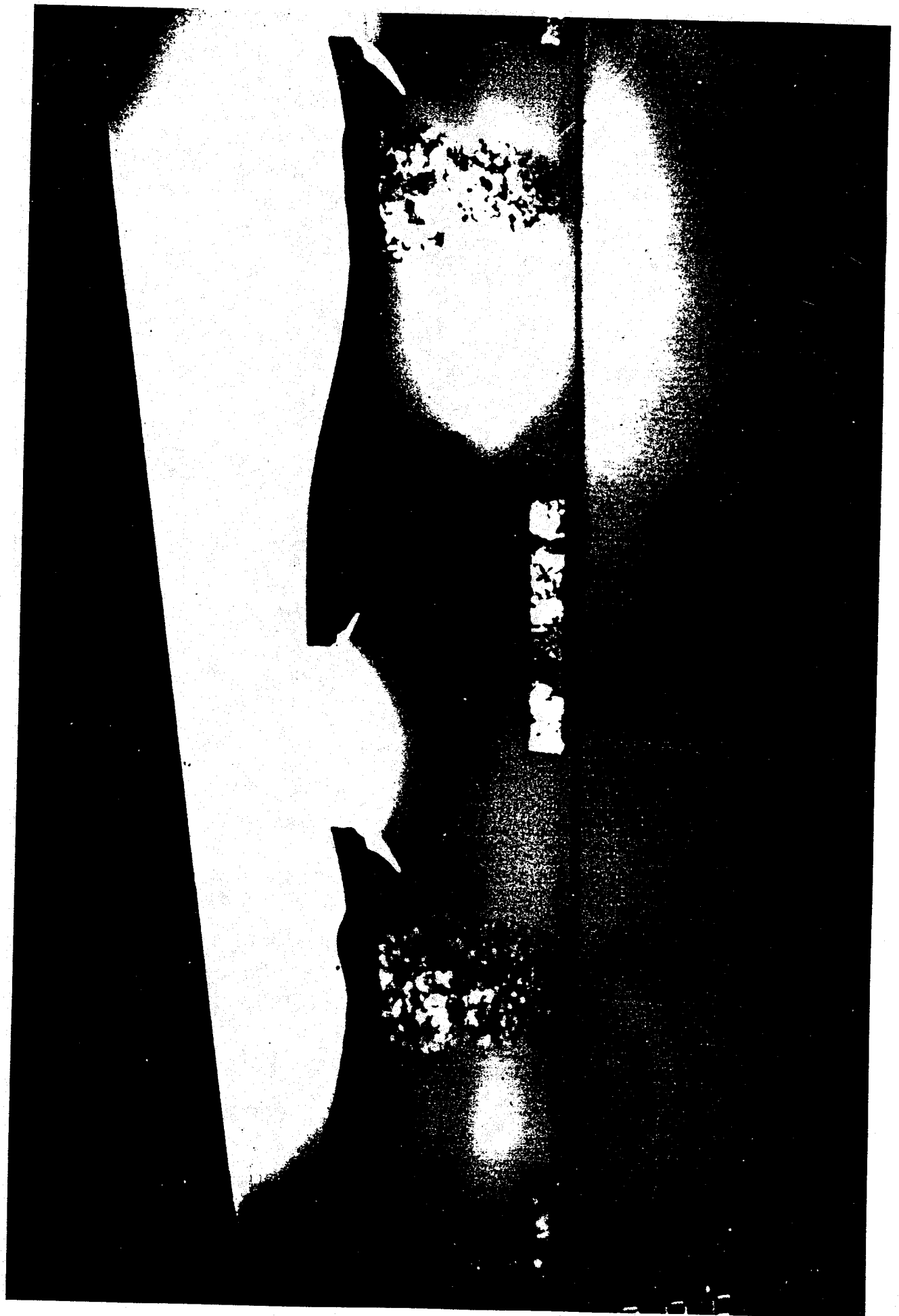


FIGURE 2 Cross section view of unit cell





NO IMAGE LAG PHOTODIODE STRUCTURE IN THE INTERLINE CCD IMAGE SENSOR

Nobukazu Teranishi, Akiyoshi Kohono, Yasuo Ishihara, Eiji Oda and Kouichi Arai

Microelectronics Research Laboratories, Nippon Electric Co., Ltd.

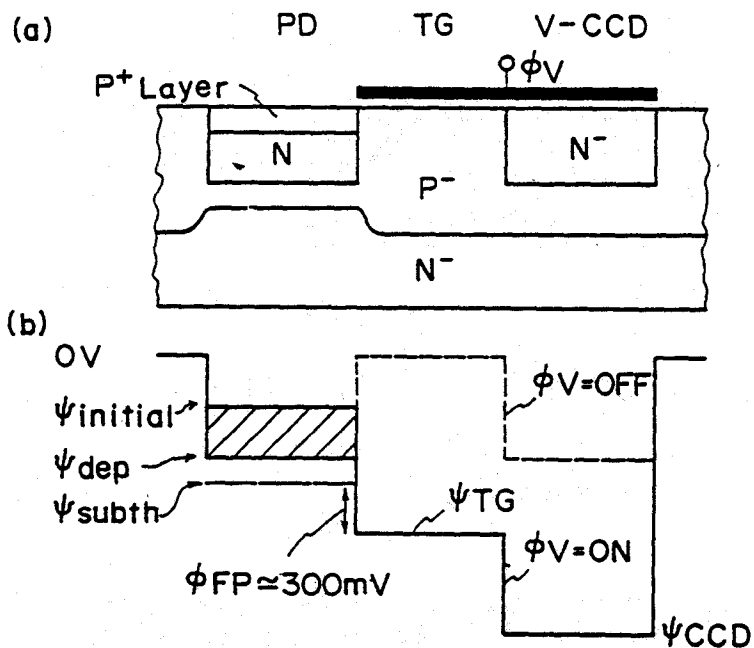


Fig.5. P+NP- structure photodiode
 (a) Unit cell cross sectional view
 (b) Potential profile in a complete transfer mode

THE PINNED PHOTODIODE FOR AN INTERLINE-TRANSFER CCD IMAGE SENSOR

B. C. Burkey, W. C. Chang, J. Littlehale, T. H. Lee,
T. J. Tredwell, J. P. Lavine, E. A. Trabka

Research Laboratories, Eastman Kodak Company
Rochester, New York 14650

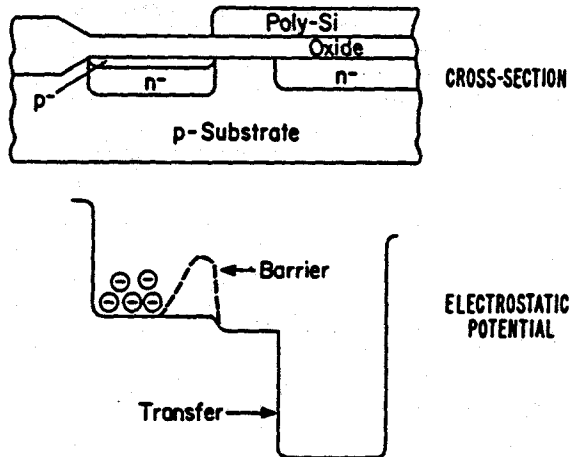
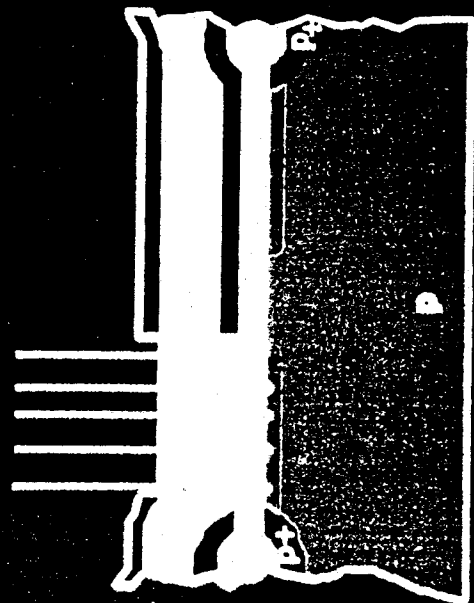


Fig. 8. Image cell schematic indicating a potential barrier at the edge of the transfer gate.

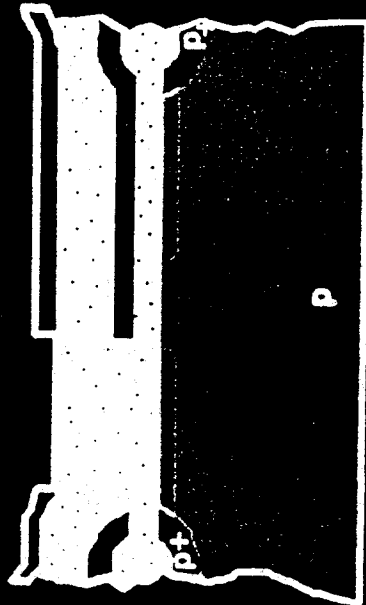
LAG IS DUE TO INCOMPLETE READOUT
OF THE PHOTOSIGNAL FROM A DIODE.

CHARGE LEFT BEHIND IS READ OUT IN
SUBSEQUENT FRAMES, CAUSING GHOST
IMAGES TRAILING MOVING OBJECTS.

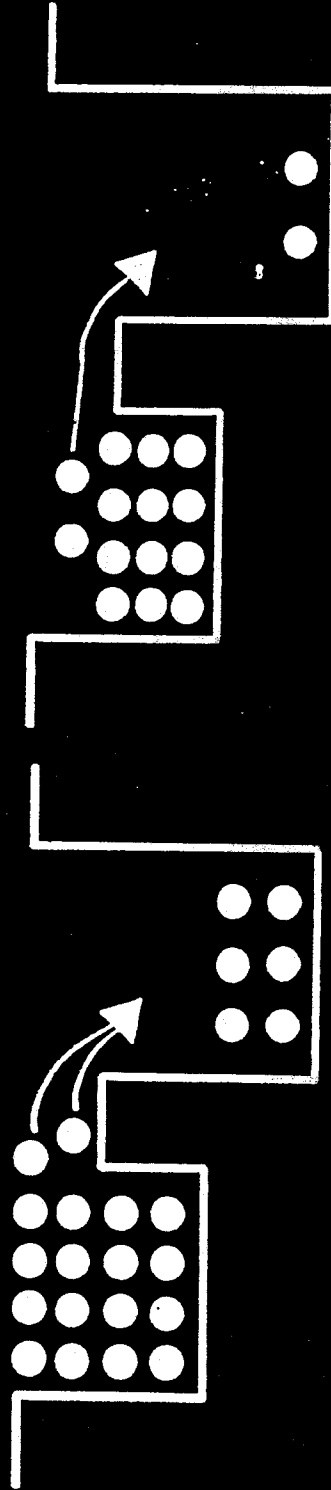
LAG IN CCD IMAGE SENSORS



Frame 1

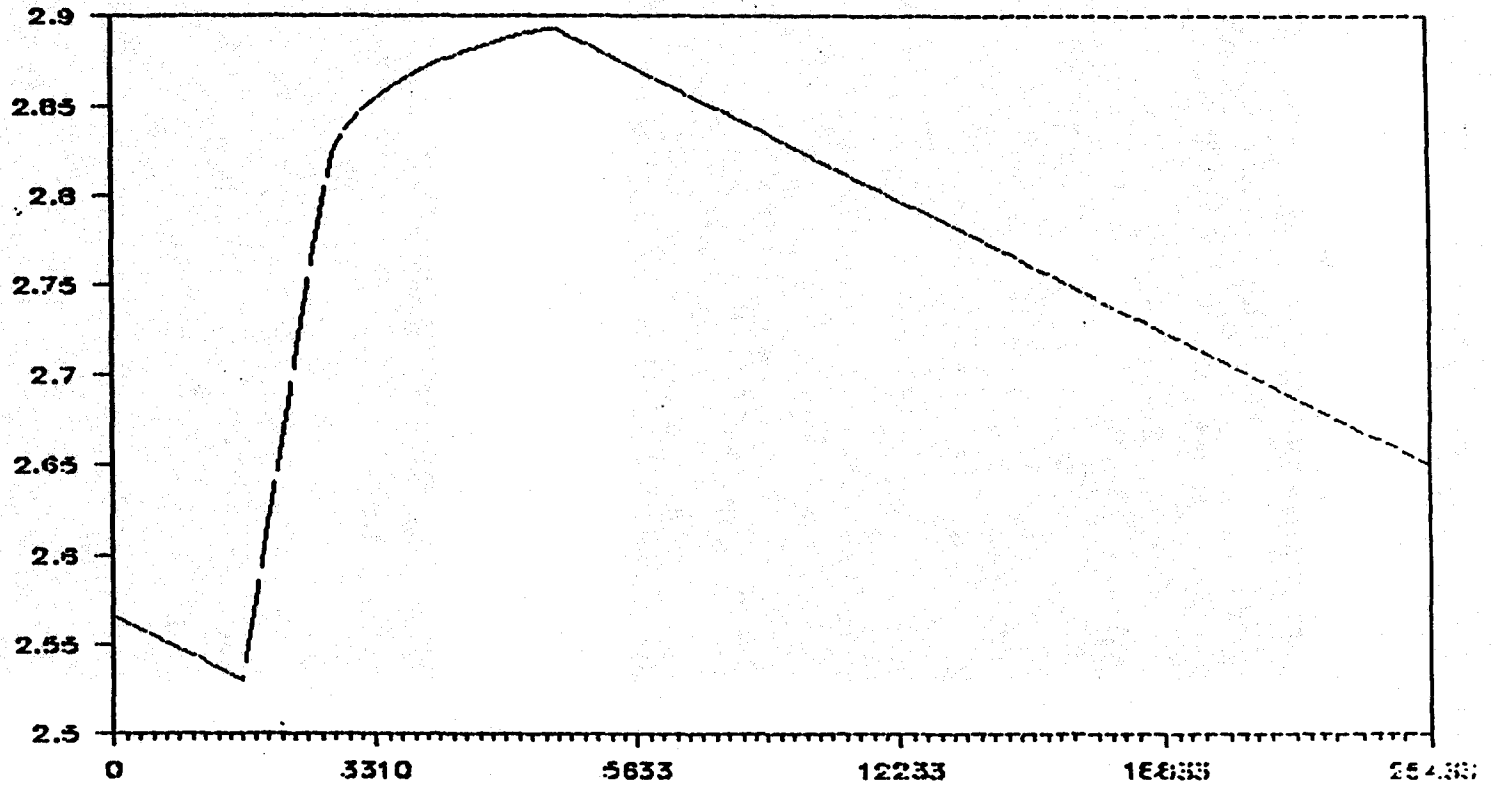


Frame 2



Photodiode Voltage vs Time

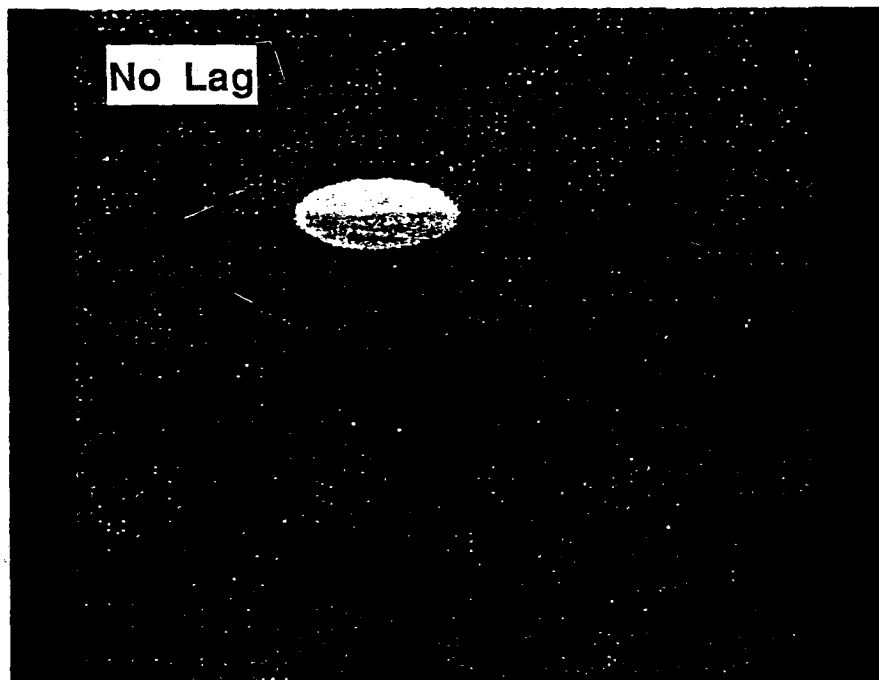
↑
PD
Voltage



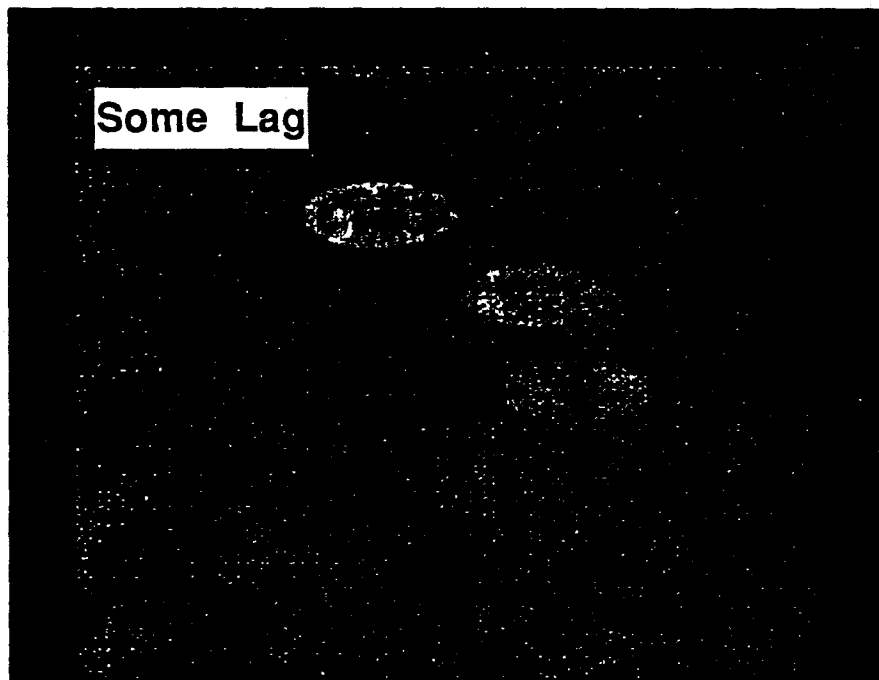
Time →

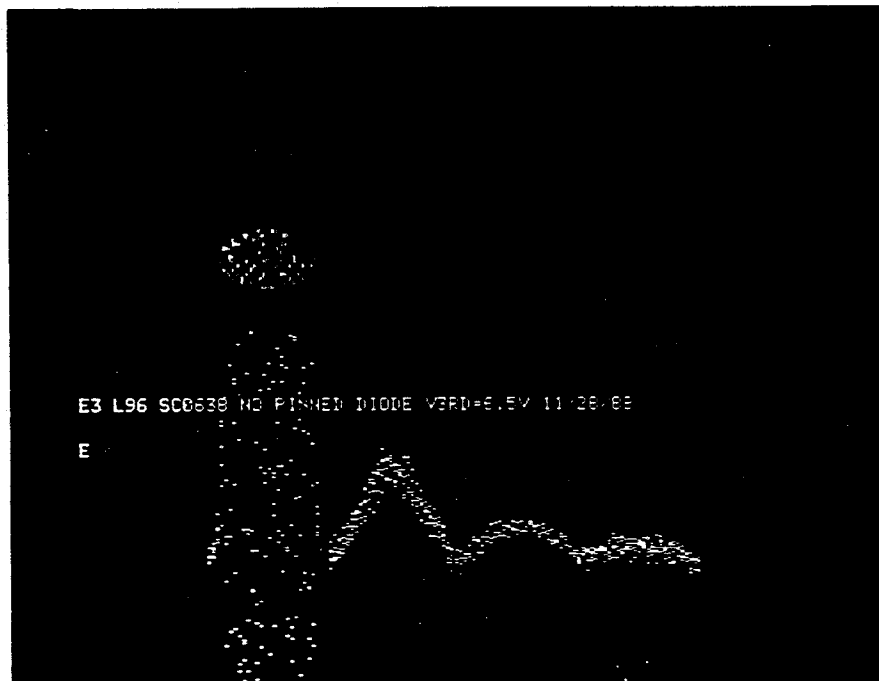
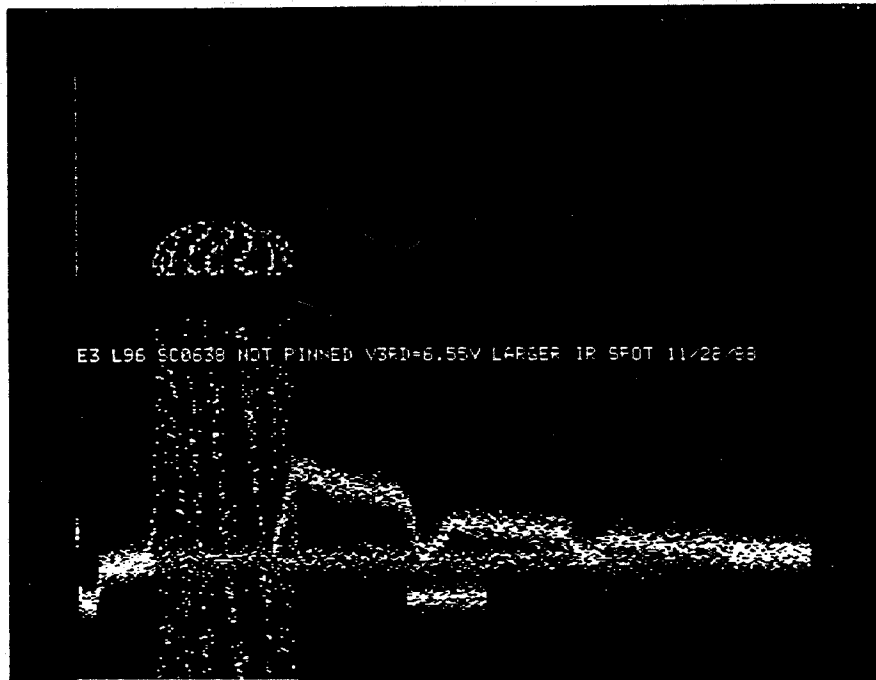
LAG vs CLOCK LEVEL

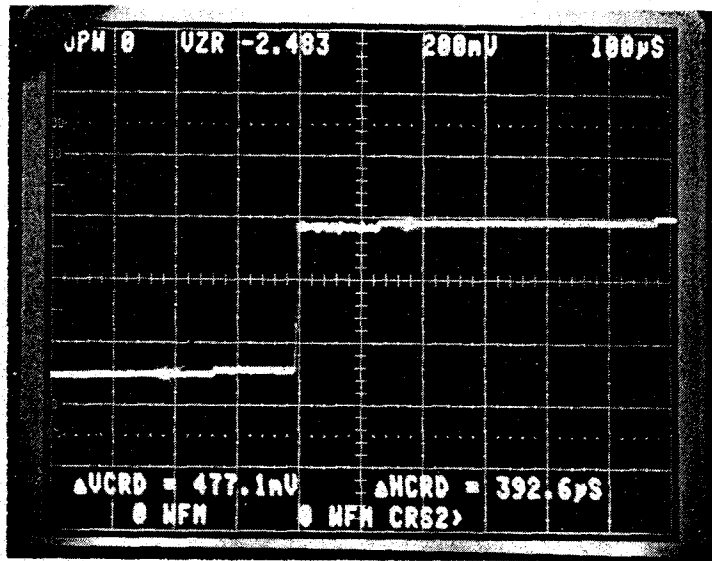
NORMAL CLOCKING
V3RD=10V
NO LAG!



MISADJUST V3RD
TO INDUCE LAG
V3RD=3.4V







Ne output

Cfd=20fF, b=40, No=30, Nsig=37,000e

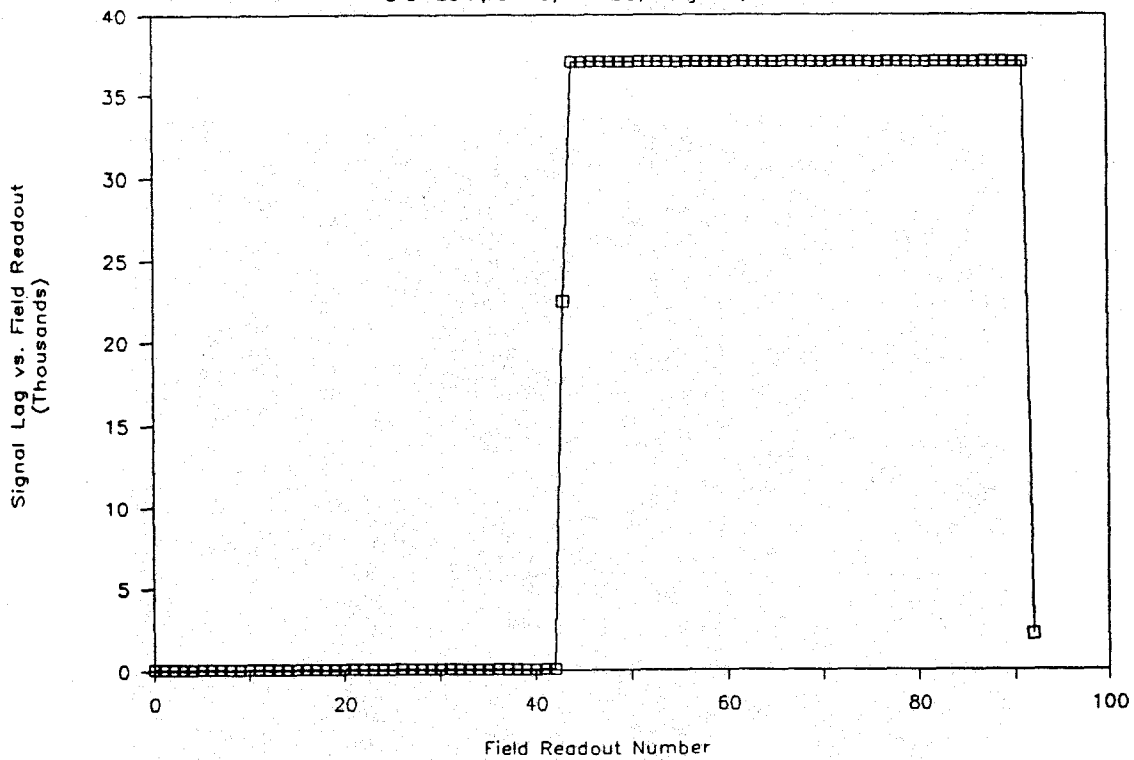
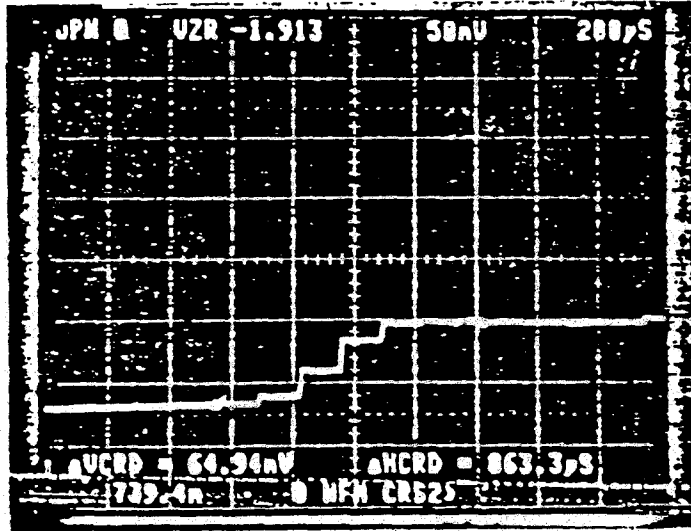


Figure 5-50. Signal lag with unpinned photodiode — 37,000 electrons signal. Run 3C-01.



Ne output

Cfd=20fF, b=40, No=30, Nsig=5,000e

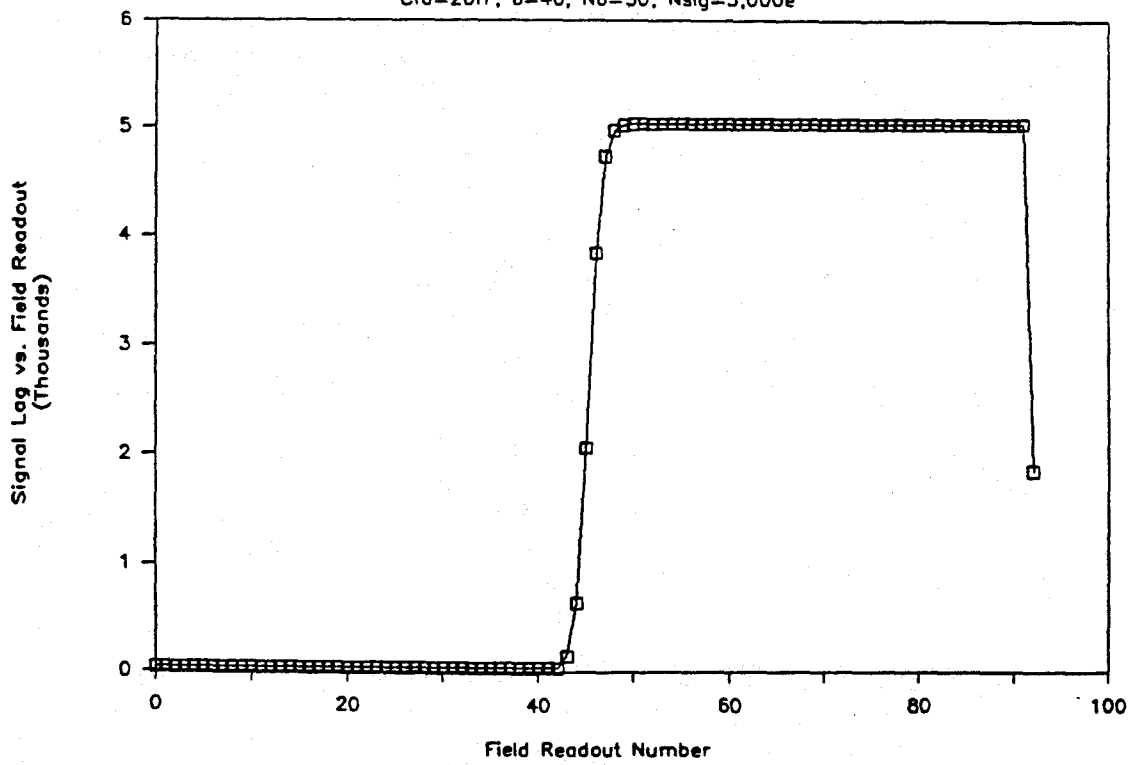
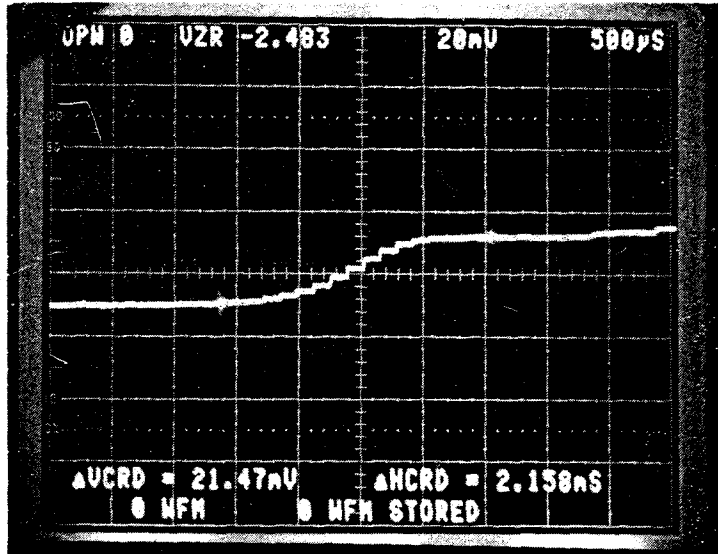


Figure 5-51. Signal lag with unpinned photodiode — 5,000 electrons signal. Run 3C-01.



Ne output

Cfd=20fF, b=40, No=30, Nsig=1,200e

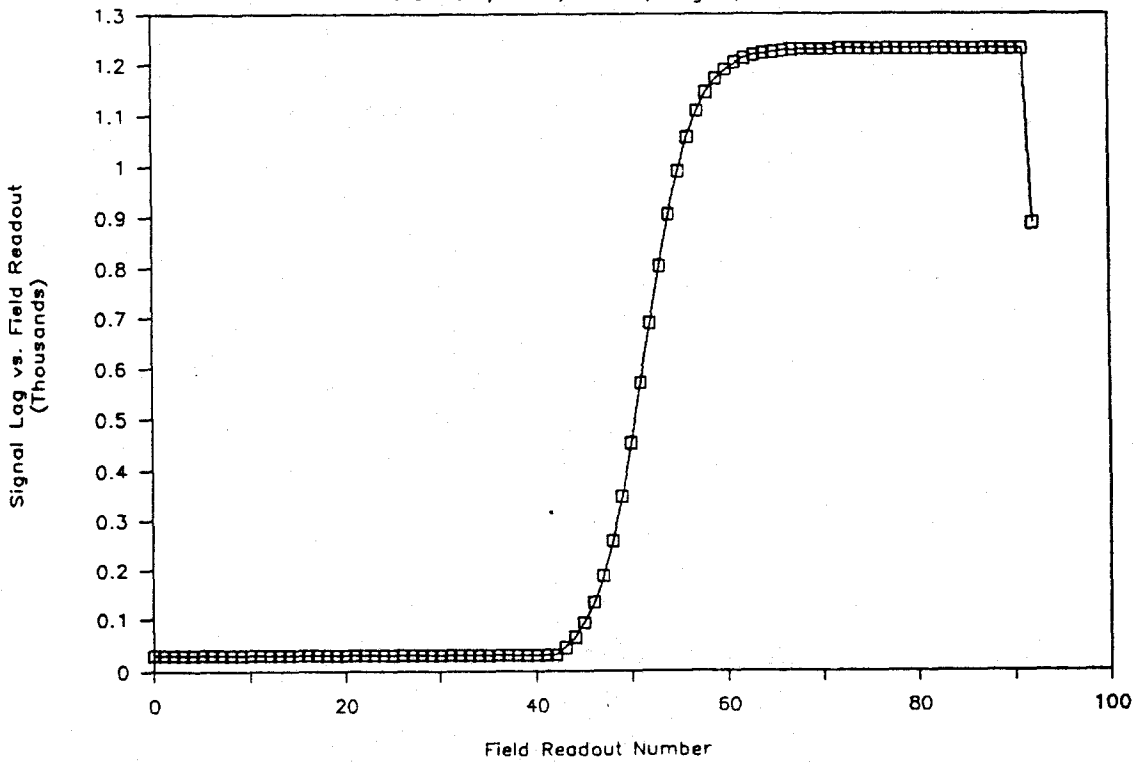


Figure 5-52. Signal lag with unpinned photodiode — 1,200 electrons signal. Run 3C-01

NO IMAGE LAG PHOTODIODE STRUCTURE IN THE INTERLINE CCD IMAGE SENSOR

Nobukazu Teranishi, Akiyoshi Kohono, Yasuo Ishihara, Eiji Oda and Kouichi Arai

Microelectronics Research Laboratories, Nippon Electric Co., Ltd.

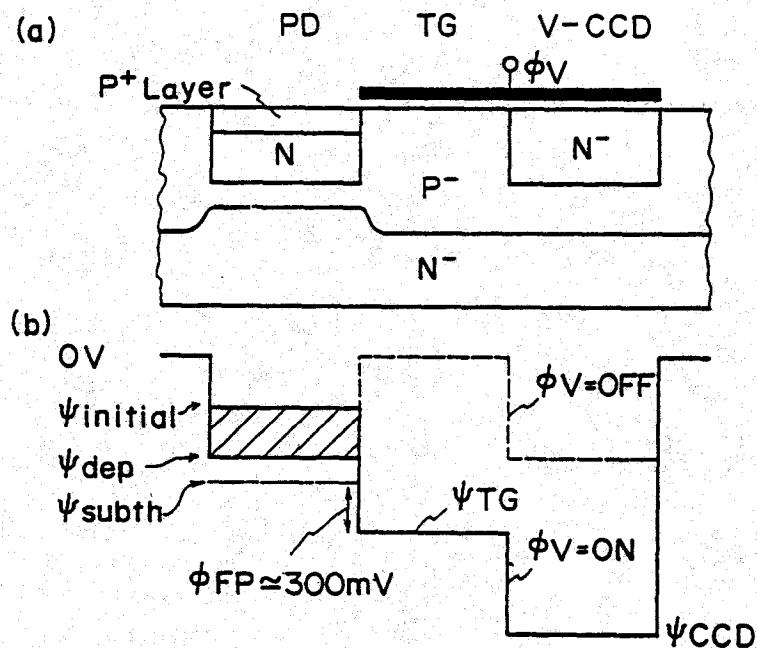
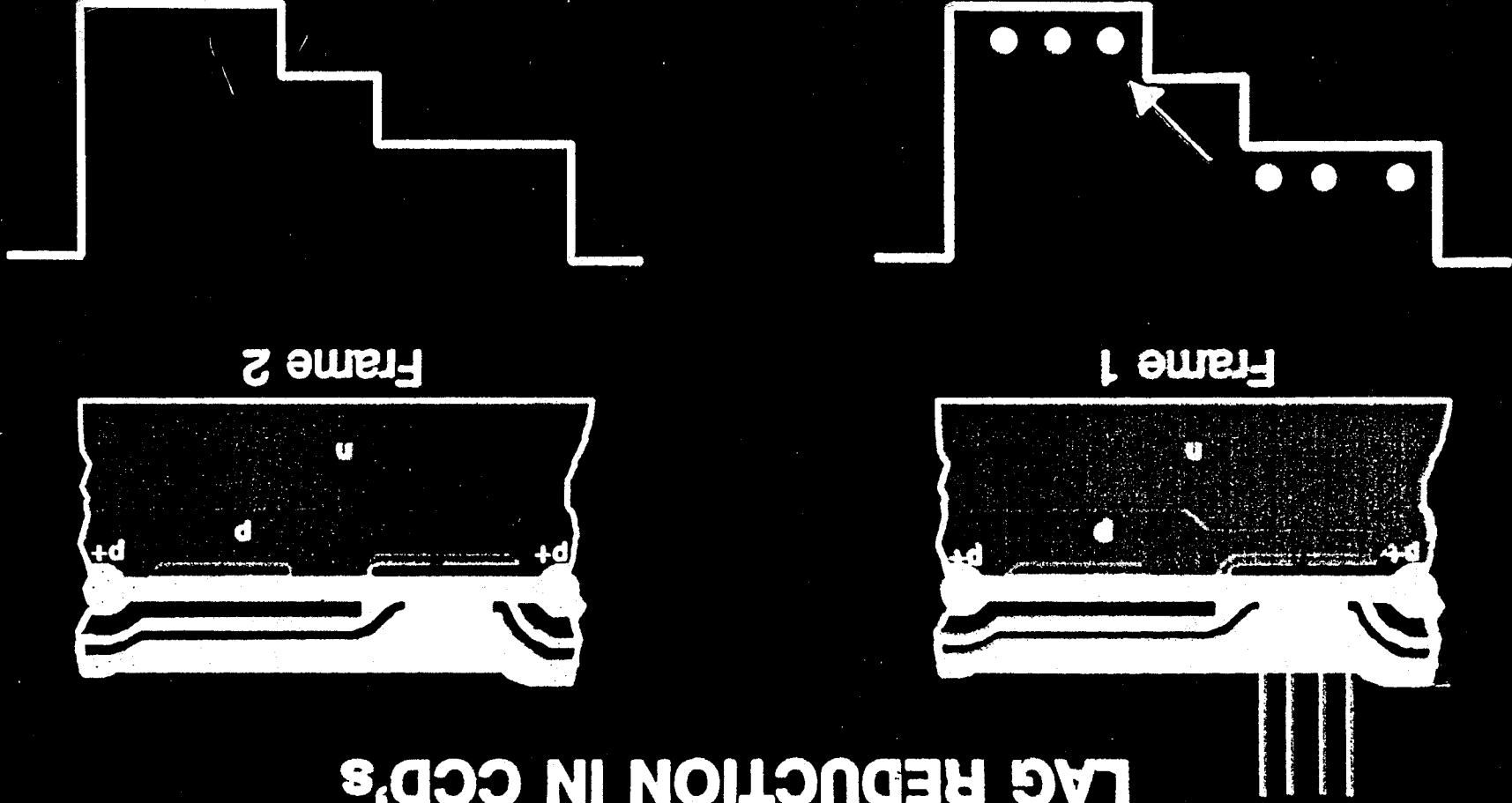
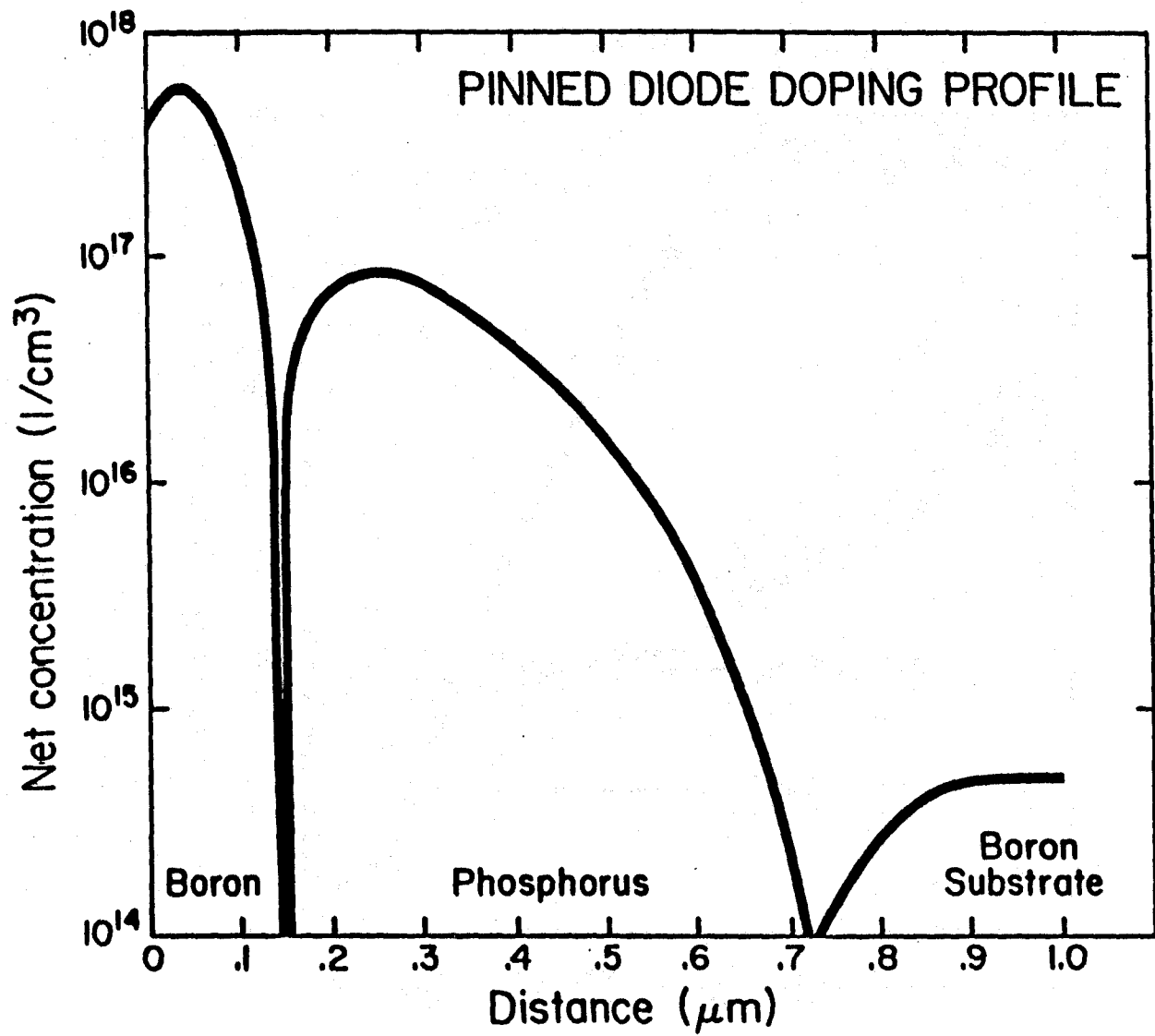


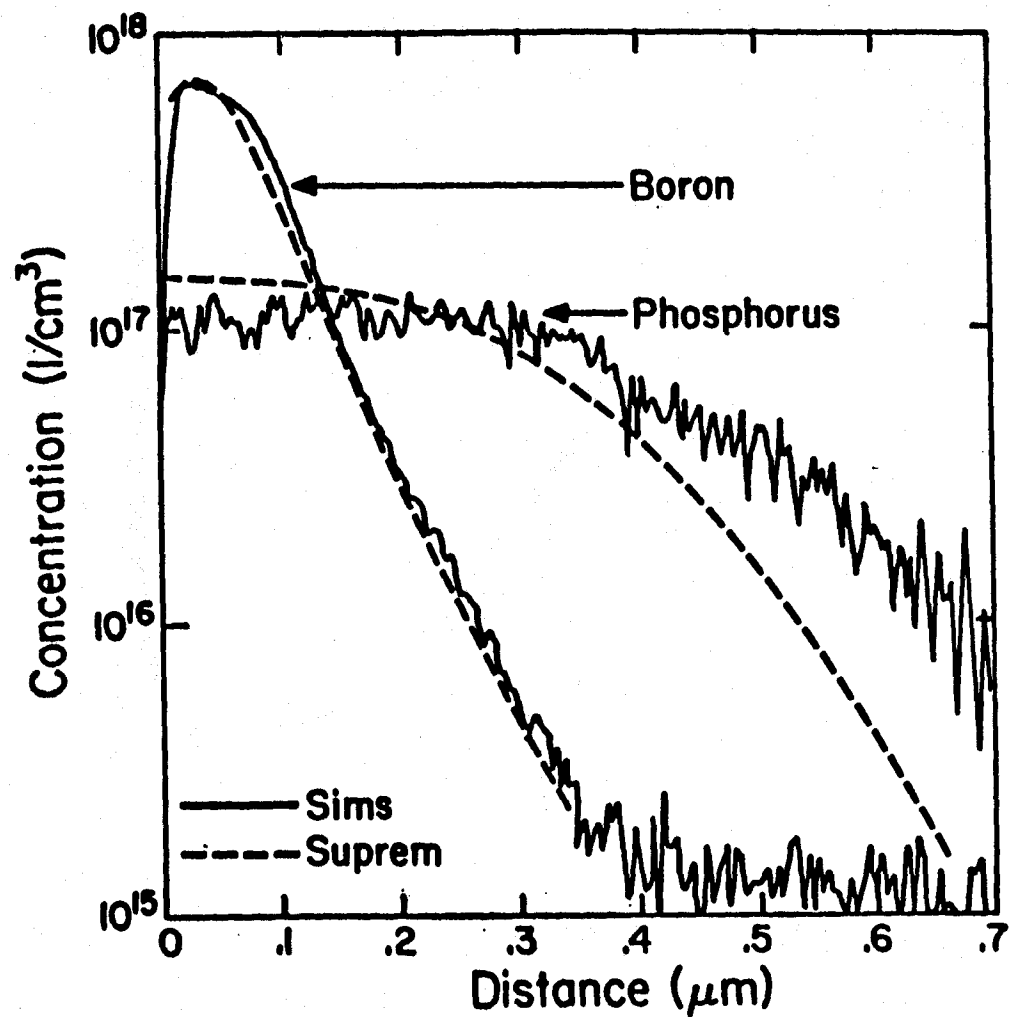
Fig.5. P⁺NP⁻ structure photodiode
 (a) Unit cell cross sectional view
 (b) Potential profile in a complete transfer mode

PINNED PHOTODIODE FOR LAG REDUCTION IN CCD'S



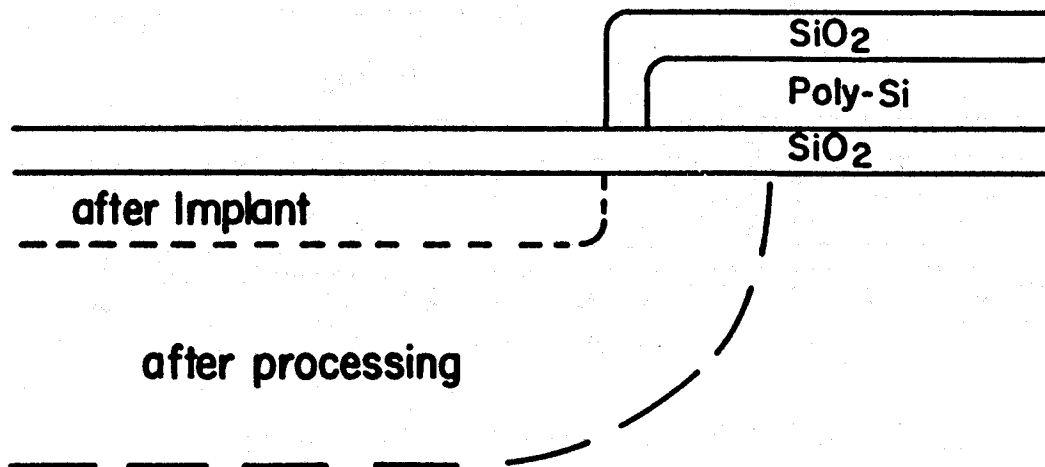
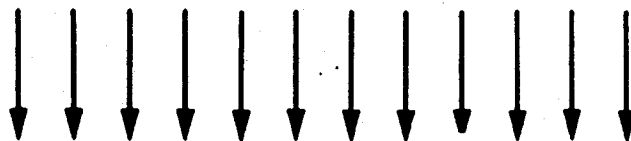


PINNED DIODE - SUPREM/SIMS

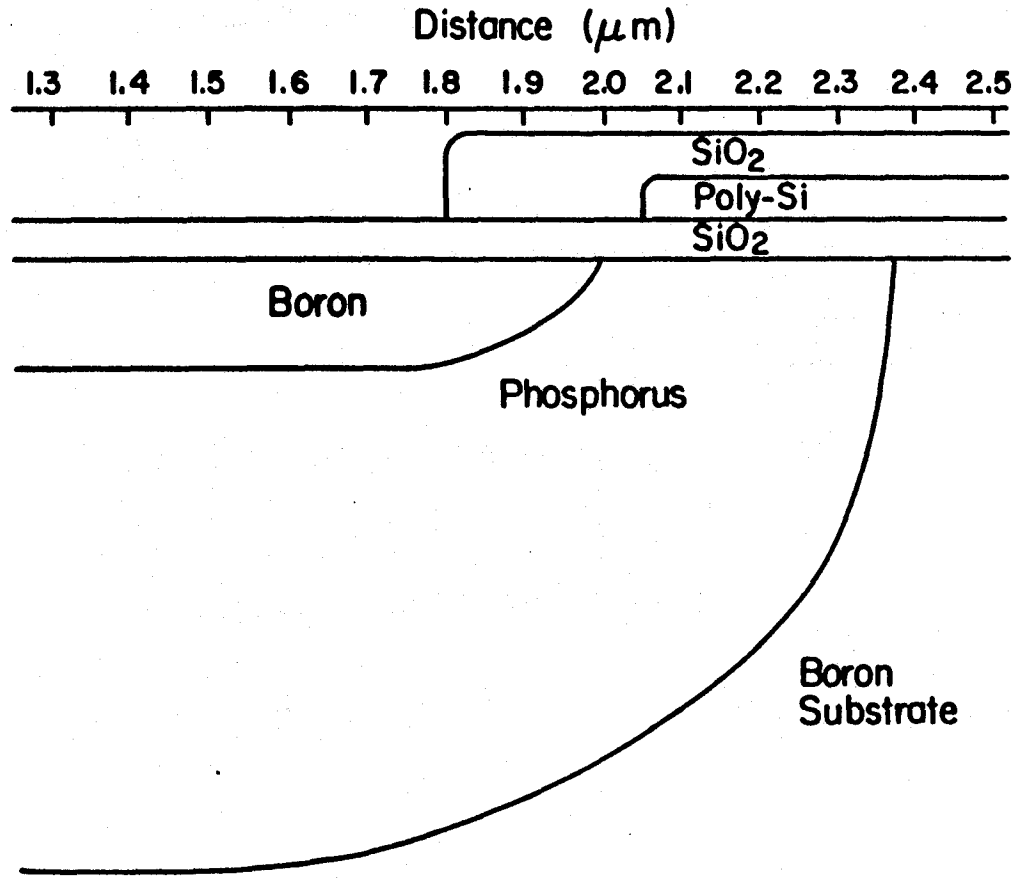


PINNED DIODE -TRANSFER GATE BARRIER

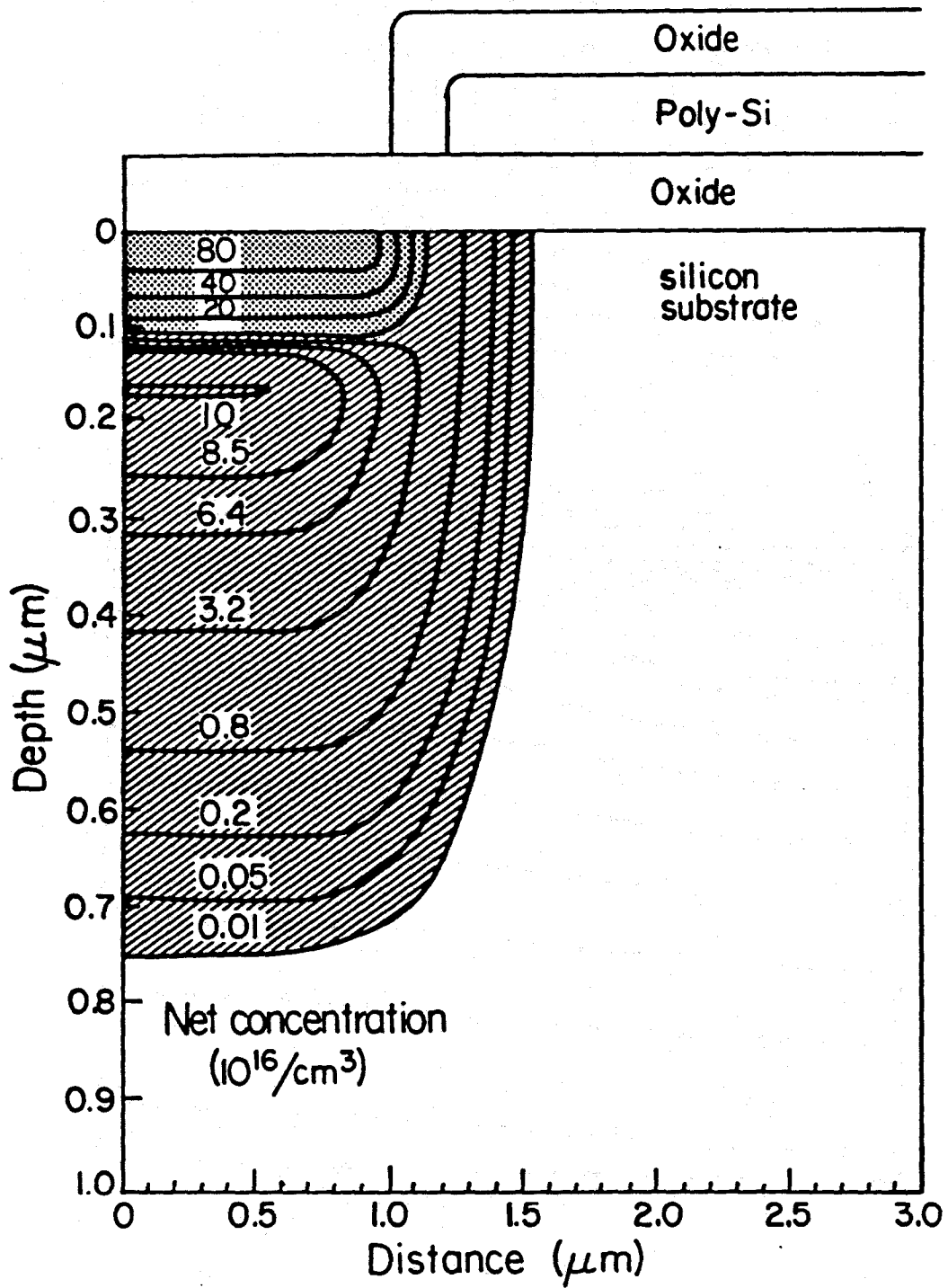
Phosphorus & Boron Implants



PINNED DIODE - TRANSFER GATE BARRIER

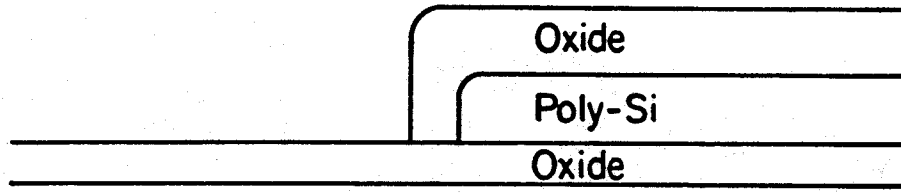
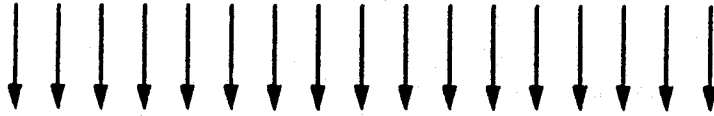


PINNED DIODE DOPING - SUPRA

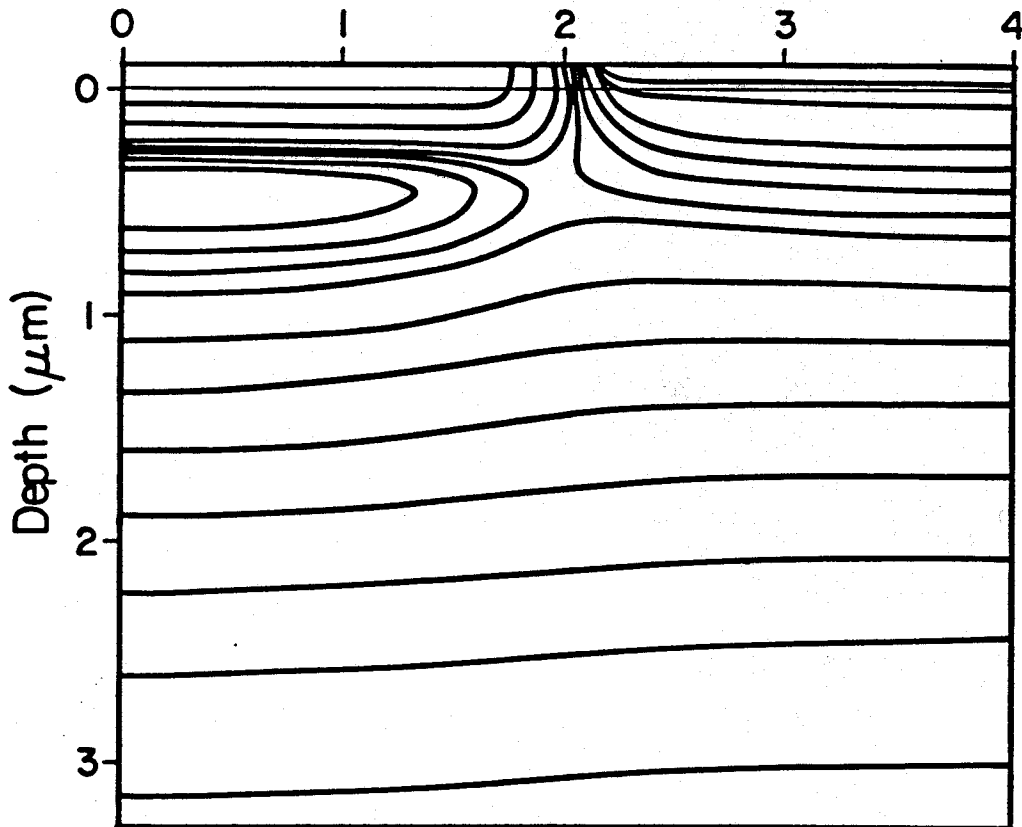


PINNED DIODE-TRANSFER GATE BARRIER
ELECTROSTATIC POTENTIAL CONTOURS

Phosphorus and Boron Implants



Distance (μm)



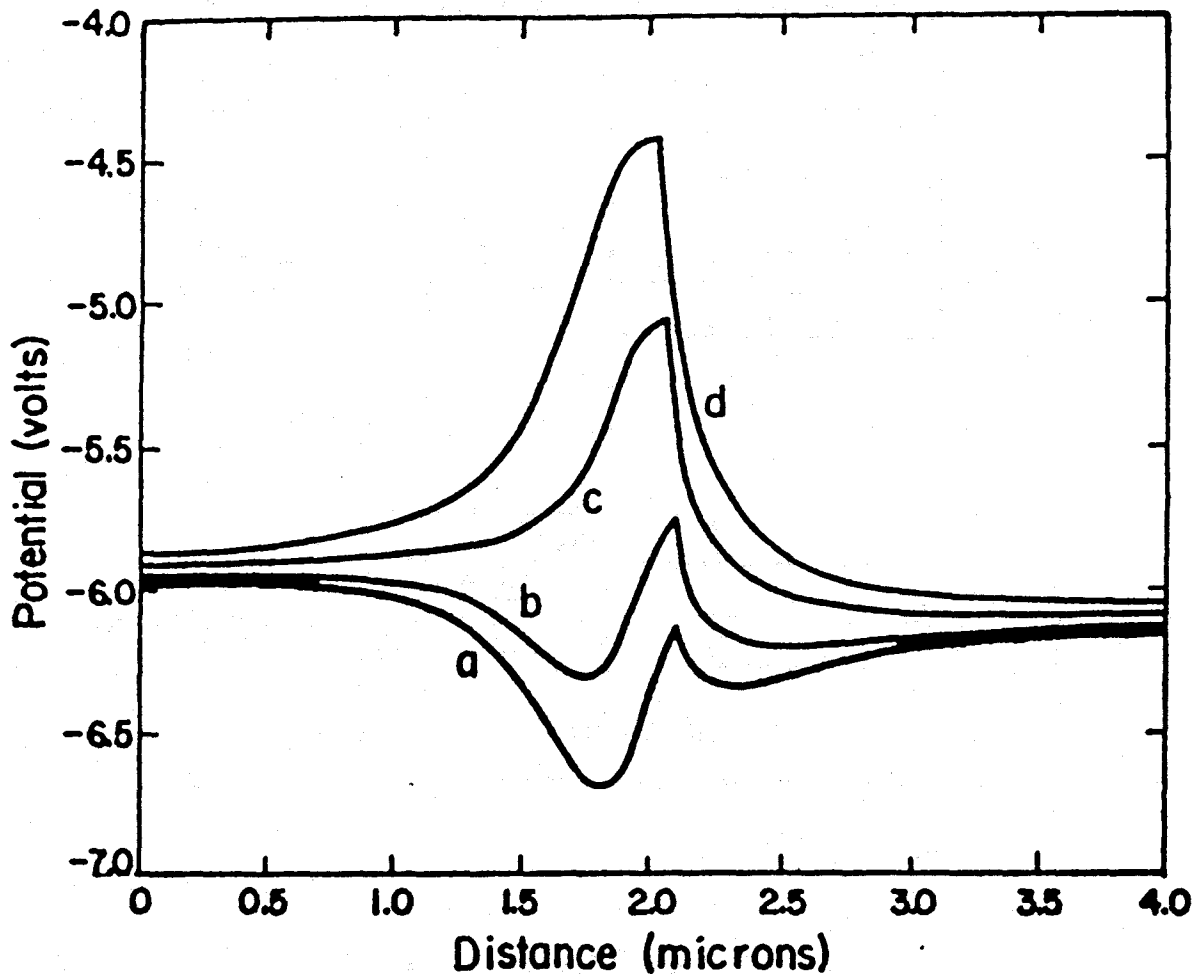
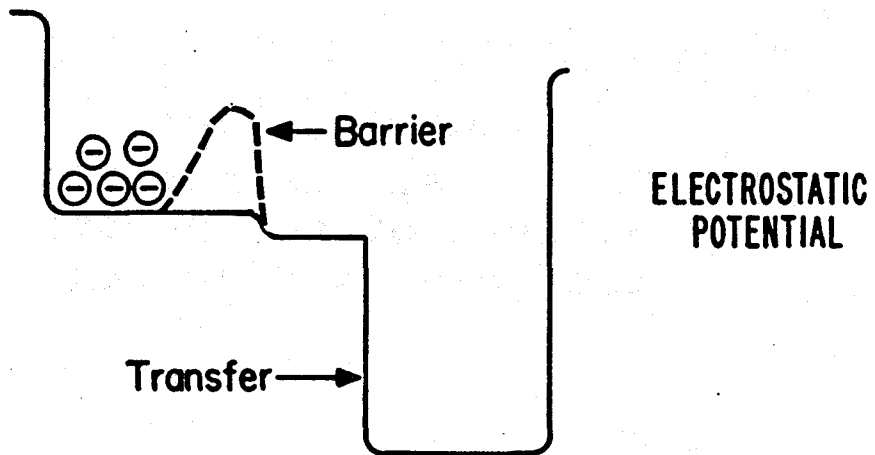
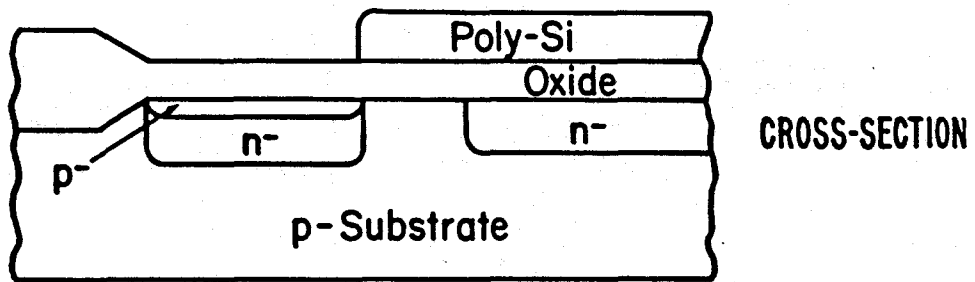
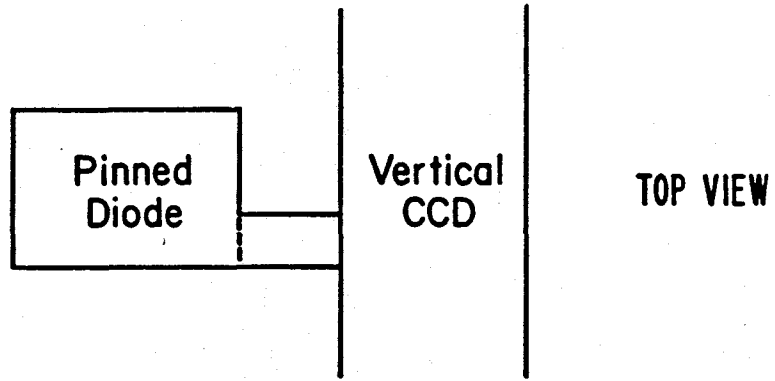
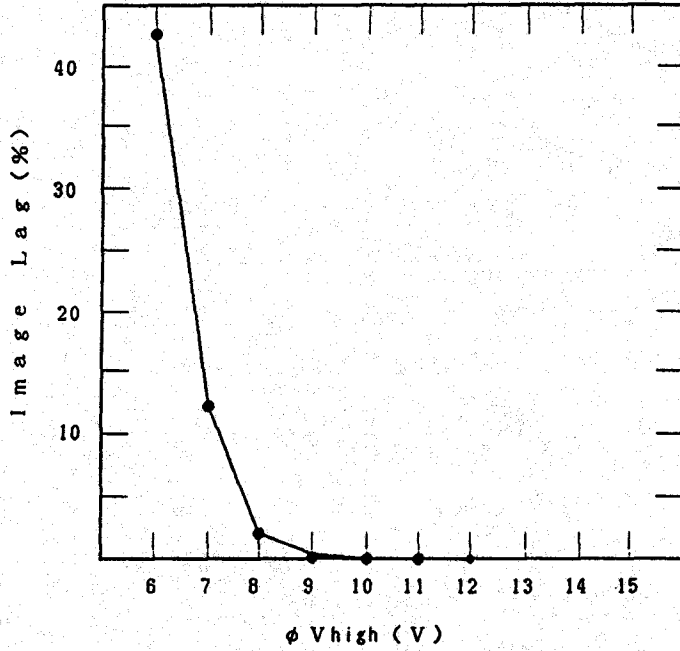


Fig. 11. Potential barrier for various offsets of the phosphorus from the poly-Si transfer gate.

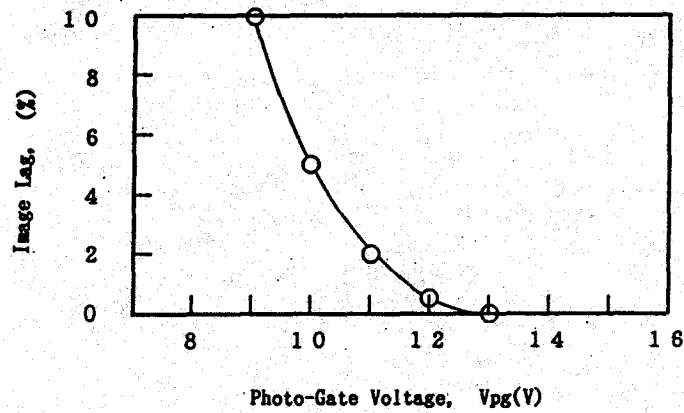
D4-IMAGE CELL ARCHITECTURE





*Kuriyama
et al*

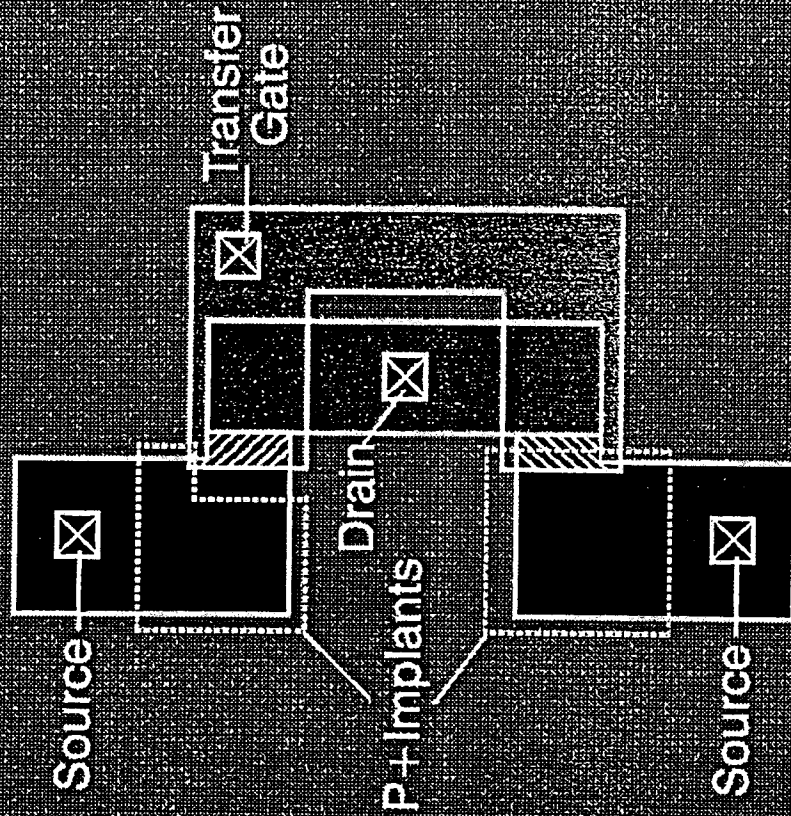
Fig. 12. Image lag as function of the VCCD transfer gate clock pulse amplitude (ϕV_{high}).



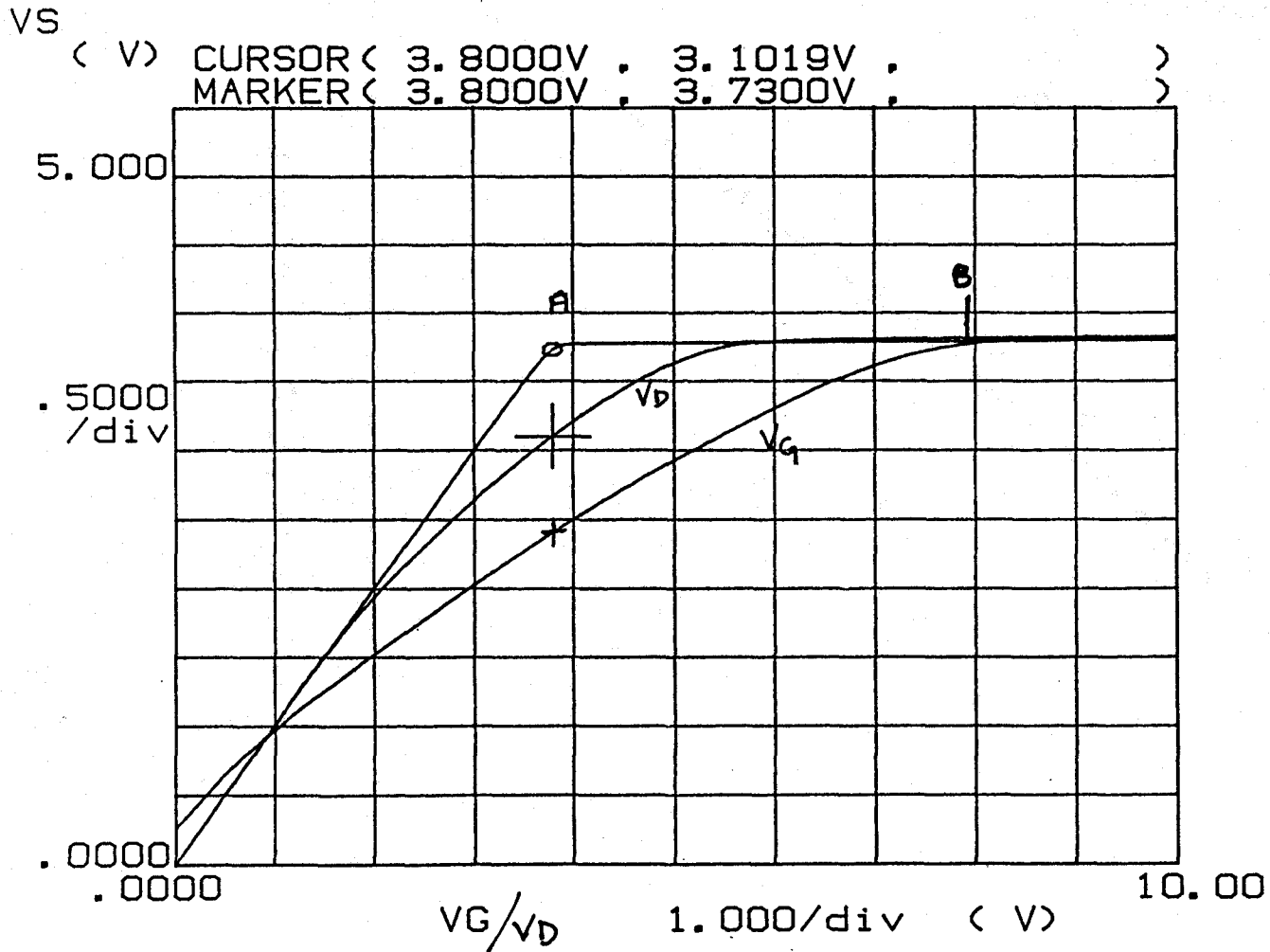
Ando et al

Fig. 10. Image lag characteristics of the device.

PD-TO-VCCD BARRIER TEST STRUCTURE

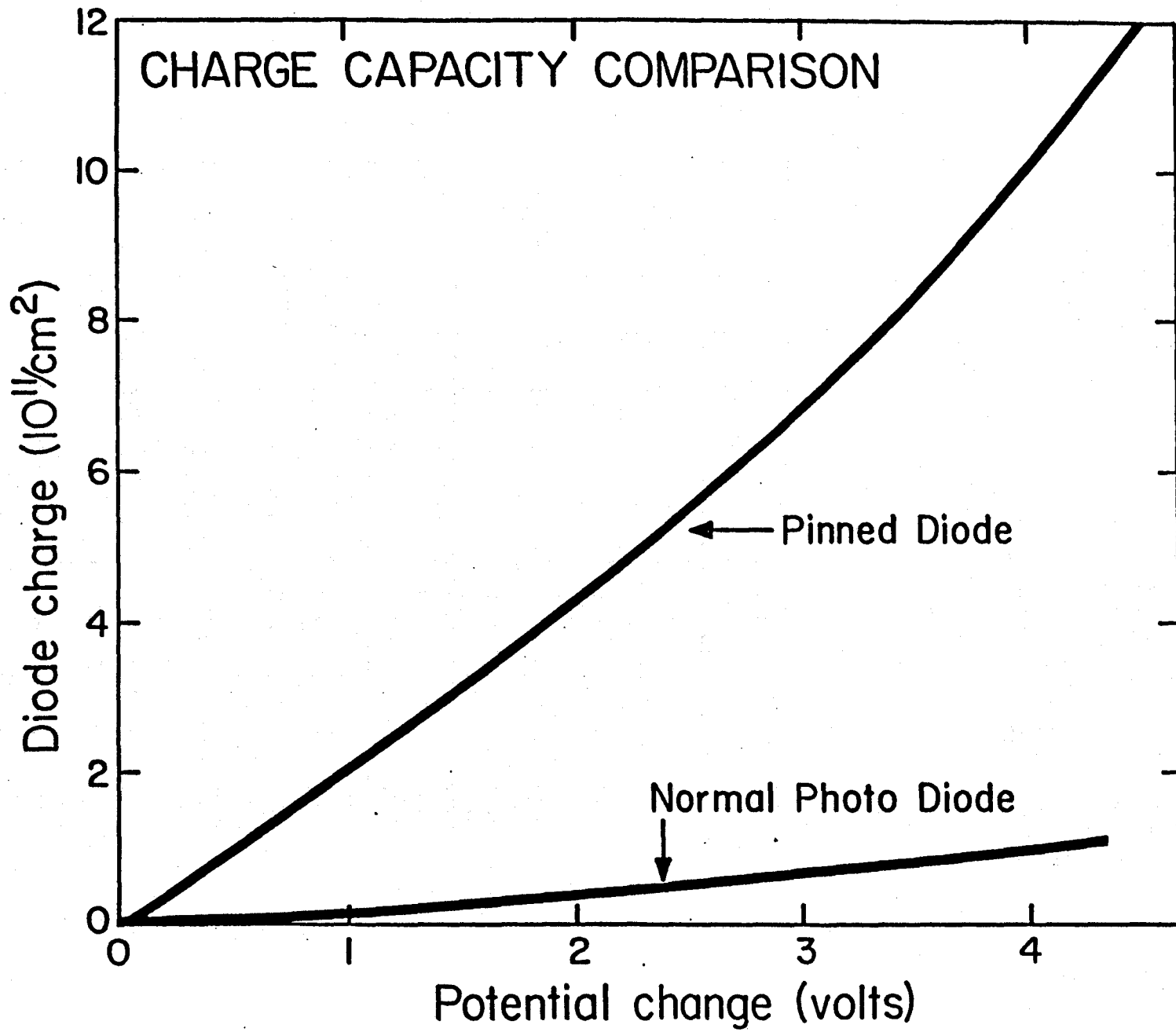


***** GRAPHICS PLOT *****
M2 3D77-14 TVOD 2



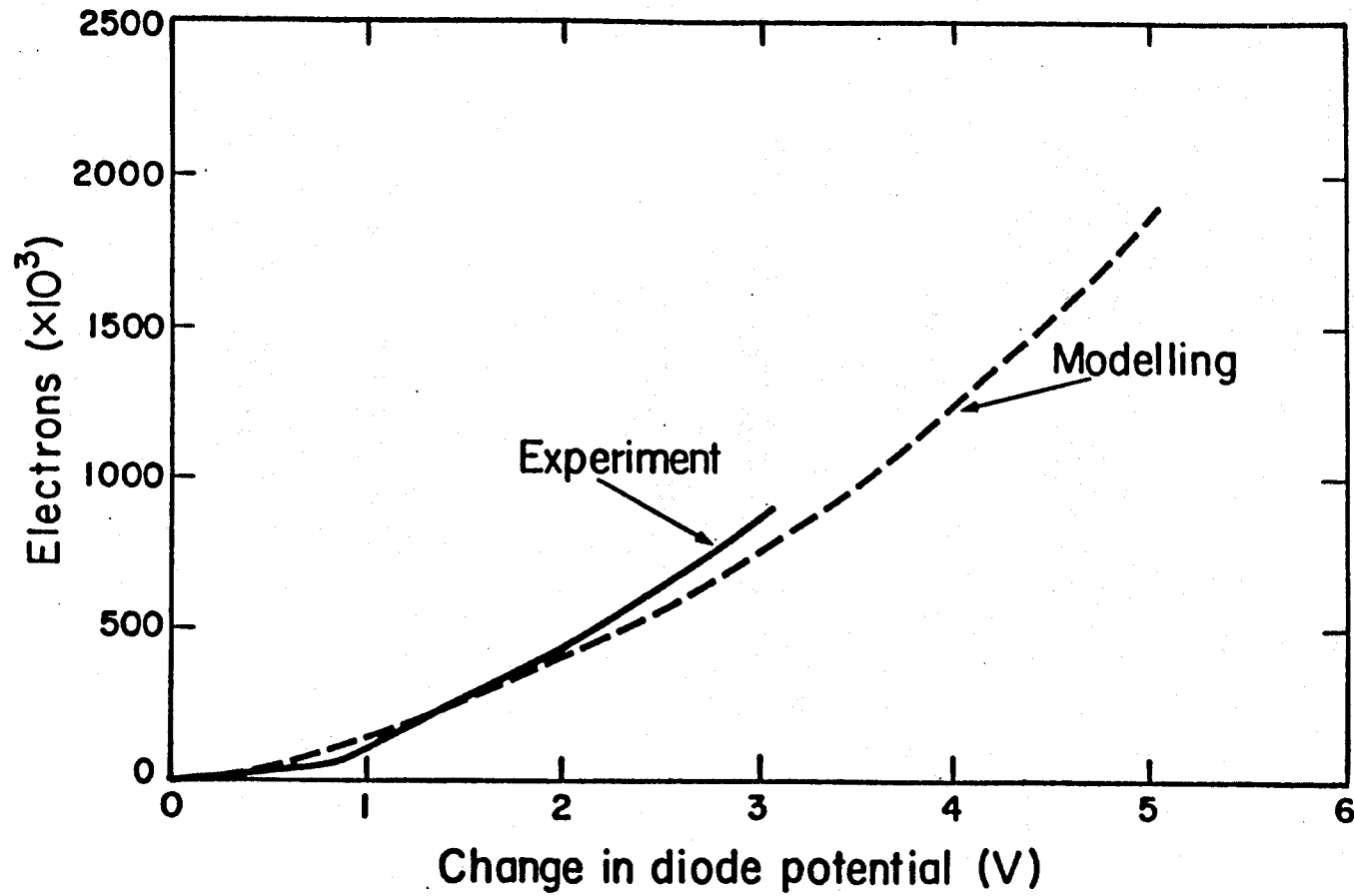
Variable1:
VG -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
VD -Ch2 15.000V
IS -Ch3 -50.00nA
VW -Ch4 .0000V
VSub -Vs1 15.000V
VS2 -Vs2 .0000V



E+3

PINNED DIODE CHARGE CAPACITY



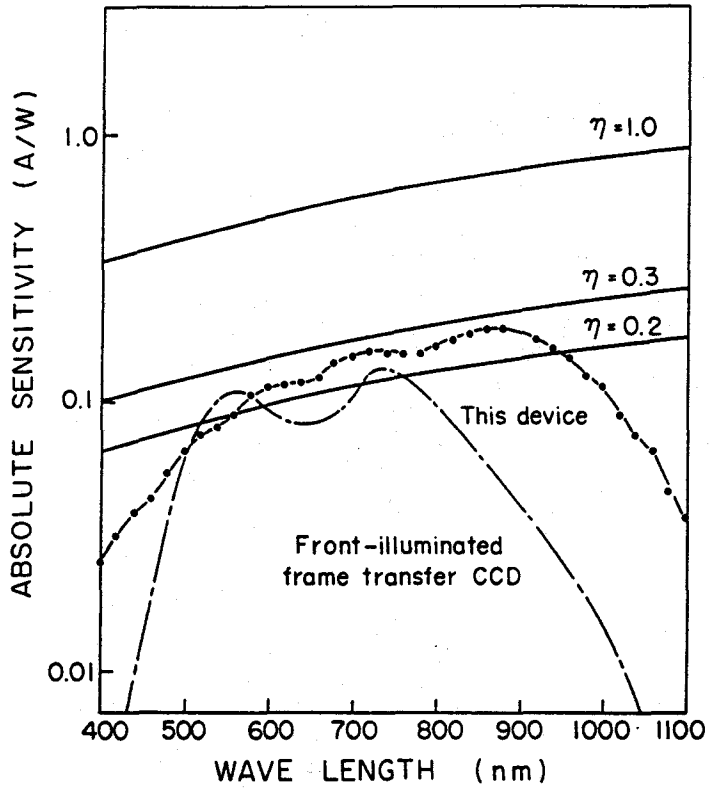
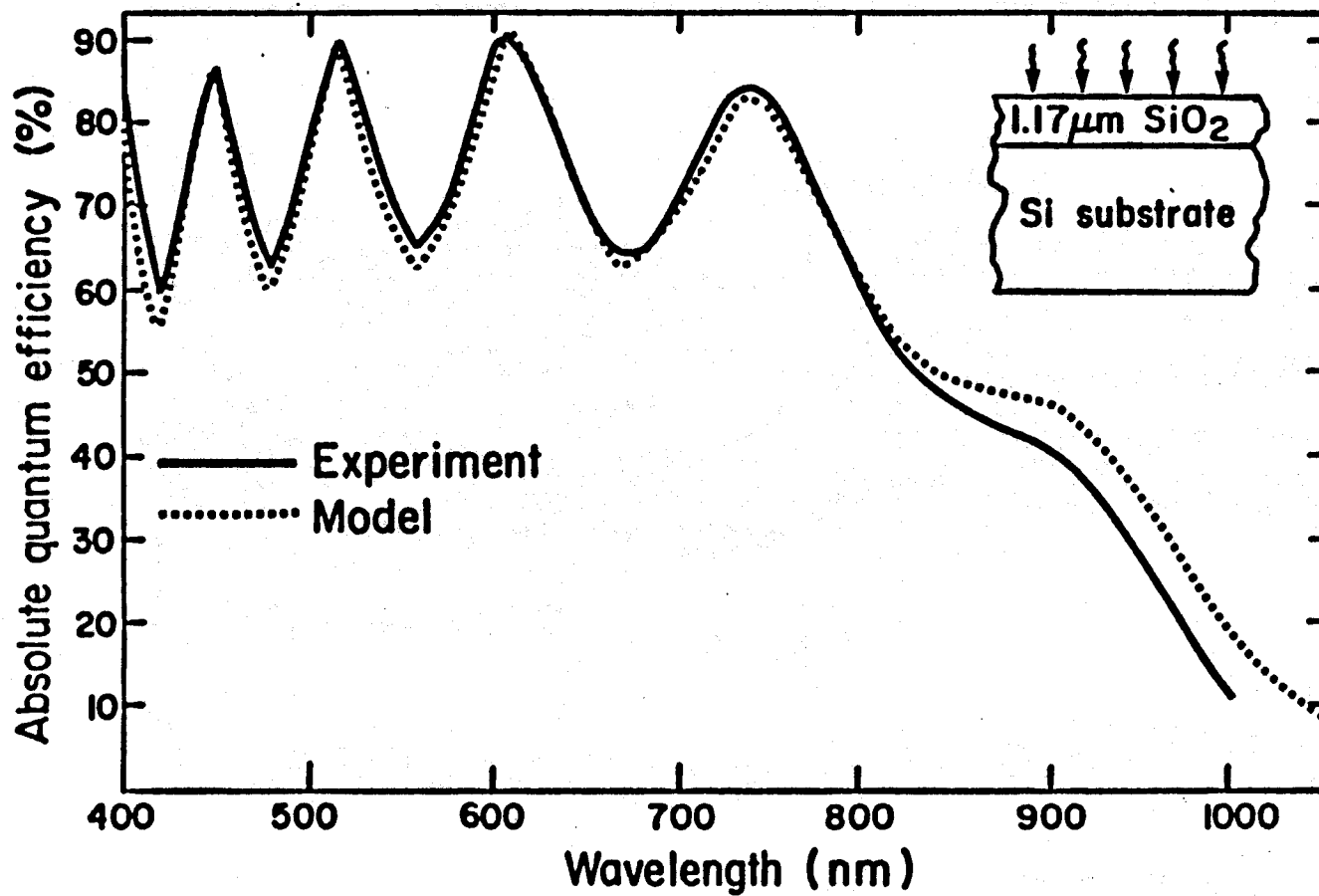


FIGURE 4—Spectral response.

Ishihara et al

ISSCC 80

PINNED DIODE
ABSOLUTE SPECTRAL QUANTUM EFFICIENCY



S.Manabe, et al., "A 2 Million Pixel CCD Imager Overlaid with an Amorphous Silicon Photoconversion Layer"

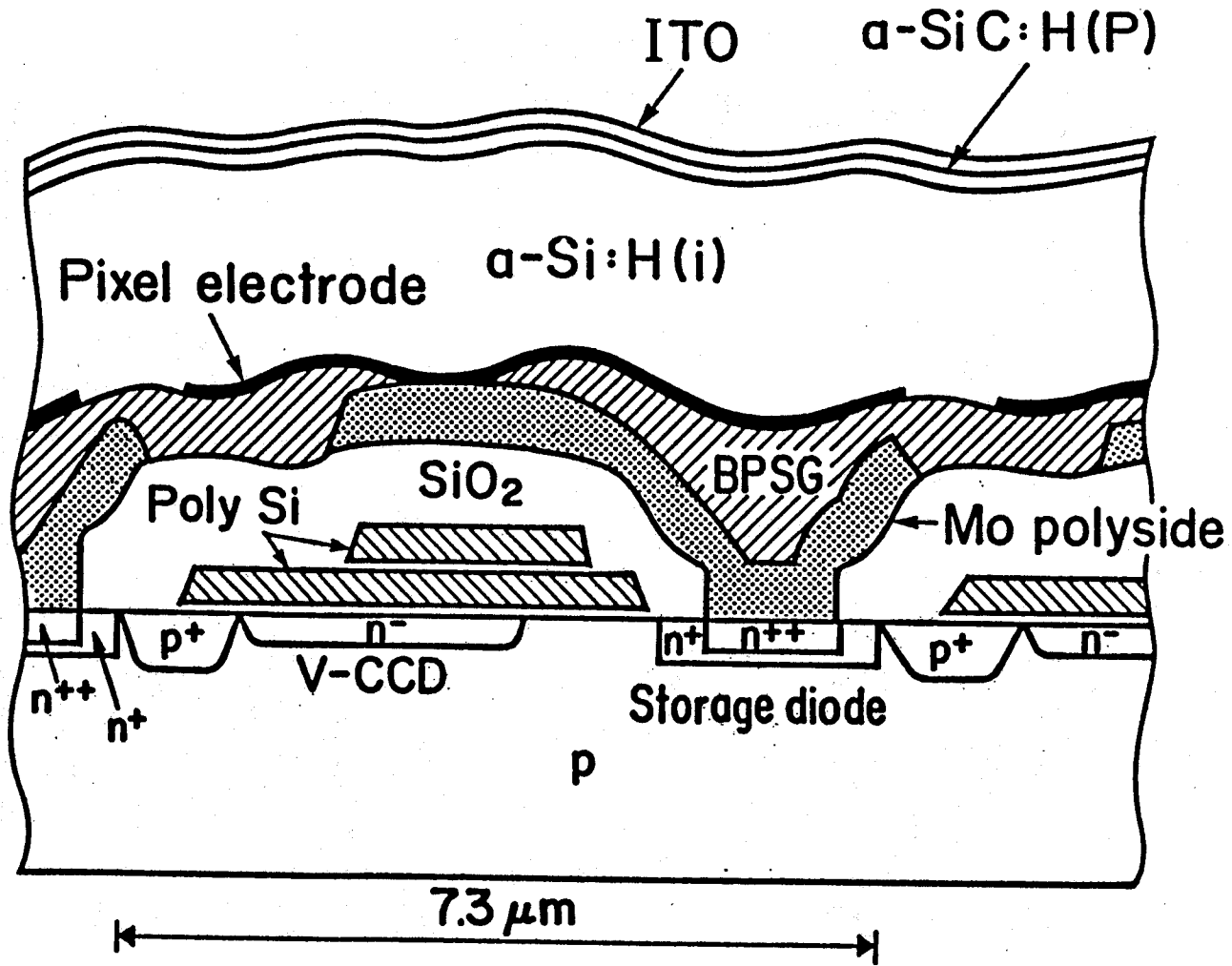
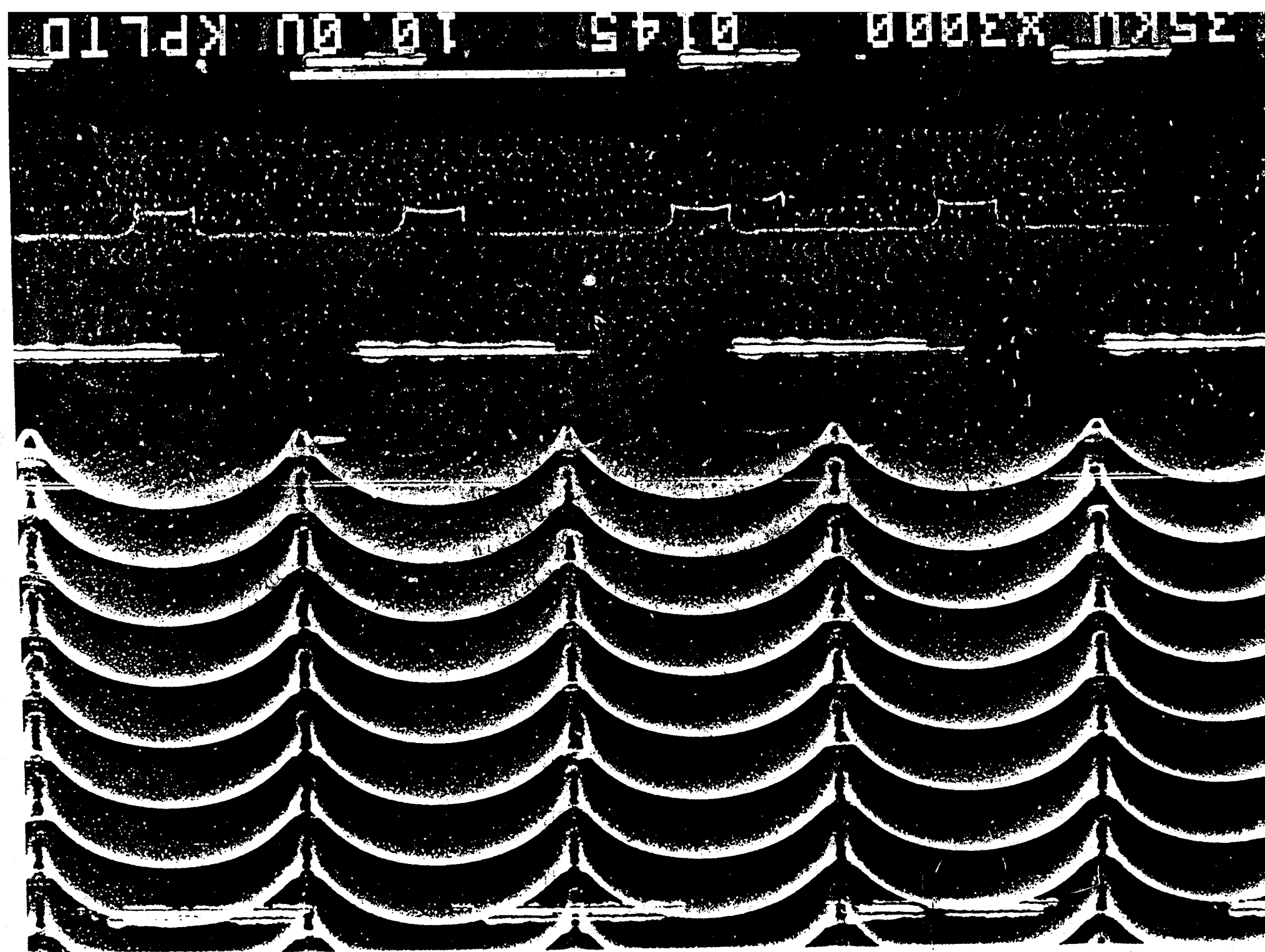
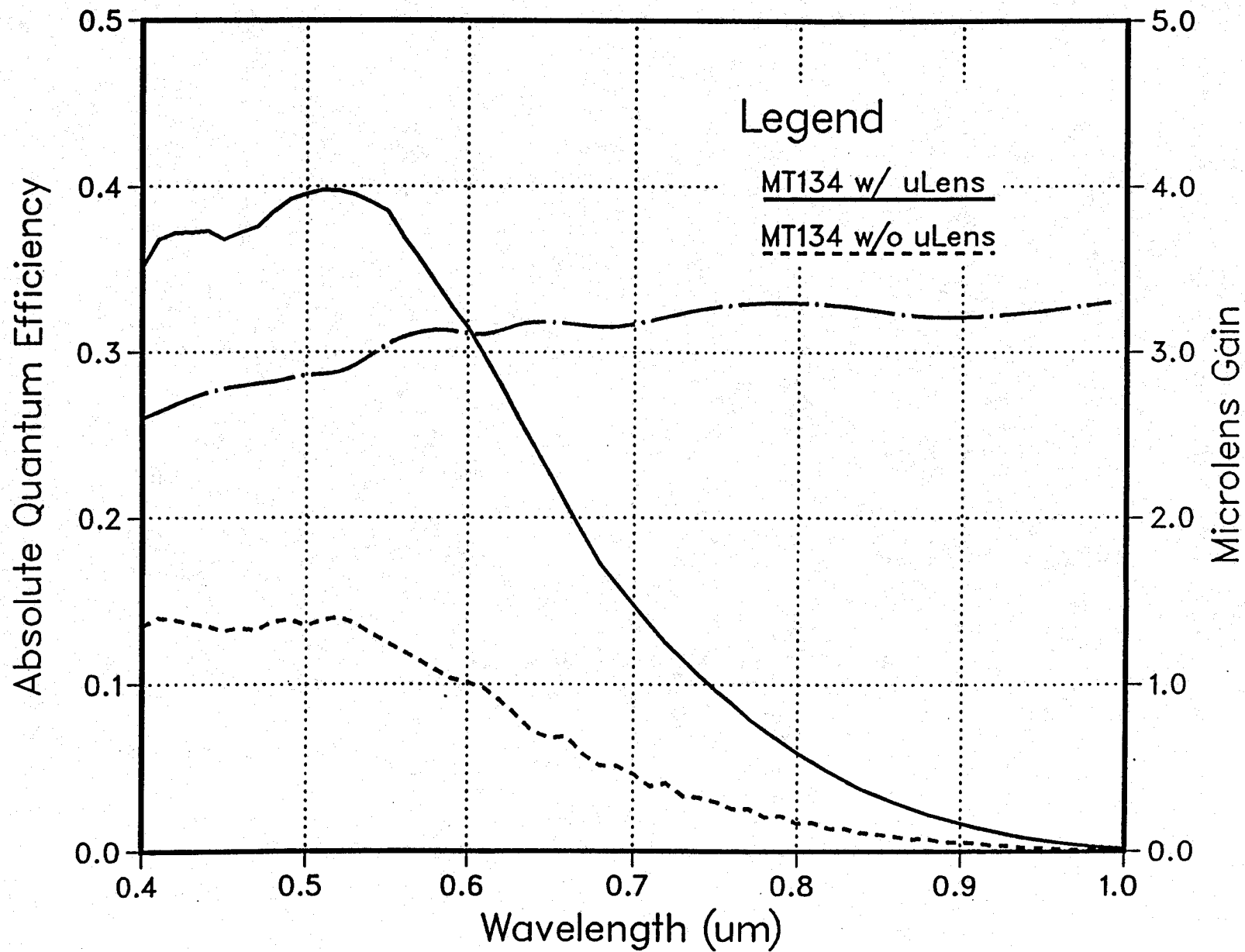


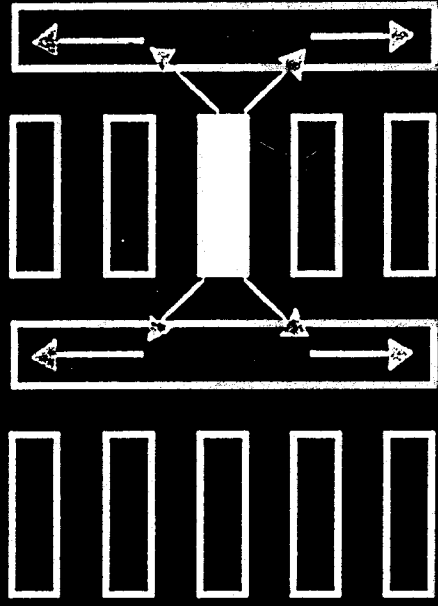
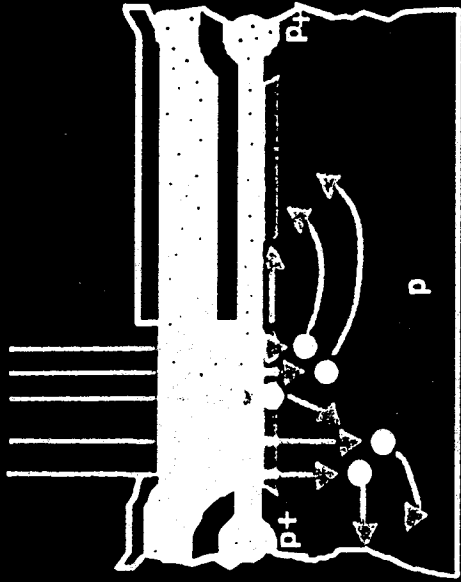
FIGURE 2 Cross section view of unit cell



M2 Quantum Efficiency w/ and w/o uLens MT134 (MEASURED)



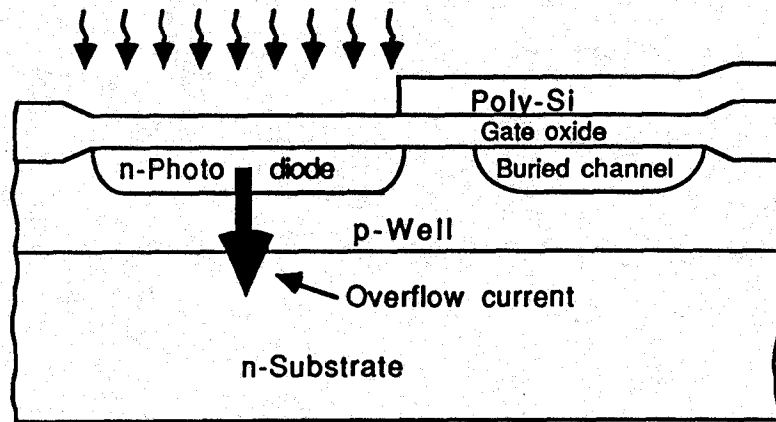
BLOOMING IN CCD IMAGE SENSORS



- Illumination Beyond Saturation Causes Overflow Into CCD
- Excess Charge Floods Vertical CCD

ANTIBLOOMING SCHEMES

Vertical Overflow Drain (VOD)



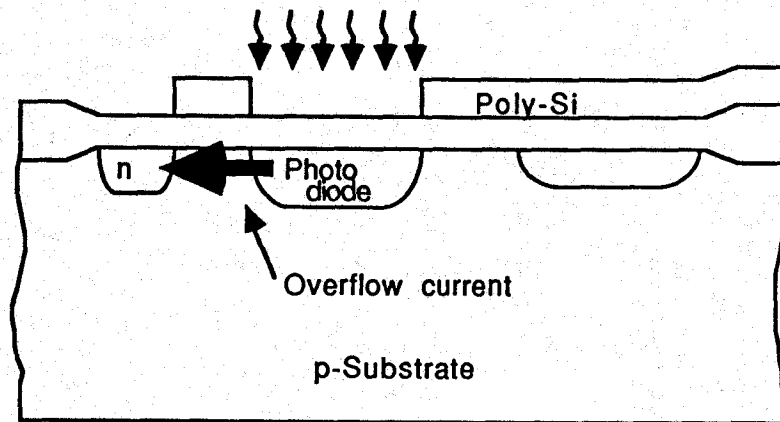
Advantages

- Large fill factor
- More scalable
- Less image smear

Disadvantages

- Less red response
- More difficult to make lag free

Lateral Overflow Drain (LOD)



Advantages

- Better red response
- Easier to make lag free

Disadvantages

- Difficult to scale
- Much smaller fill factor
- More image smear

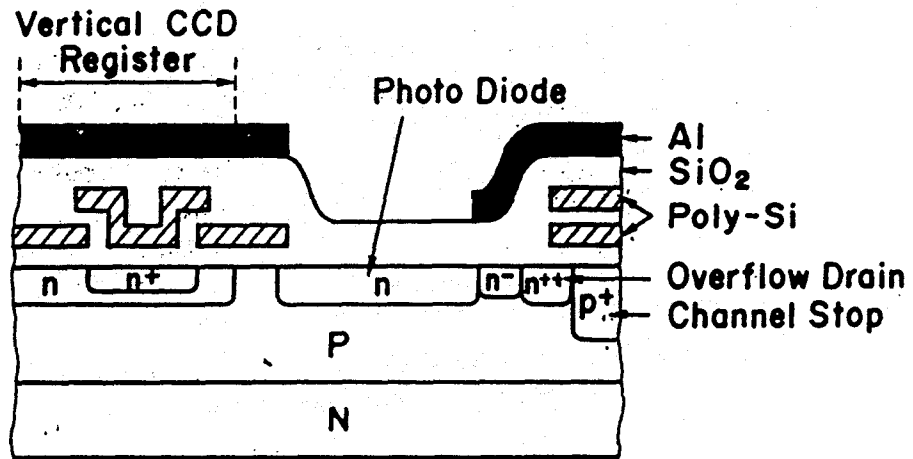


Fig. 3. Picture element ^{VU} cross section.

Furukawa et al

IEDM 1980

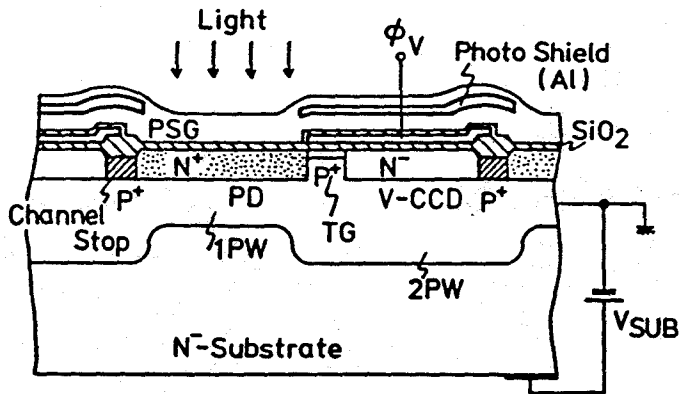
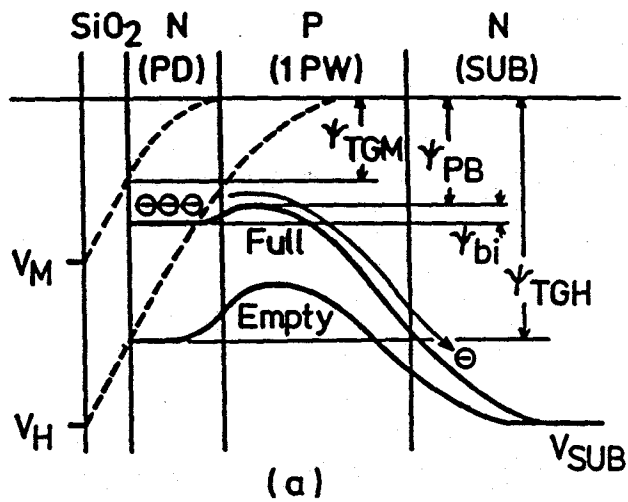
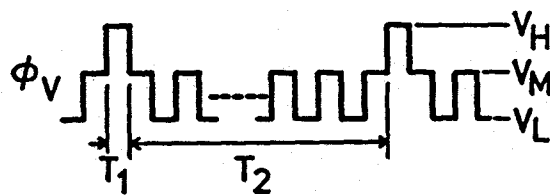


FIGURE 1—Cross sectional view of a unit cell for vertical overflow drain CCD image sensor.



(a)



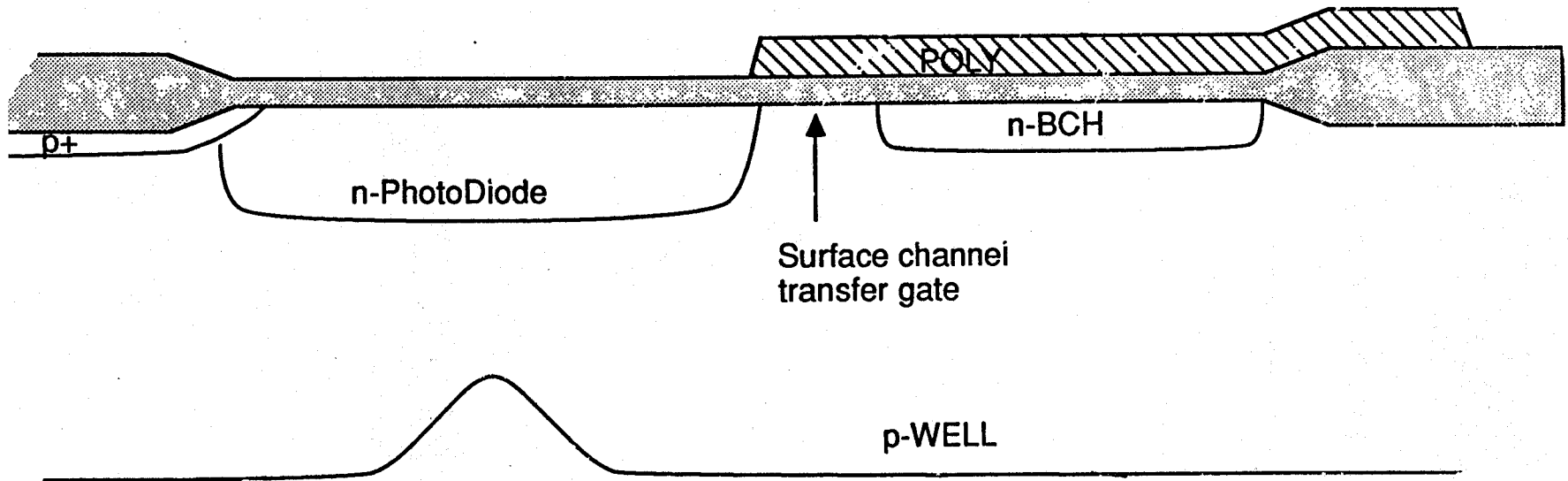
(b)

FIGURE 2—(a) Potential profiles under the PD and the TG region, and (b) one of the V-CCD clock pulses ϕ_V .

Ishihara / NEC

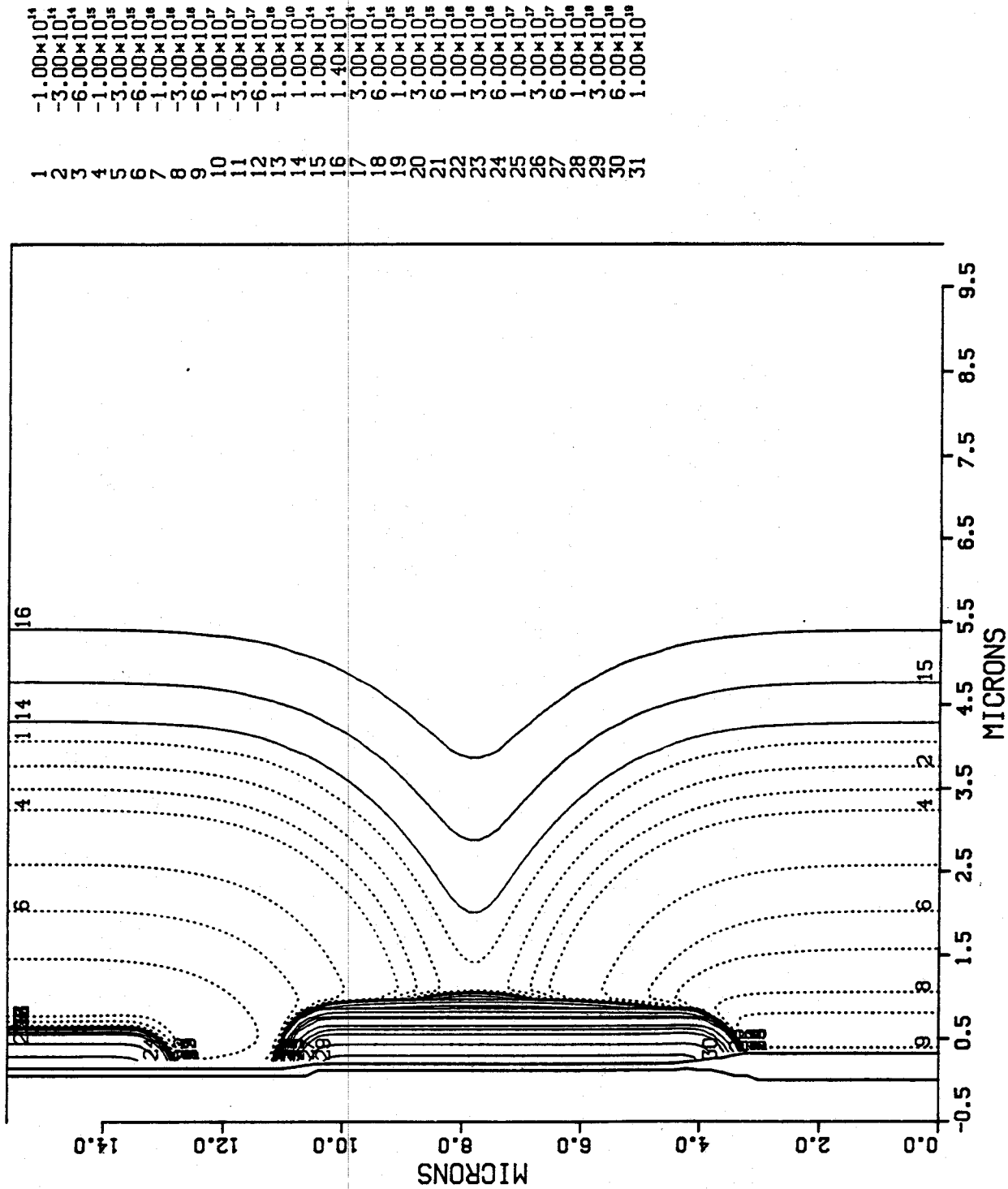
ISSCC 82

IEEE ED-30 84

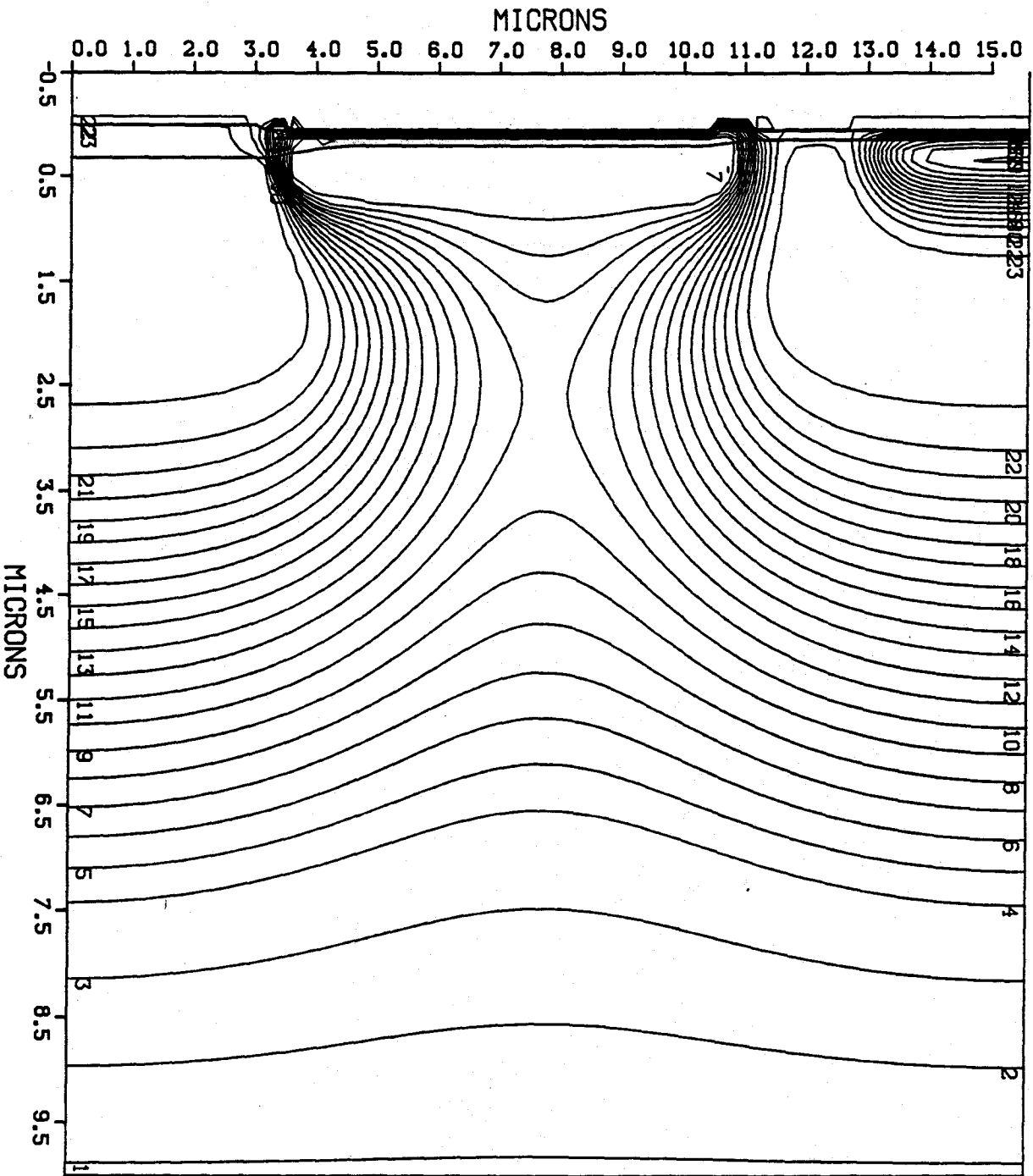


**PIXEL CROSS-SECTION OF
INTERLINE CCD WITH VOD**

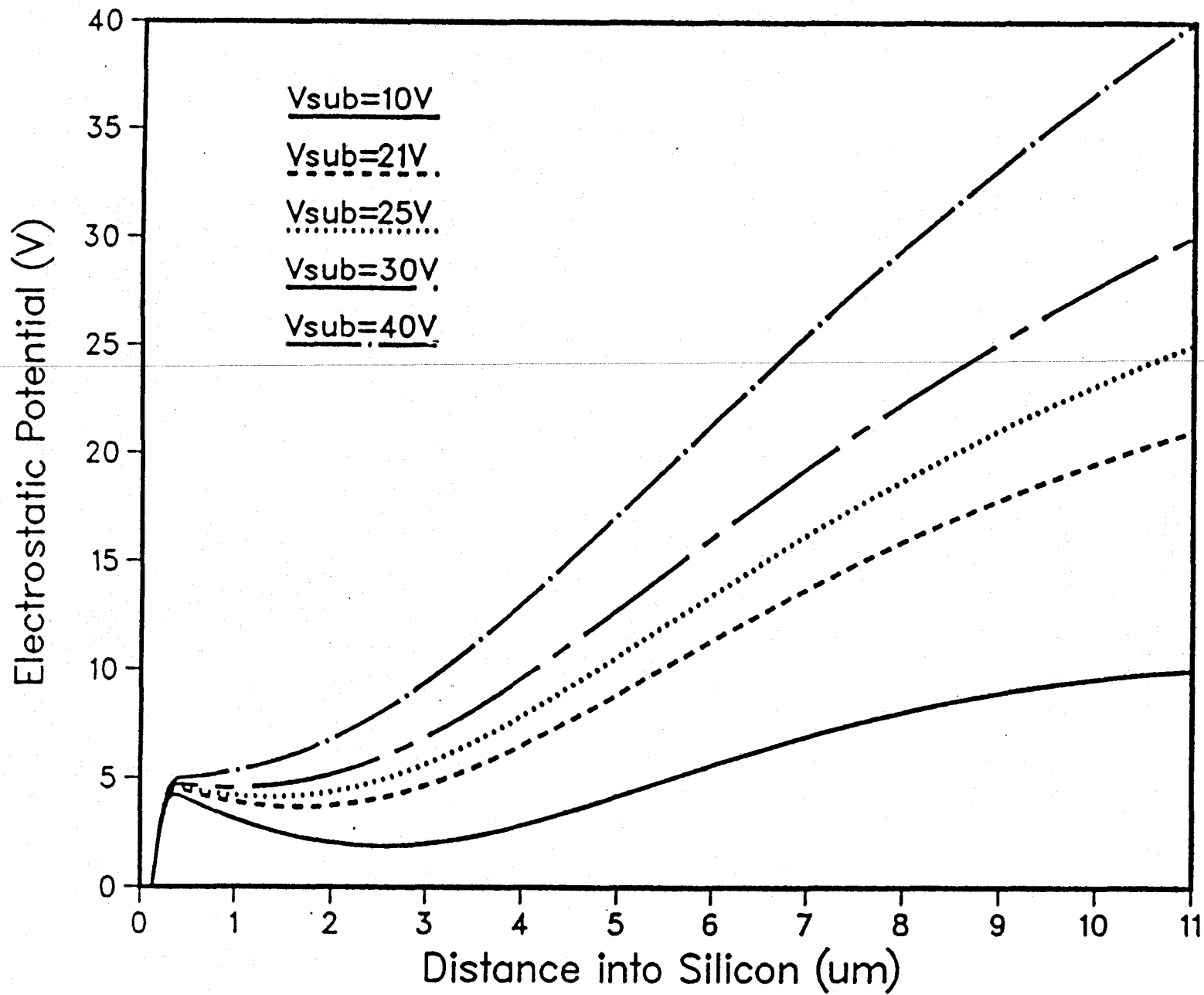
NOMINAL PROCESS

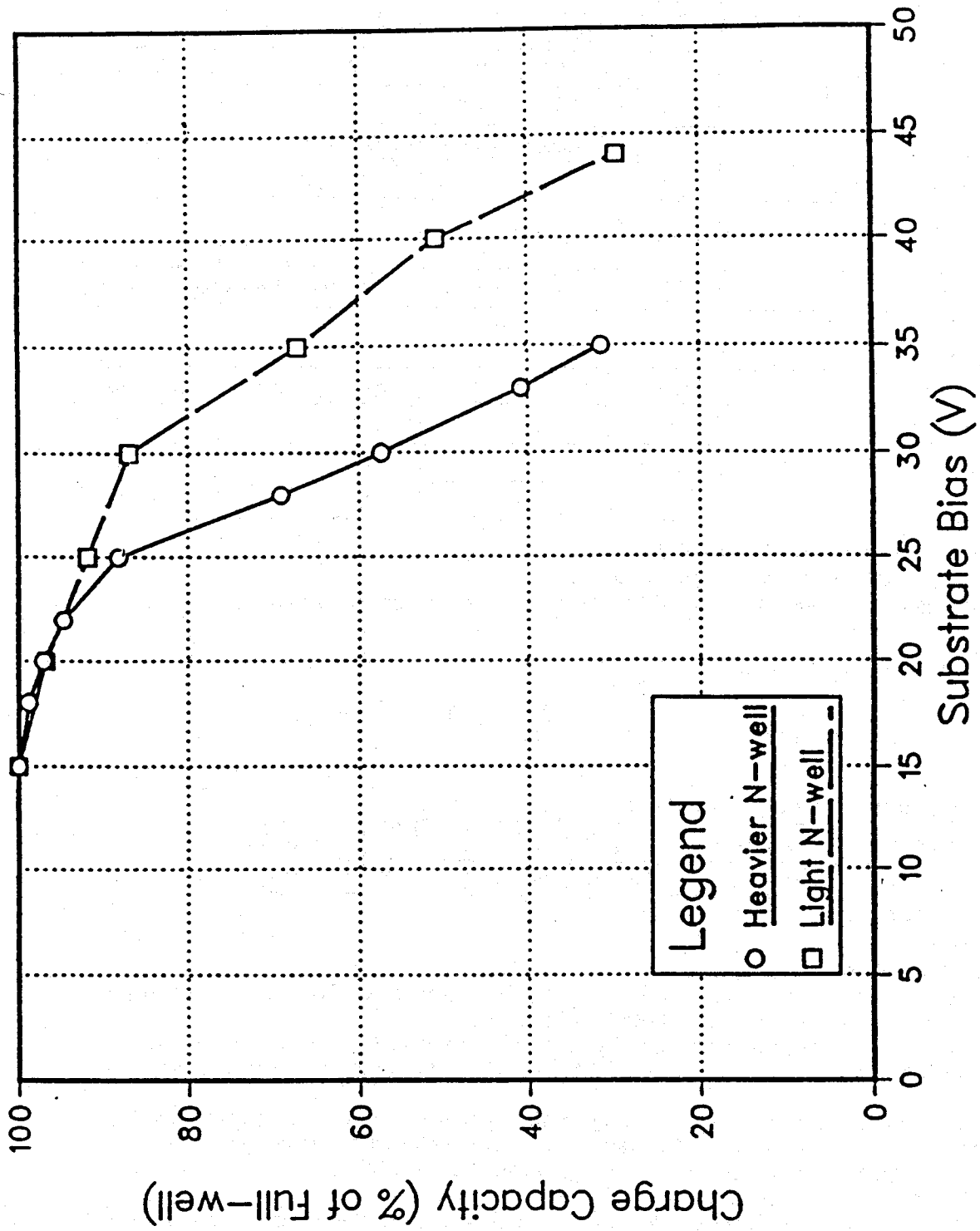


VG-12, VS-12, VD-12, VTL-5, VTR--5, 9/3/86



1	0.10
2	1.00
3	2.00
4	3.00
5	3.50
6	4.00
7	4.50
8	5.00
9	5.50
10	6.00
11	6.50
12	7.00
13	7.50
14	8.00
15	8.50
16	9.00
17	9.50
18	10.00
19	10.50
20	11.00
21	11.50
22	12.00
23	12.50





Measured charge capacity versus substrate bias.

Conditions

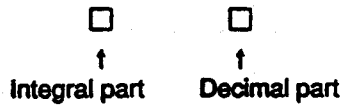
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V _{DD}	14.55	15.0	15.45	V	
	V _{PD}	14.55	15.0	15.45	V	Note 1
	V _{GG}	1.6	2.0	2.4	V	
	V _{SS}	Ground with a 390 Ω resistance				
Substrate voltage adjustable range	V _{SUB}	9		19	V	Note 2
Substrate voltage variation range after substrate voltage adjustment	V _{SUB}	-3		3	%	
Vertical transfer clock transistor bias	V _L	To be the vertical transfer clock low-level clamp bias				

Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I _{DD}		5.0		mA	Note 3
Input current	I _{IN1}			1	μA	Note 4
	I _{IN2}			10	μA	Note 5

- V_{PD} and V_{DD} must have the same voltage.
- Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code - Two digit indication

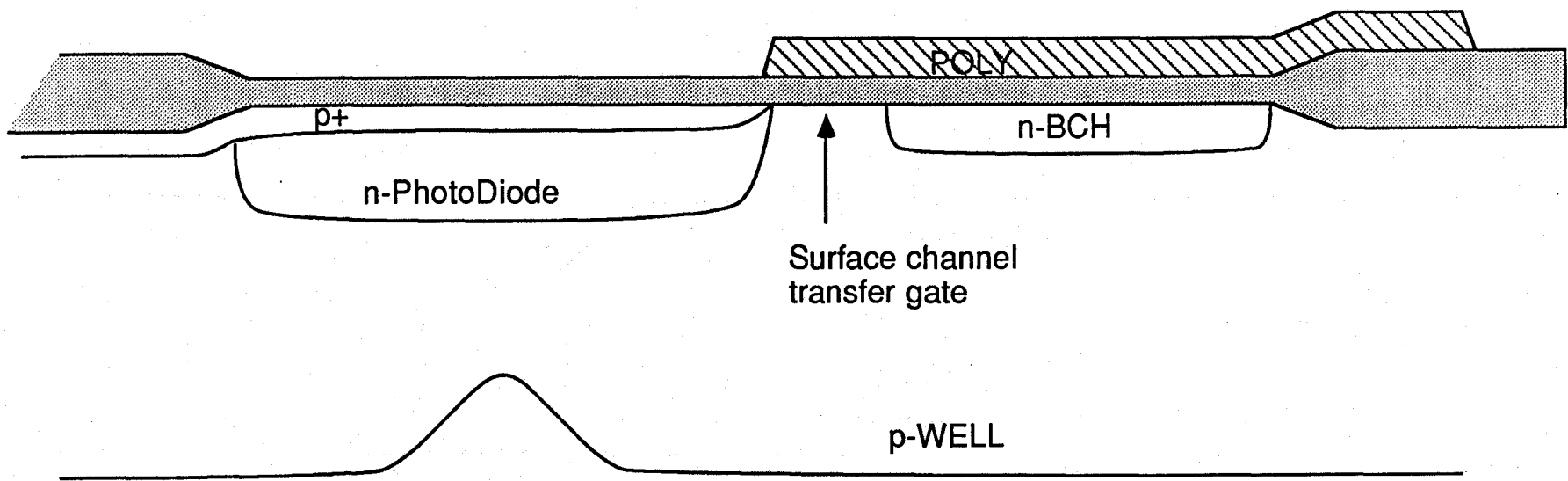


The integral codes correspond to the following actual values:

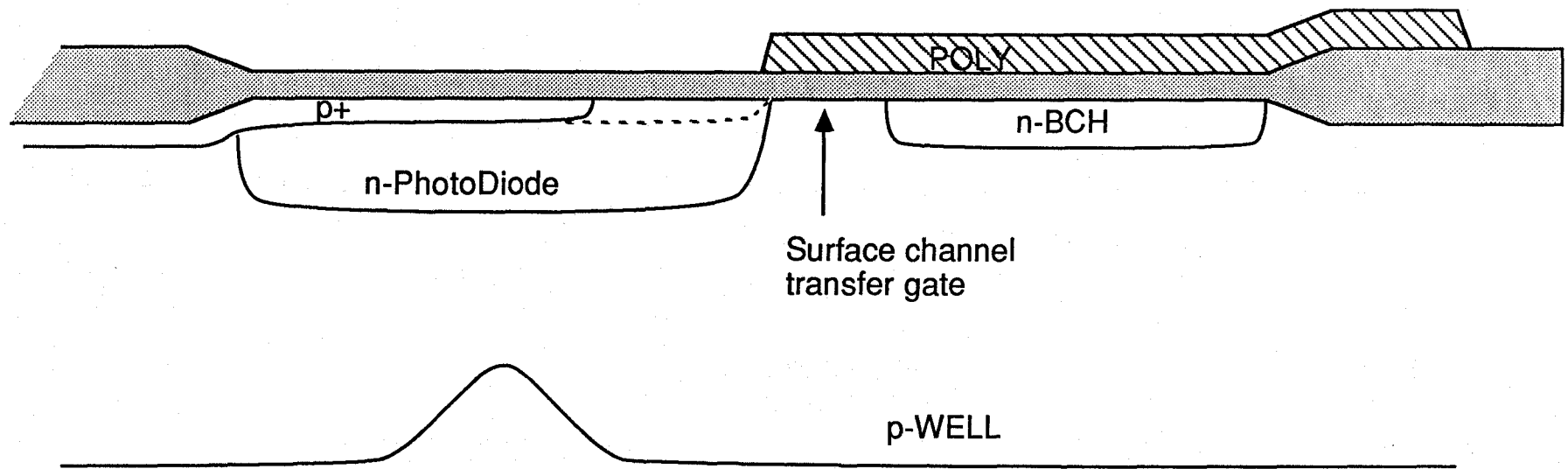
Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

- Ground V_{SS} with a 390Ω resistance.
- 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins.
Test ground all the pins other than those under test.
- 2) Current flowing to the ground when a voltage of 25 V is applied to V_{φ1}, V_{φ2}, V_{φ3}, V_{φ4}, H_{φ1} and H_{φ2} pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
- 3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order.
Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
- 4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.



PIXEL CROSS-SECTION OF
INTERLINE CCD WITH VOD



PIXEL CROSS-SECTION OF
INTERLINE CCD WITH VOD

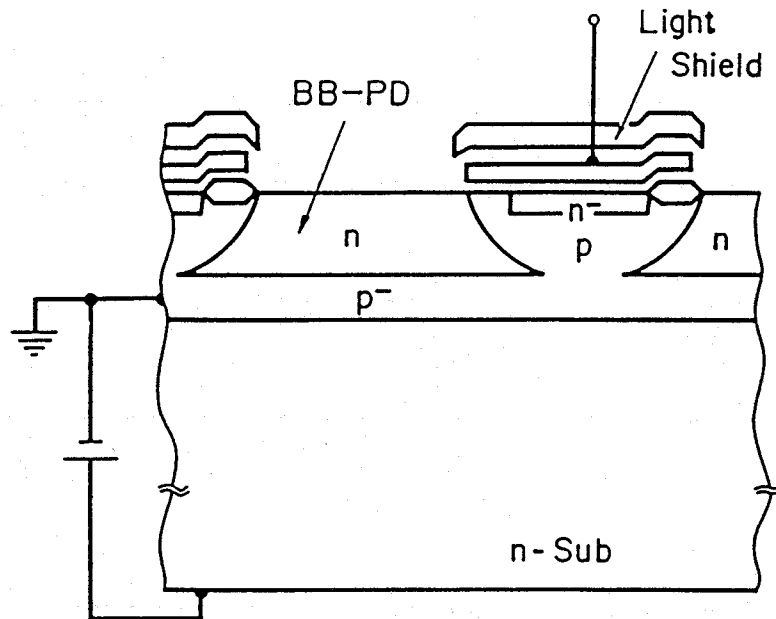
WPM 9.1: A Smear-Suppressing CCD Imager

Takao Kuroda, Toshihiro Kuriyama, Yuji Matsuda, Toshiyuki Kozono, Shigenori Matsumoto,

Yoshimitsu Hiroshima, Kenji Horii

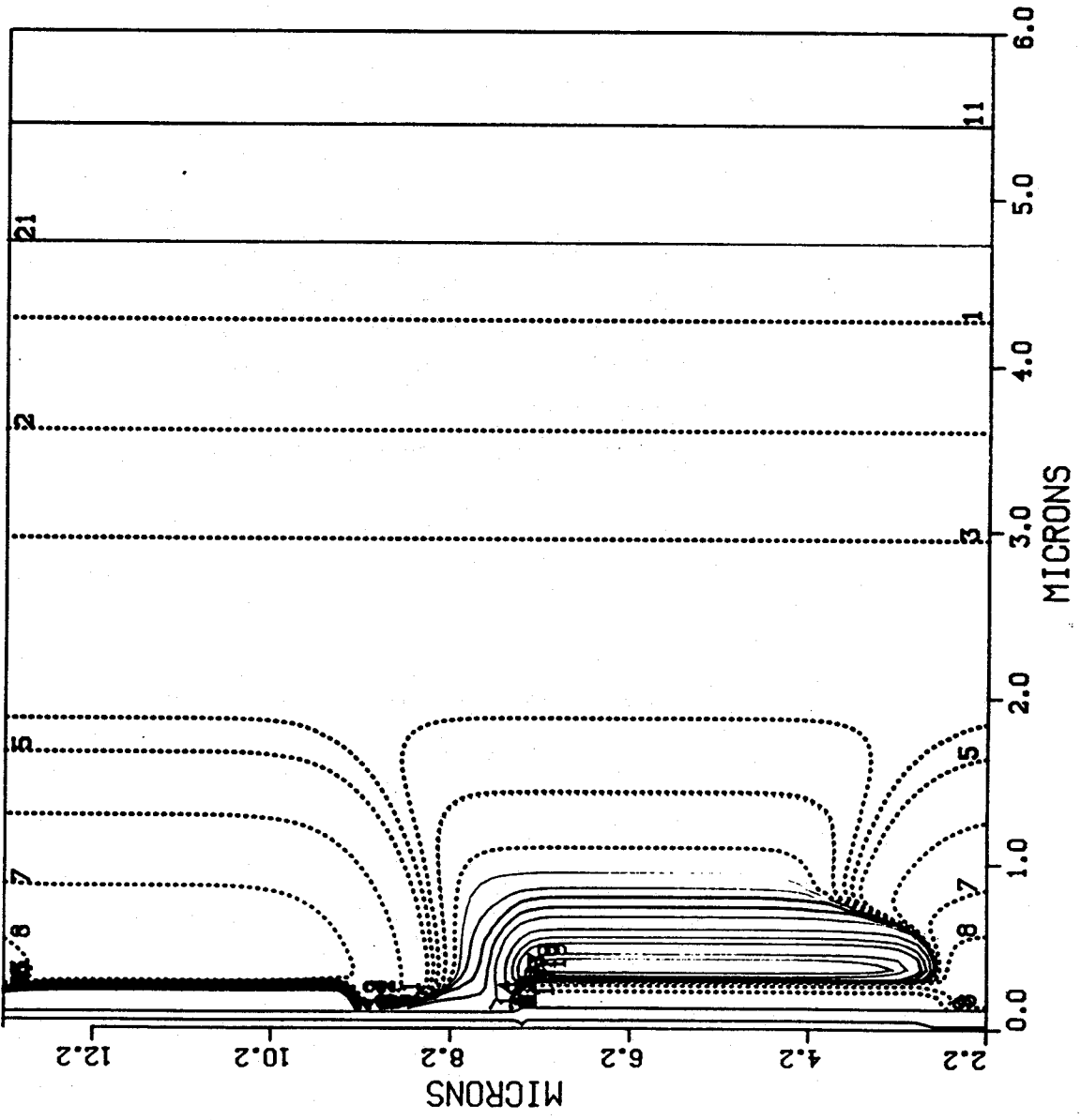
Masushita Semiconductor Laboratory

Osaka, Japan



ISSCC 86

SUPRA 6/5/88



- | | |
|----|-----------------------|
| 1 | 1.00x10 ⁻⁴ |
| 2 | 3.00x10 ⁻⁴ |
| 3 | 5.00x10 ⁻⁴ |
| 4 | 7.00x10 ⁻⁴ |
| 5 | 1.00x10 ⁻³ |
| 6 | 3.00x10 ⁻³ |
| 7 | 1.00x10 ⁻³ |
| 8 | 3.00x10 ⁻³ |
| 9 | 1.00x10 ⁻² |
| 10 | 3.00x10 ⁻² |
| 11 | 1.00x10 ⁻¹ |
| 12 | 3.00x10 ⁻¹ |
| 13 | 1.00x10 ⁰ |
| 14 | 3.00x10 ⁰ |
| 15 | 1.00x10 ¹ |
| 16 | 2.00x10 ¹ |
| 17 | 3.00x10 ¹ |
| 18 | 5.00x10 ¹ |
| 19 | 6.00x10 ¹ |
| 20 | 7.00x10 ¹ |
| 21 | 1.00x10 ² |

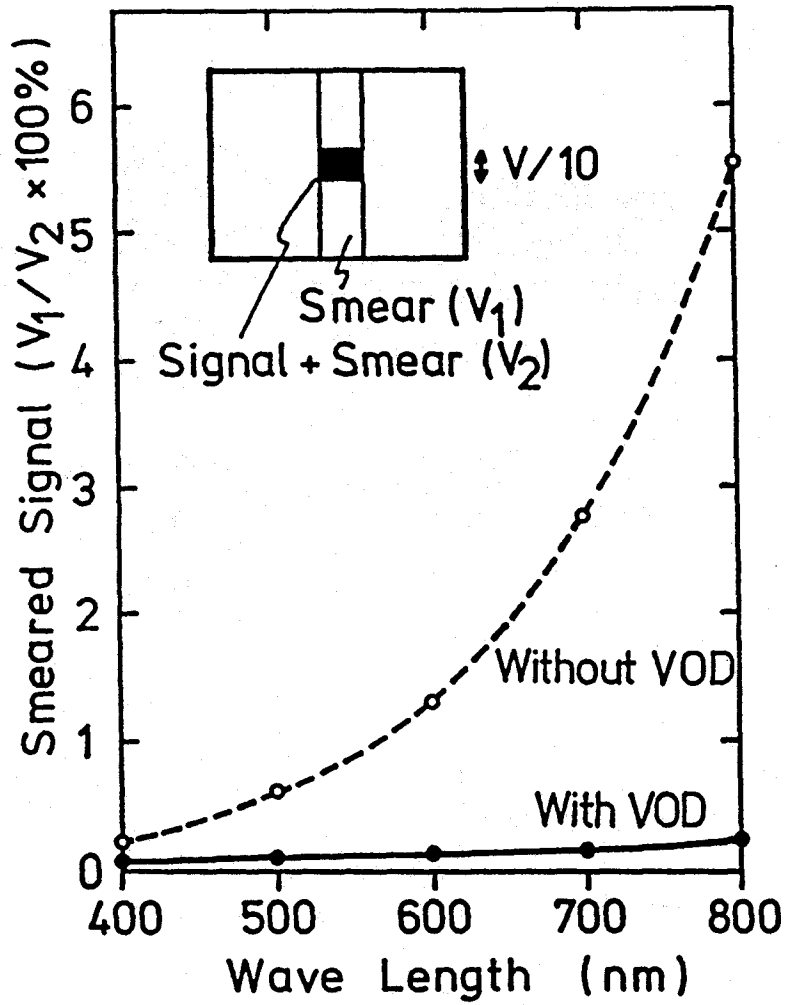


FIGURE 5—Percentages of smeared signal as a function of incident light wavelength.

Ishihara / NEC

ISSCC 82

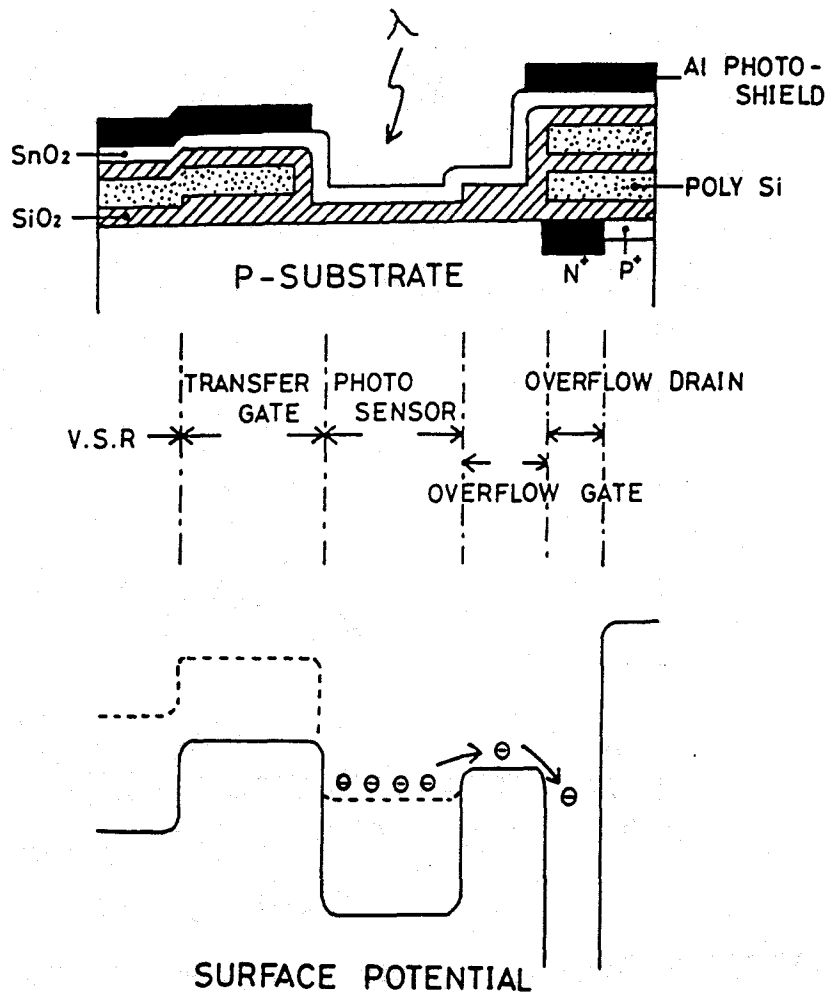


FIGURE 3—Cross sectional view and surface potential of antiblooming system.

Matsumoto et al / SONY

ISSCC 1978

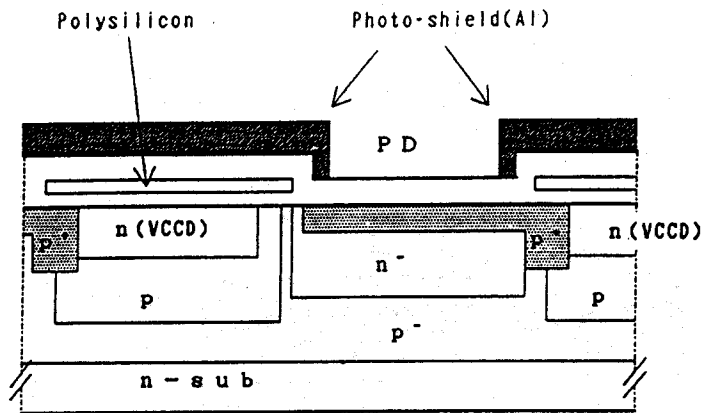


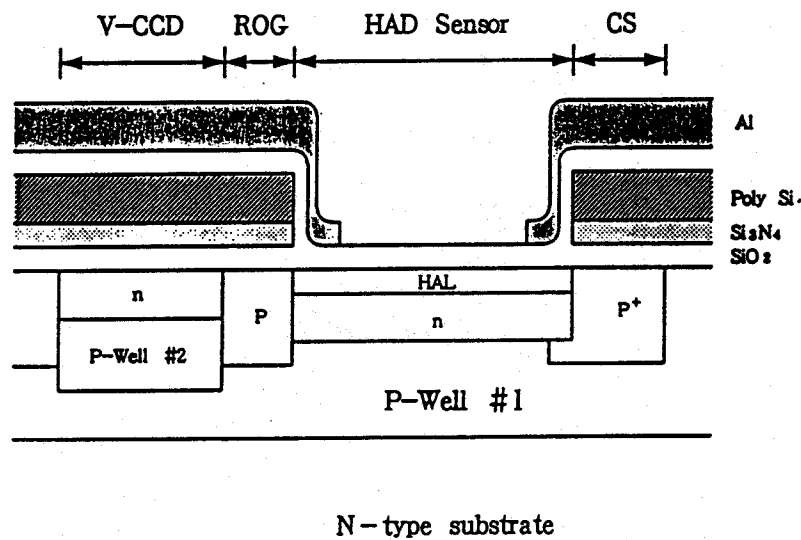
Fig. 5. Cross-sectional view of a unit cell.

Kuriyama et al

IEEE Trans

ED-38

May 1991



Hajo et al

IEEE Trans

ED-38

May 1991

Fig. 3. Schematic cross-sectional view of the unit cell.

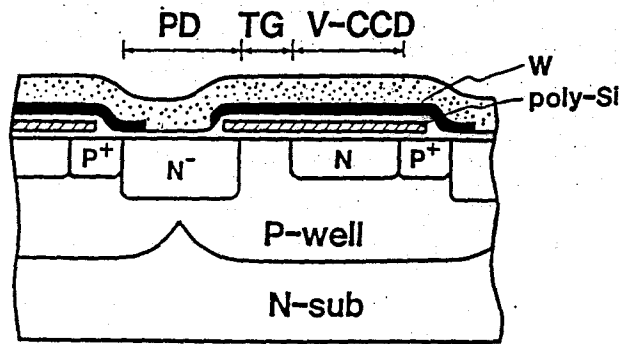
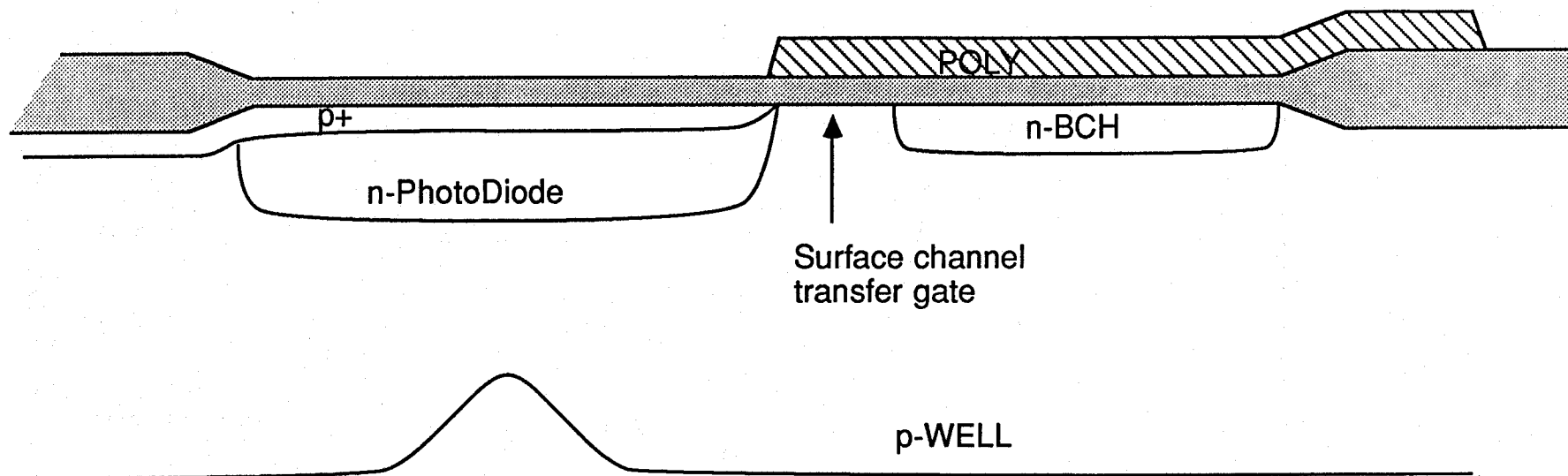


Fig. 5. Cross-sectional view of a unit pixel.

Toyoda et al

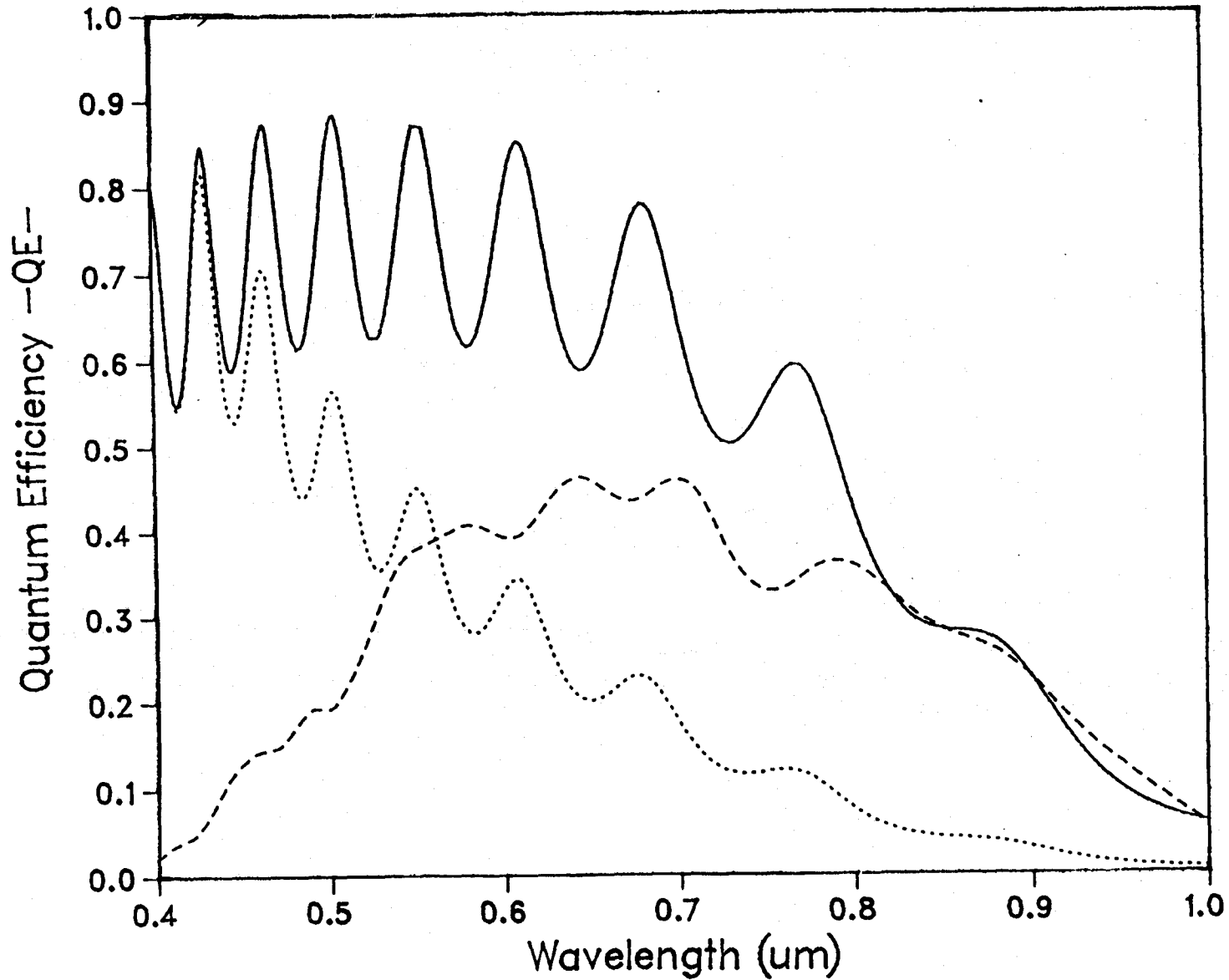
IEEE Trans ED-38

May 1991



PIXEL CROSS-SECTION OF
INTERLINE CCD WITH VOD

IL and FF Quantum Efficiency With 100% Fill Factor



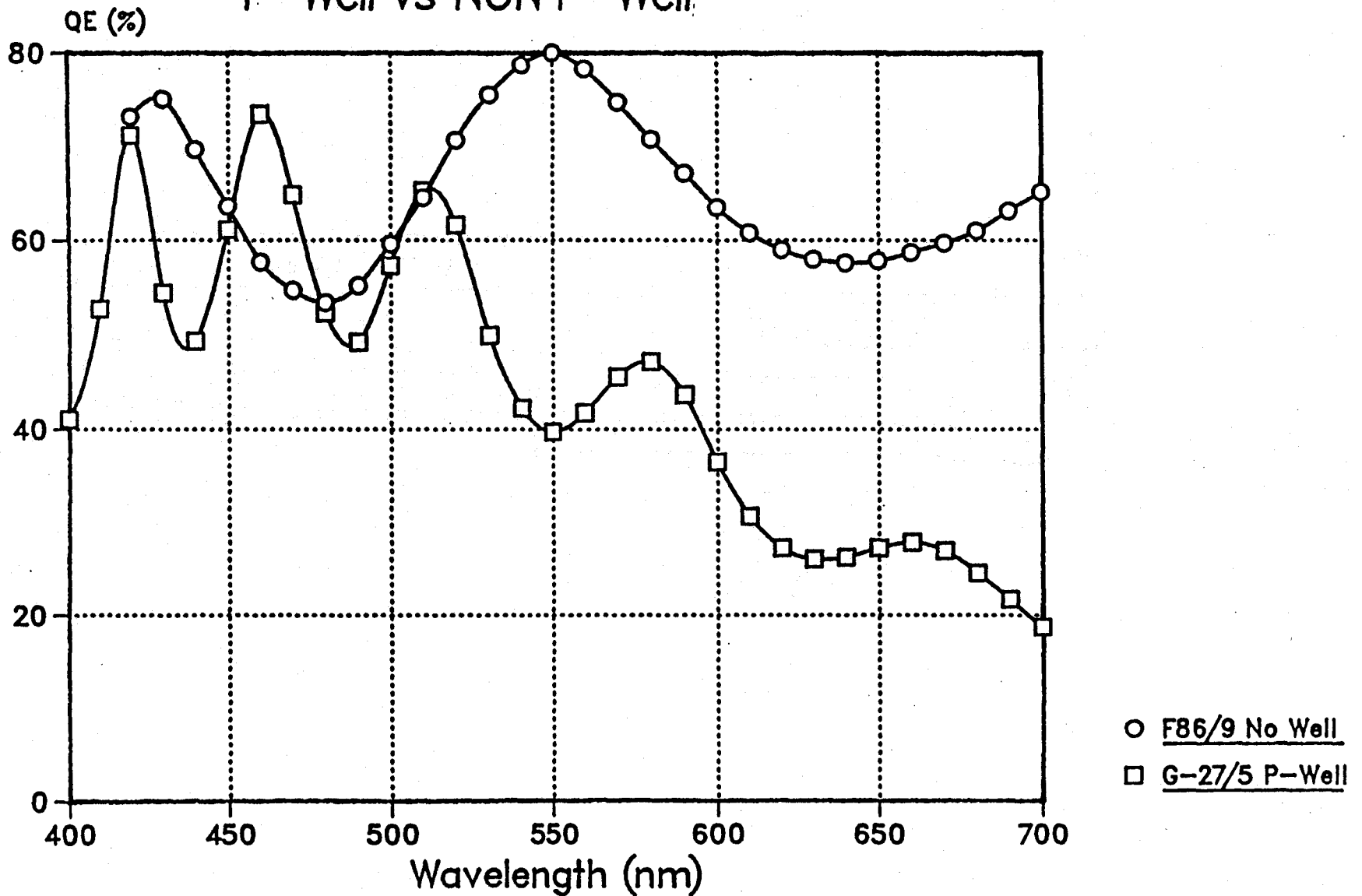
Legend

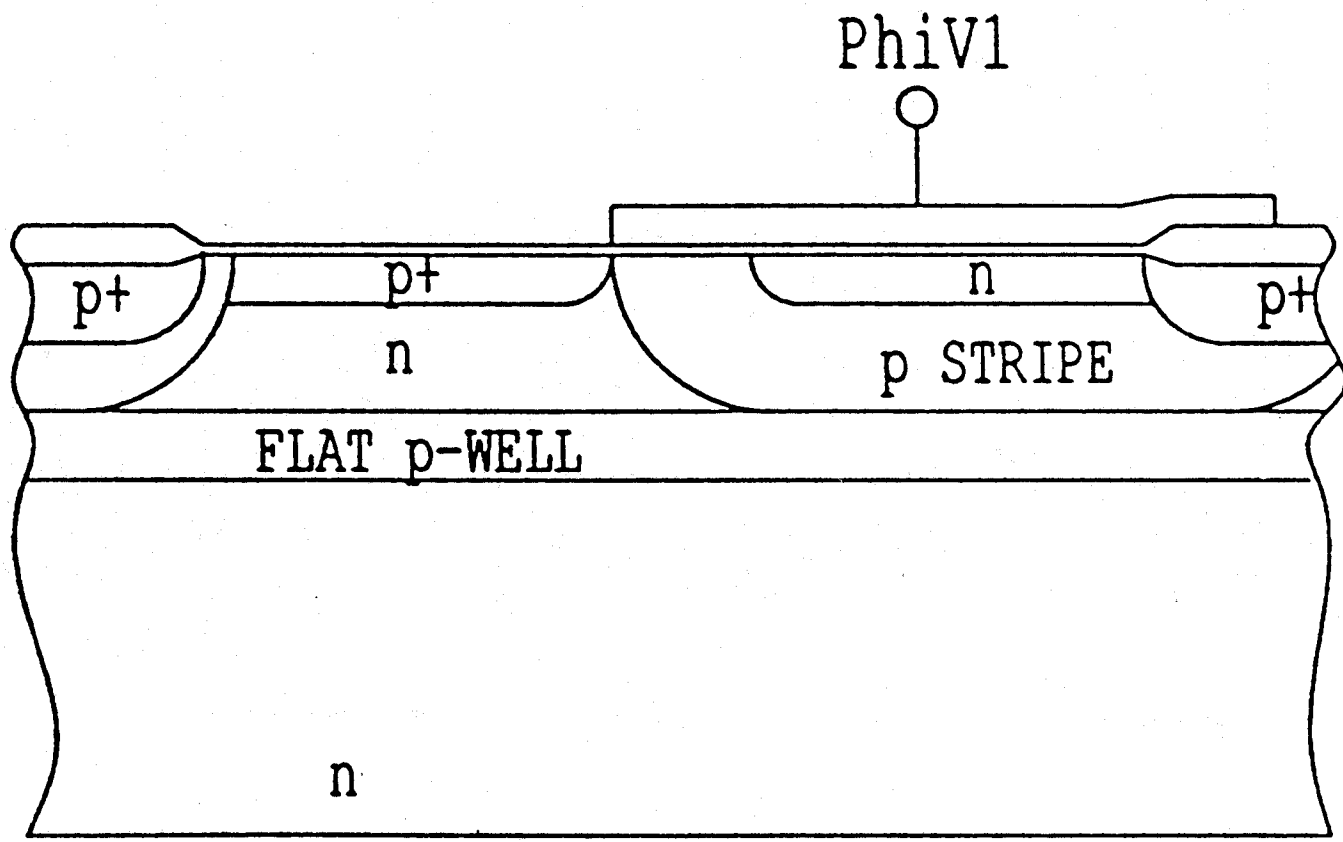
IL w/o p-well

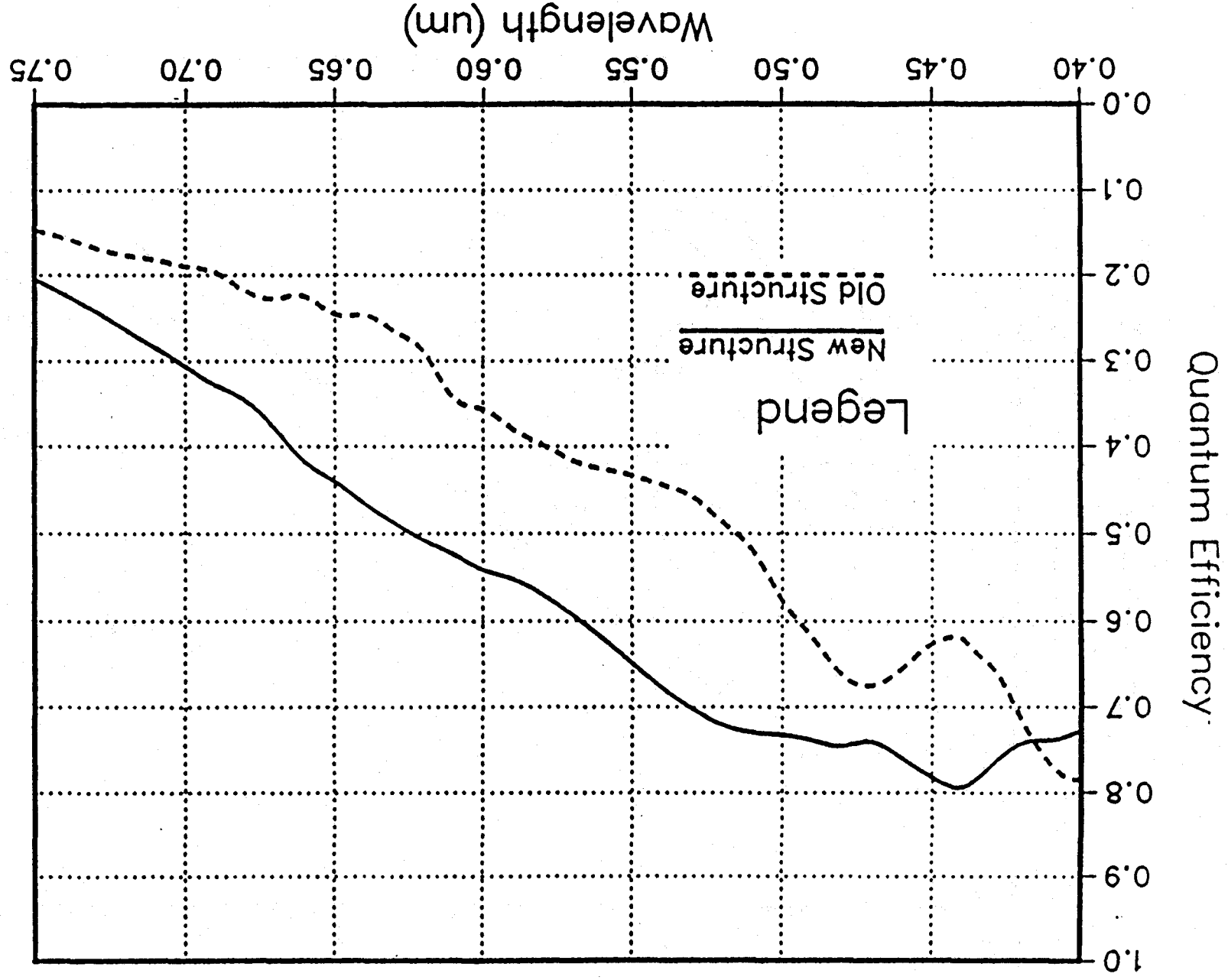
IL w/ p-well

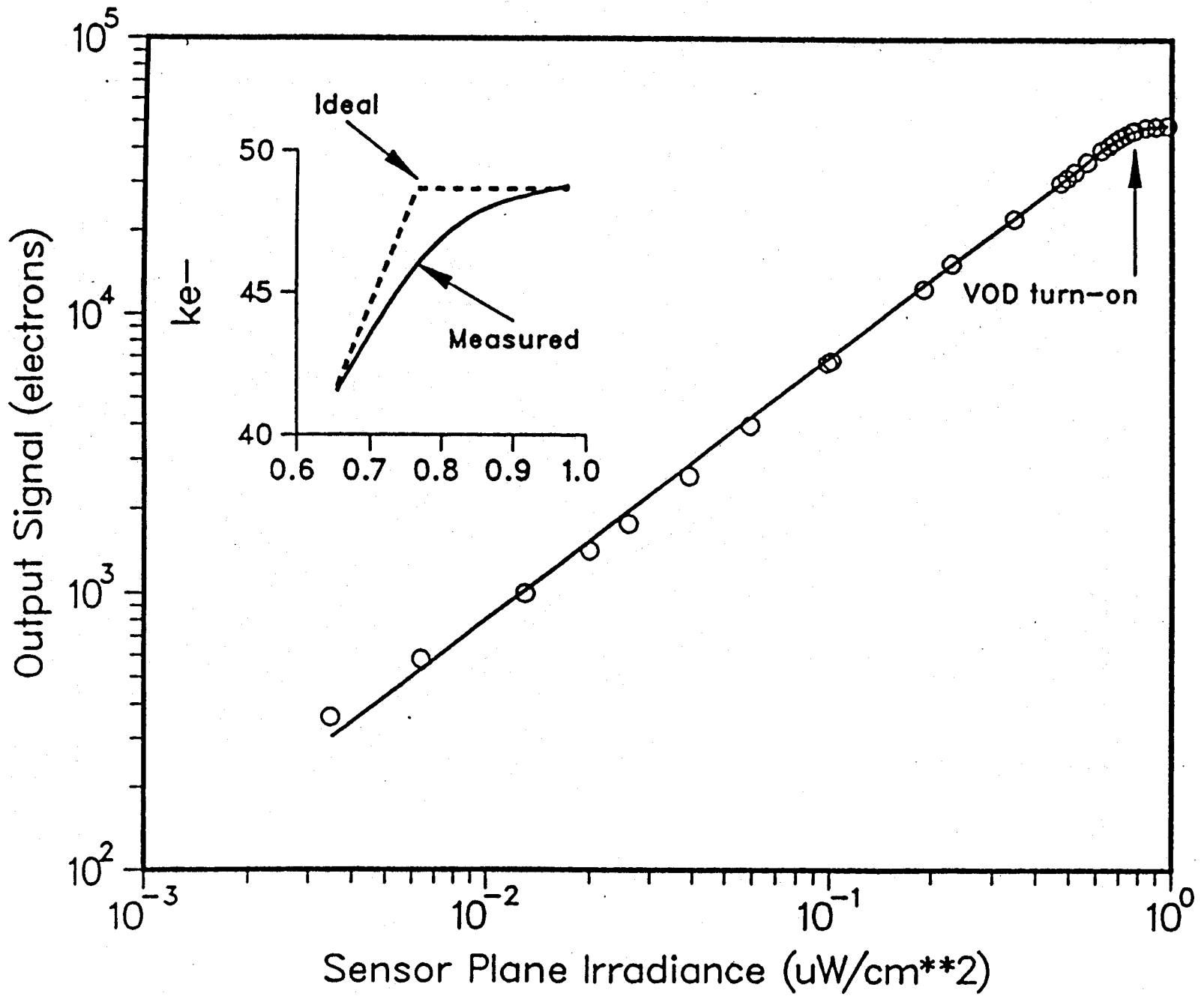
FF w/o p-well

PHOTODIODE ABSOLUTE QUANTUM EFFICIENCY DATA 6/11/86
P-Well vs NON P-Well



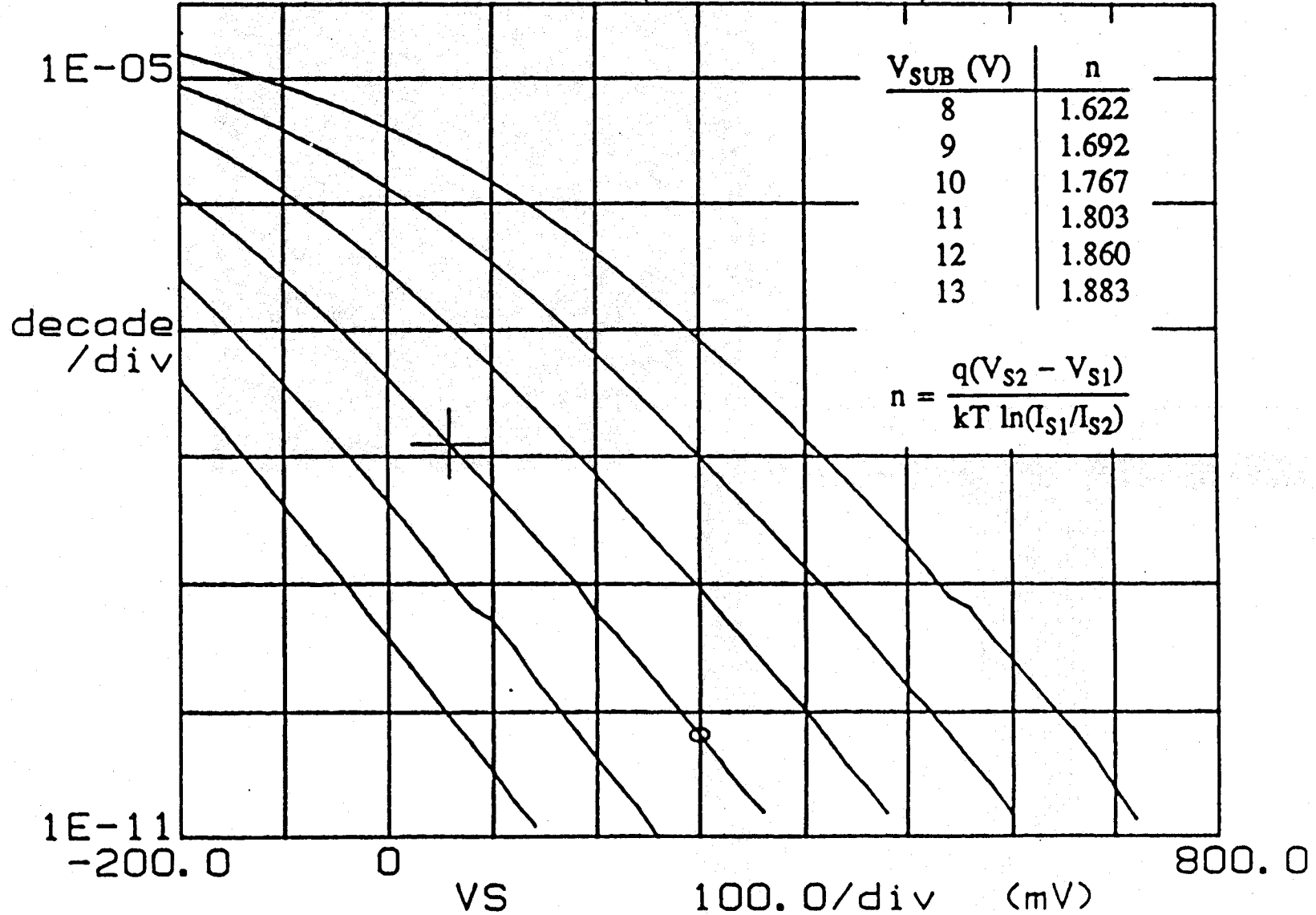


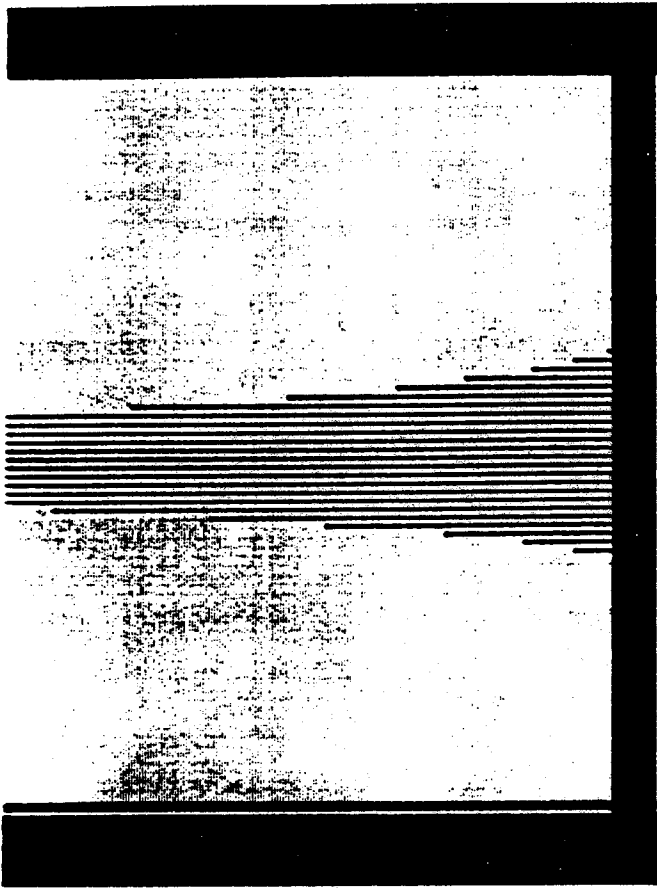




ISS

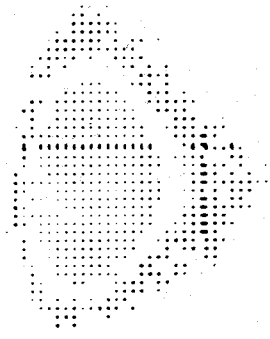
(A) CURSOR (.0600V ; 12.6E-09,)
MARKER (.3000V ; 66.0E-12,)





N29A.I08 HISTOGRAM

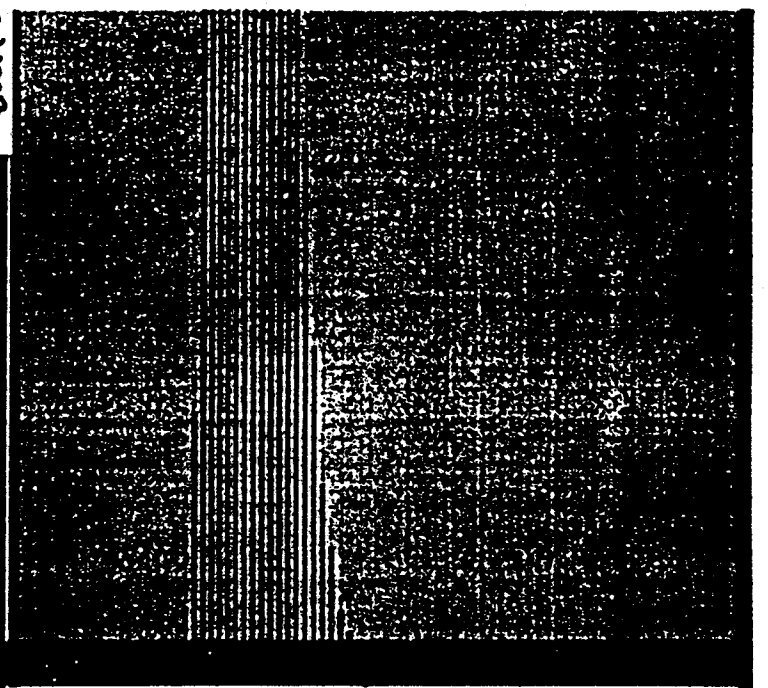
PD vs CCD DARK PATTERN CORRELATION 2/28



PHOTODIODE DARK PATTERN

2/28/89

20093



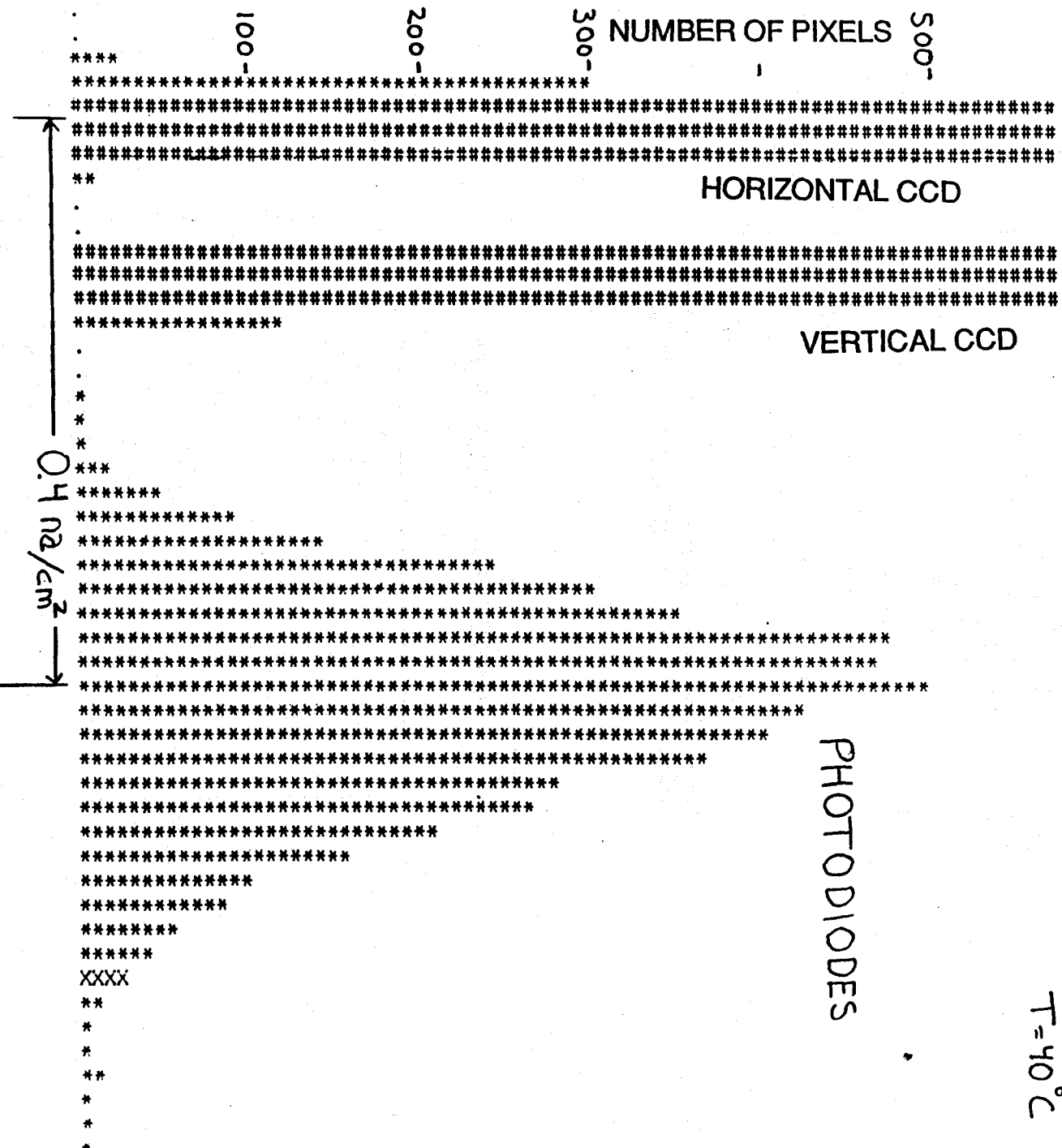
N29A.I08 HISTOGRAM

DARK CURRENT HISTOGRAM

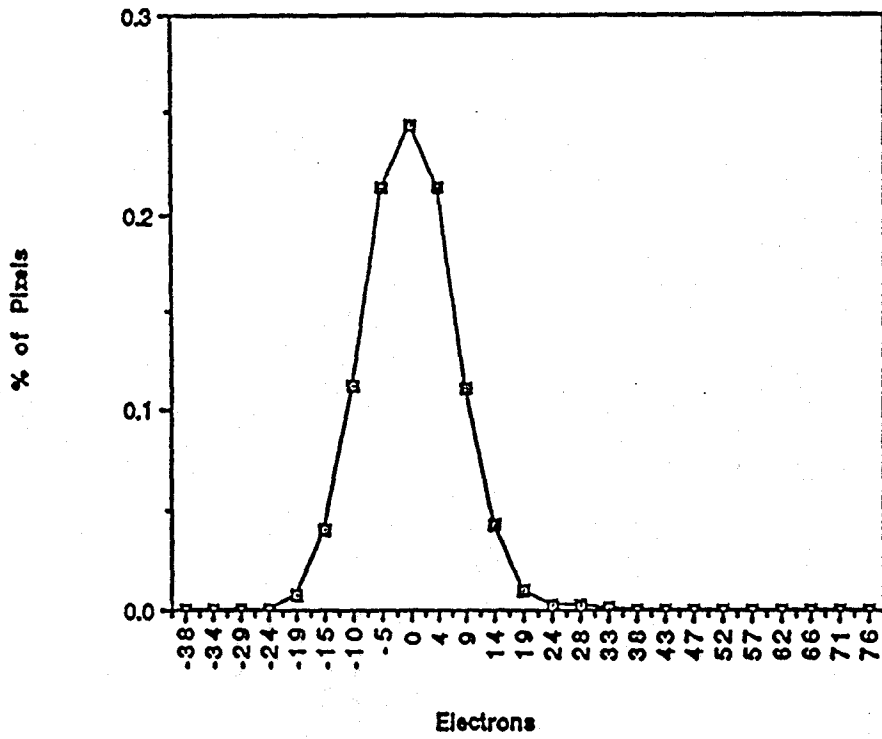
NUMBER OF PIXELS WITH A GIVEN DARK CURRENT VERSUS DARK CURRENT

TRUNCATED

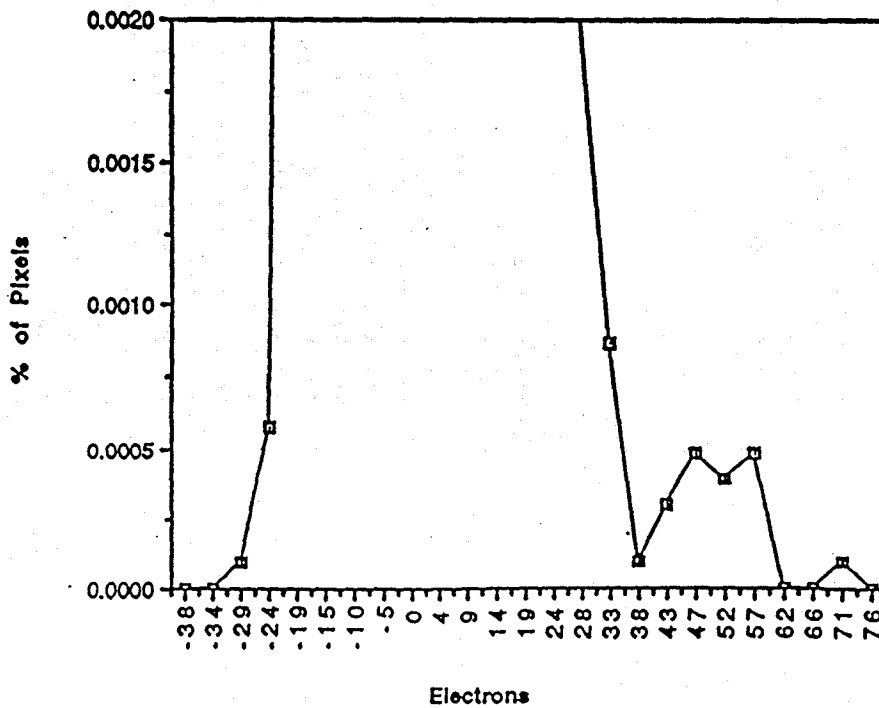
T = 40°C



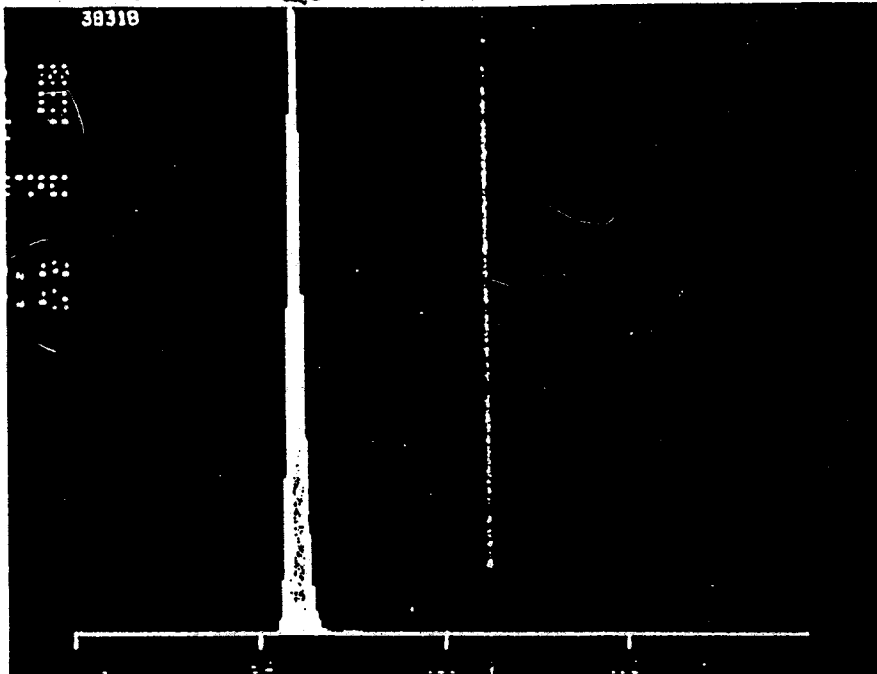
**DARK CURRENT PATTERN NOISE
AT 40°C**



**DARK CURRENT PATTERN NOISE
AT 40°C**

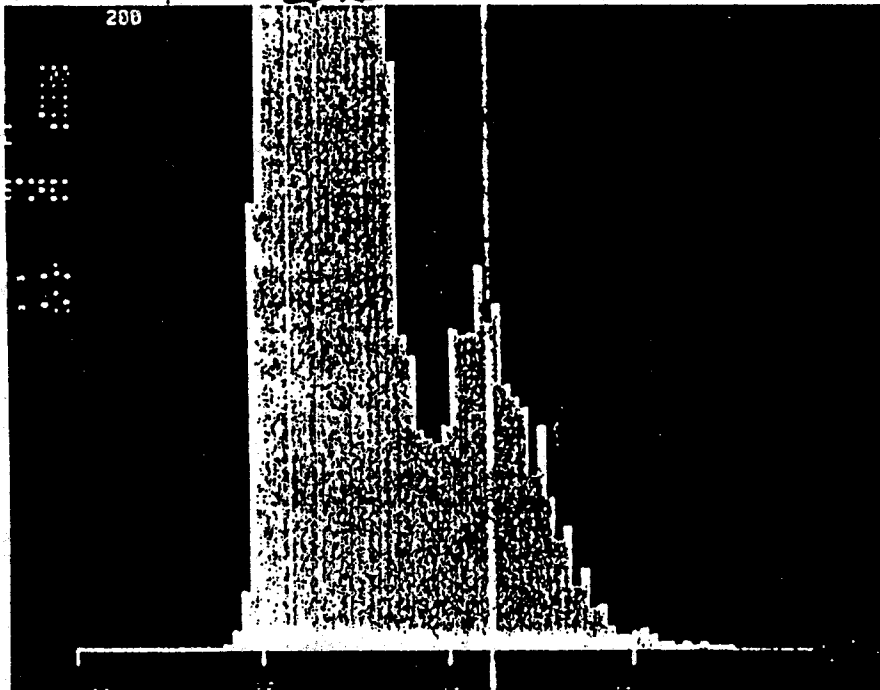


N-32 #20 25:25



- TOTAL DISTRIBUTION - PEAK = 30,318.

N-32 #20 23:23



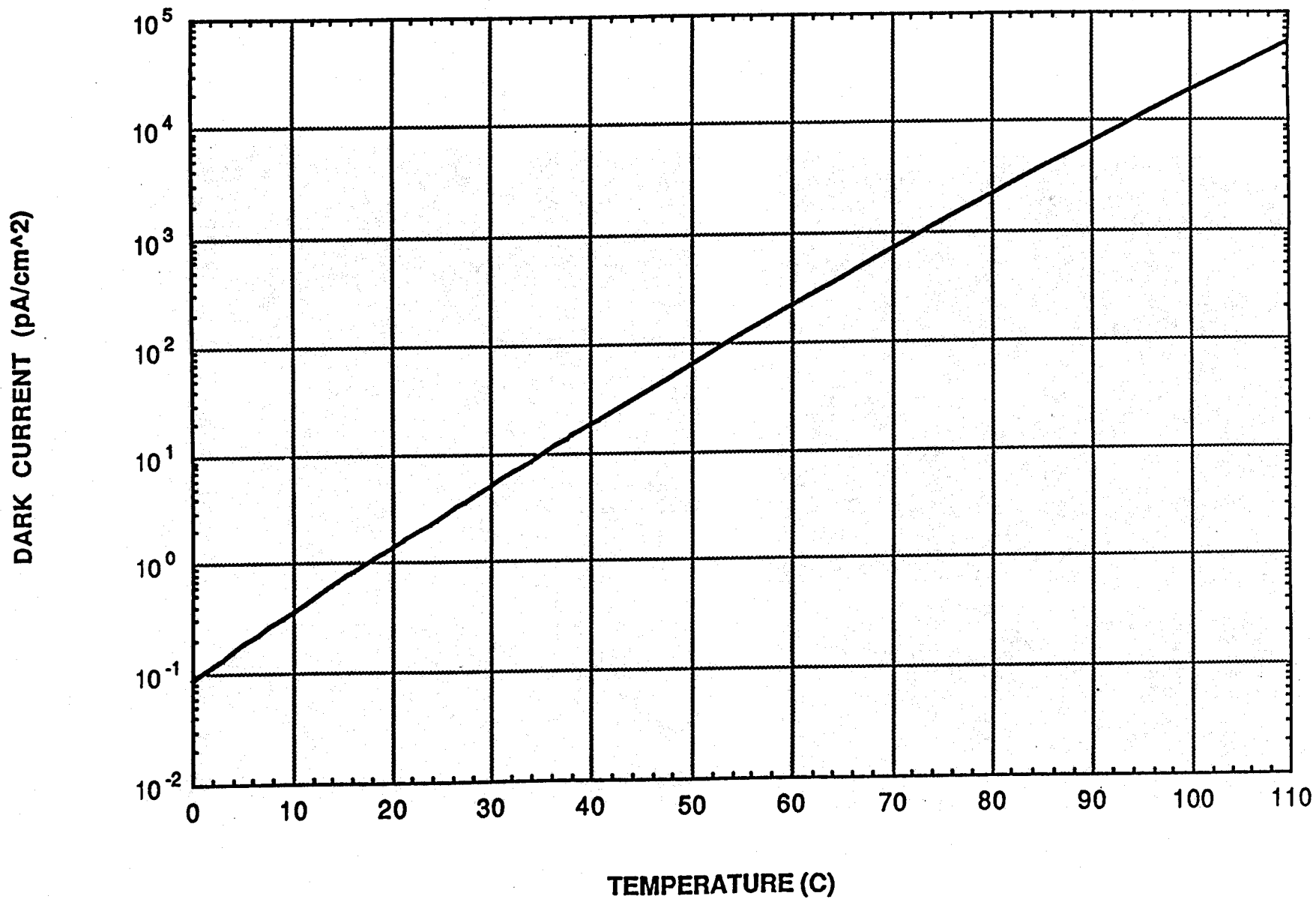
- "BLOW-UP" OF BASE - CLIPPED AT 200.

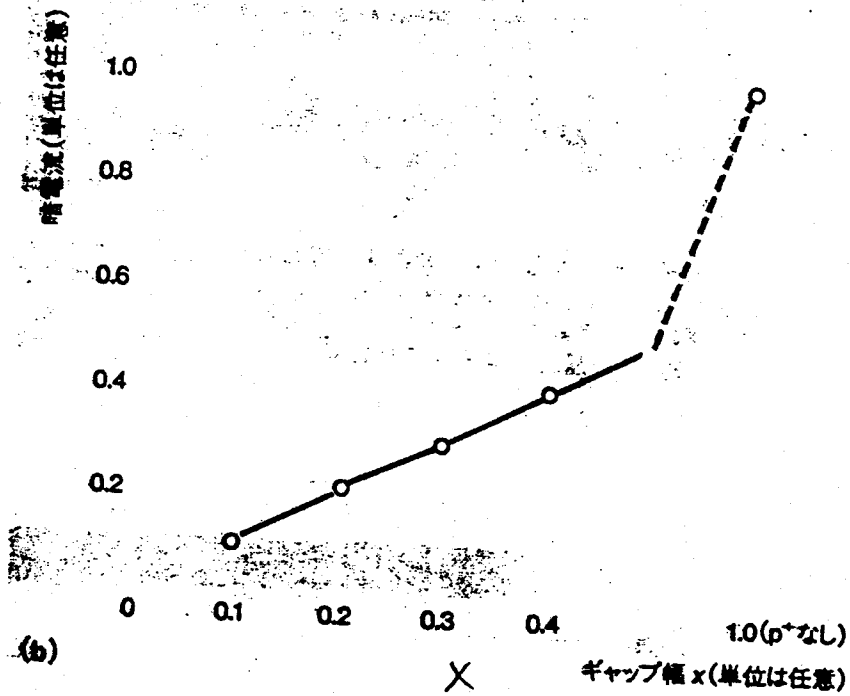
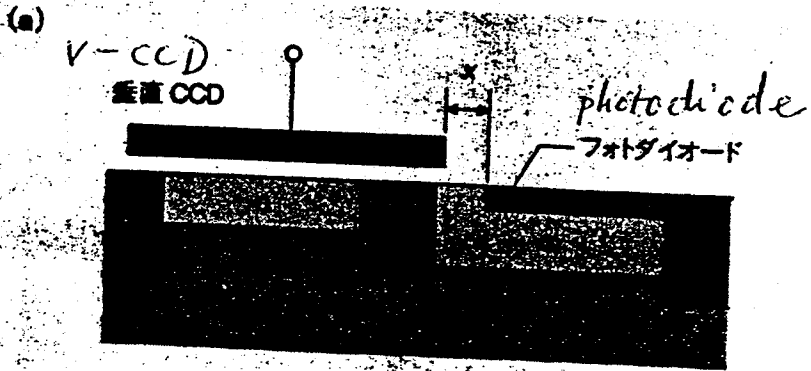
$$J_D = 0.46 \text{ nA/cm}^2$$

$$\text{PTS.} = 110/1492$$

KAF-1400

DARK CURRENT vs TEMPERATURE





Airoshima / Matsushita

Nikkei Microdevice Nov. 88

SUMMARY