DESIGN AND PERFORMANCE CONSIDERATIONS OF CCD'S FOR USE IN ACOUSTO-OPTICAL CHANNELIZERS

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CCD'S DESIGNED FOR ACOUSTO-OPTICAL CHANNELIZERS FACE SOME OF THE MOST DEMANDING PERFORMANCE REQUIREMENTS. THIS WORKSHOP REVIEWS COMPRESSIVE DETECTOR ARCHITECTURES, PERFORMANCE AND DESIGN ISSUES RELATED TO SUCH HIGH PERFORMANCE IMAGERS, AND ALSO DESCRIBES METHODS OF ON-FPA SIGNAL PROCESSING.

ACKNOWLEDGEMENTS

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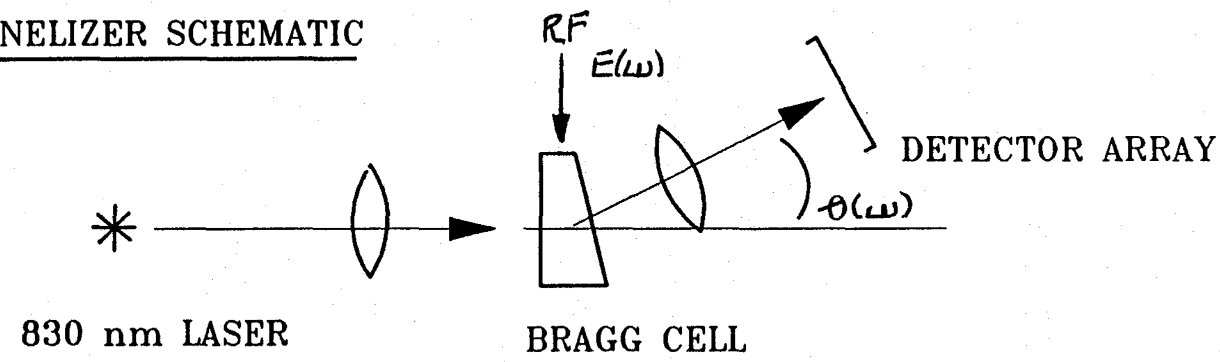
APPLICATION

CHANNELIZER SCHEMATIC



DETECTOR REQUIREMENTS:

* HIGH DYNAMIC RANGE: > 50 dB
* LOW NOISE
* FAST READOUT ~1 uS
* CROSS-TALK IMMUNITY THROUGHOUT DEVICE
* TEMPORAL AND SPATIAL RESPONSE UNIFORMITY

LINEAR DETECTOR ARRAYS FOR AO CHANNELIZERS

SERIAL-ADDRESSED (CCDs) VERSUS PARALLEL-ADDRESSED (INSTANTANEOUS)

ADVANTAGES OF SERIAL-ADDRESSED:

- LOW PIN COUNT
- LOW CHANNEL CROSSTALK
- REDUCED ARRAY POWER DISSIPATION
- REDUCED SYSTEM POWER DISSIPATION
- INCREASED SIGNAL RESOLUTION
- IMPROVED SENSITIVITY

ADVANTAGES OF PARALLEL-ADDRESSED:

- INCREASED TOA RESOLUTION

DETECTOR ARRAY NEAR TERM REQUIREMENTS

SPECIFIC

NO. OF ELEMENTS	12,000
EFFECTIVE SAMPLE RATE	> 10 GHz
DYNAMIC RANGE	10^8
CROSSTALK	
PIXEL–PIXEL	$\lesssim$ −60 dB (2NN)
ALL OTHER	$\lesssim$ PK–PK NOISE
SENSITIVITY	~ 10 pW (1 μs INT.)

GENERAL

VARIABLE INTEGRATION TIMES

LOW POWER DISSIPATION

LOW DRIVE COMPLEXITY

HIGH UNIFORMITY

ON–FPA SIGNAL PRE–PROCESSING

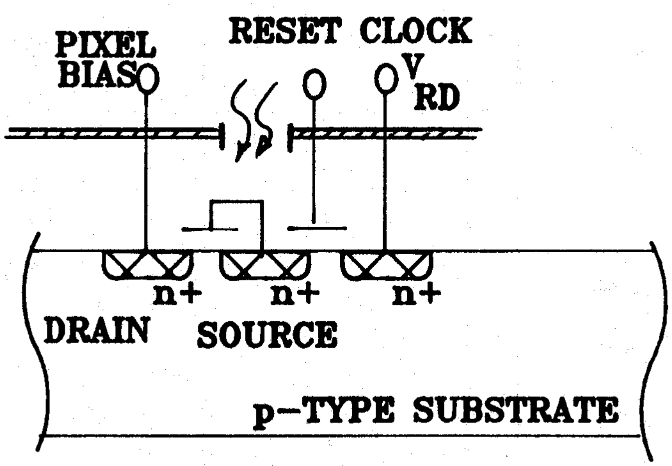
AO DETECTOR ARCHITECTURES

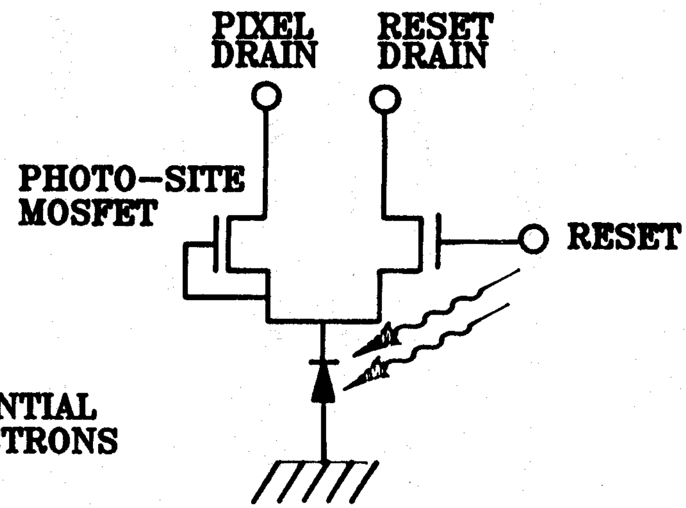
PHOTODETECTORS WITH HIGH SENSITIVITY, WIDE DYNAMIC RANGE, MINIMAL IMAGE LAG AND FAST RESPONSE TIMES ARE NECESSARY FOR MEETING AO SYSTEM REQUIREMENTS. ADDITIONALLY, MINIMUM POWER, SIZE AND DRIVING COMPLEXITY ARE FUNDAMENTAL IN ACHIEVING PRACTICAL SYSTEMS. THE FOLLOWING DETECTOR ARCHITECTURES WILL BE DISCUSSED:

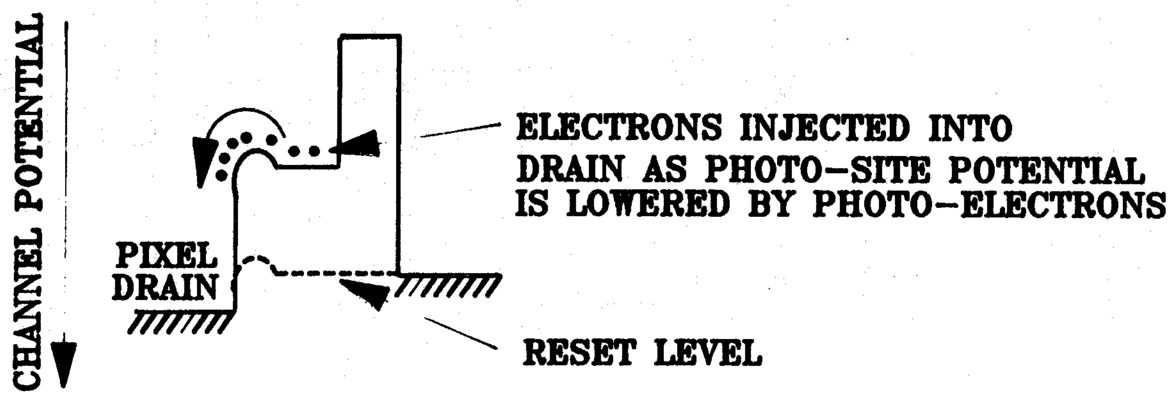
- DYNASENSOR 3
- DYNASENSOR 4
- FLOATING GATE DETECTOR
- CHARGE PARTITION DETECTOR
- CHARGE DIFFUSION DETECTOR
- MULTI-RESPONSE DETECTOR

DALSA PhotoFET

OPTICAL GAIN COMPRESSION







SUBTHRESHOLD CURRENT VERSUS SUBSTRATE VOLTAGE

- Long Channel Subthreshold Current Versus Surface Potential

$$I = (W/L)\mu(kT/q)qN_A L_b (n_i/N_A)^2$$

$$exp(-\beta V_{BS})exp(\beta\phi_{SAT})[1-exp(-\beta V_{DS})](2\beta\phi_{SAT})^{-1/2}$$

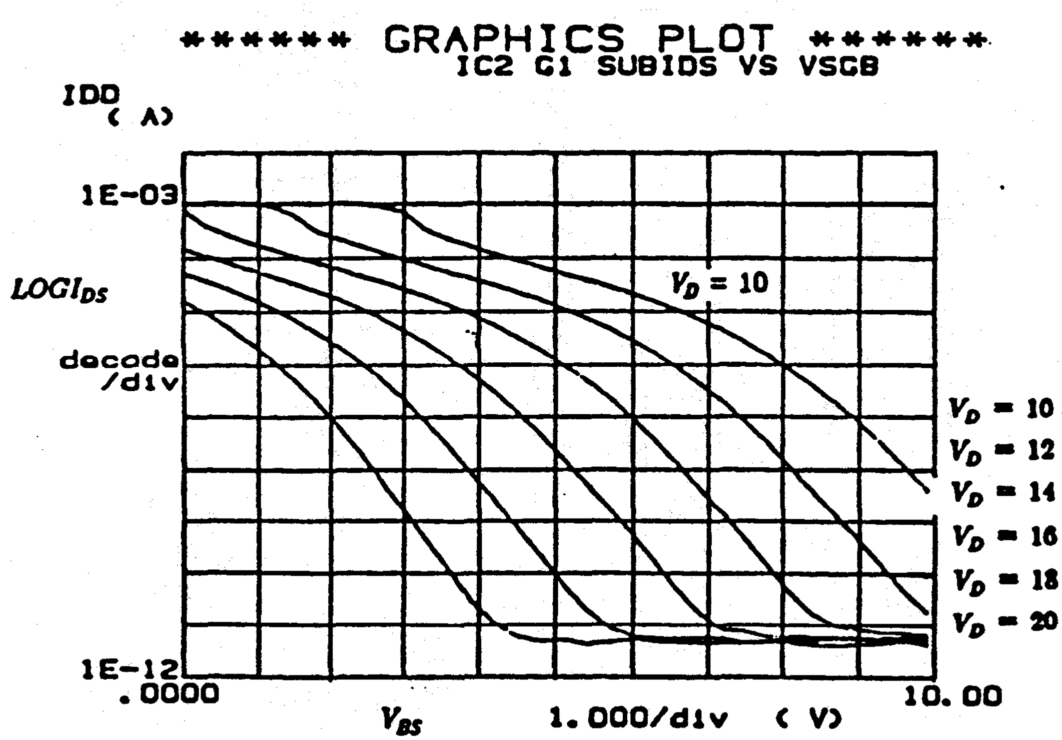
$$\beta\phi_{SAT} = \beta V_{GS} + \beta V_{BS} + a^2/2 - a(\beta V_{GS} + \beta V_{BS} + a^2/4)^{1/2}$$

- Assuming V_{DS} is high, $V_{GS} = 0$ and $a = 1$

$$I \approx K \frac{exp[-(\beta V_{BS} + L)^{1/2}]}{[\beta V_{BS} - (\beta V_{BS} + M)^{1/2}]^{1/2}}$$

where K, L, and M are constants of proportionality.

- Measured Subthreshold Current Versus Substrate Bias



PHOTODETECTOR TRANSIENT RESPONSE MODEL

- Model for Transient Response

$$I_{tot} = C_{pel}\frac{dV_{ph}}{dt} + V_{ph}\frac{dC_{pel}}{dt}$$

- Total Node Current

$$I_{tot} = I_{pc} - I_{ph} - I_{leak}$$

- Total Sense Node Capacitance

$$C_{pel} = C_{fixed} + D\,(V_{ph} + V_{bi})^{-1/2}$$

$$D = Area \times \left(\frac{q\,\varepsilon_s N_A}{2}\right)^{1/2}$$

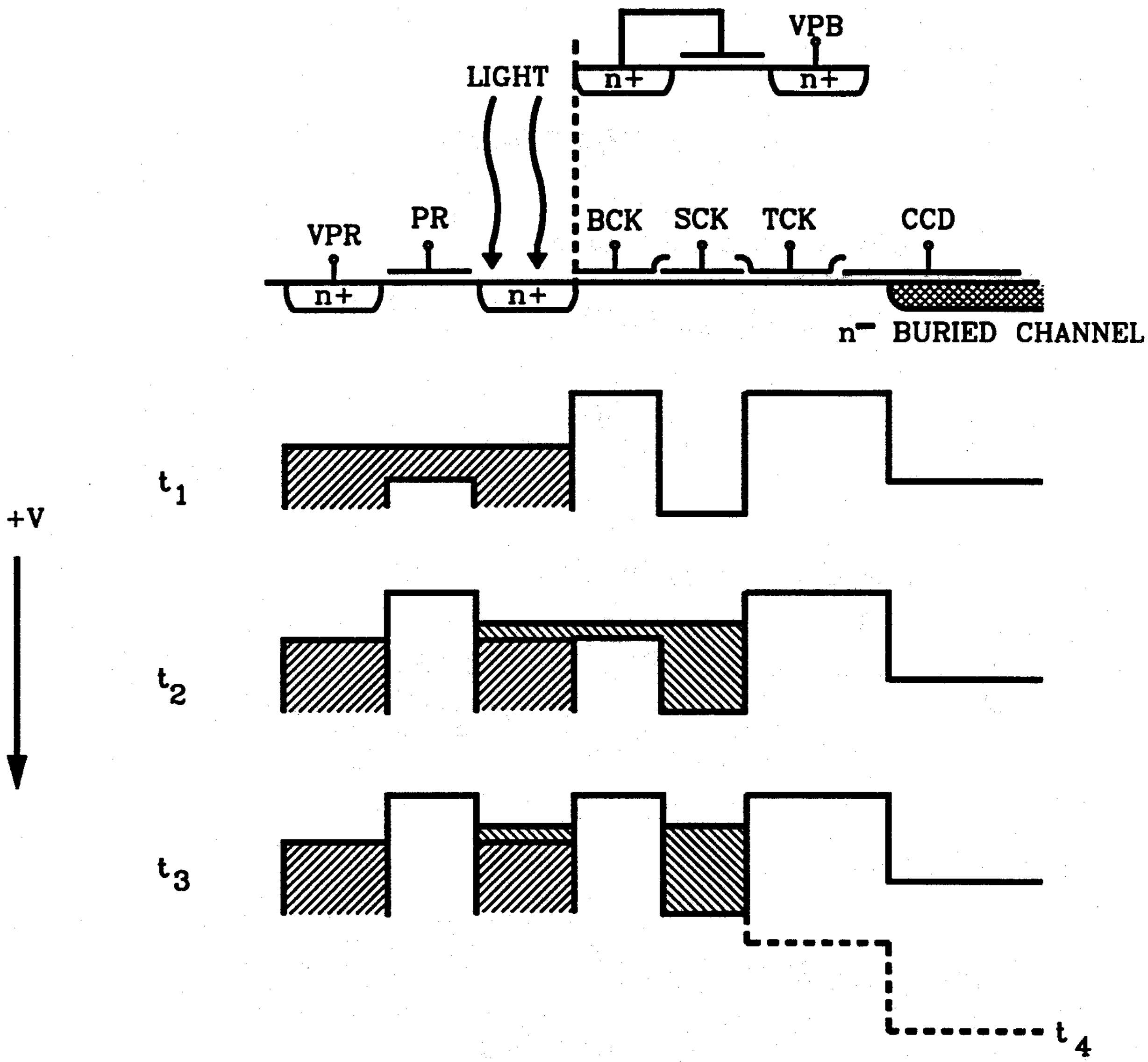
- Final Model after Manipulation

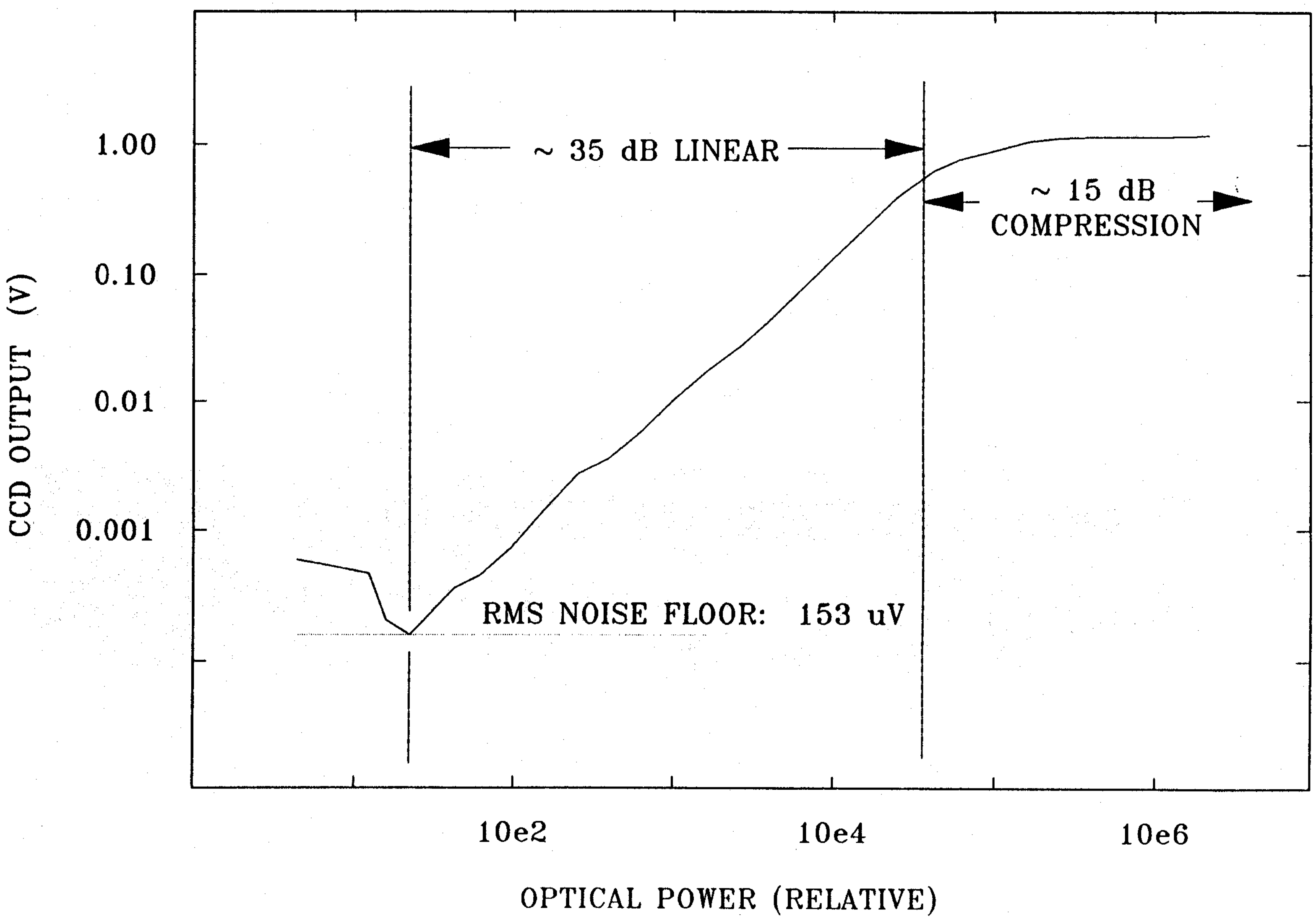
$$\frac{dV_{ph}}{dt} = \frac{I_{pc} - I_{ph} - I_{leak}}{C_{fixed} + D\,(V_{ph} + V_{bi})^{1/2} - \frac{DV_{ph}(V_{ph} + V_{bi})^{-3/2}}{2}}$$

- Resulting Integral

$$\int_0^t dt = \int_{V_{phini}}^{V_{ph}(t)} \frac{C_{fixed} + D\,(V_{ph} + V_{bi})^{1/2} - \frac{DV_{ph}(V_{ph} + V_{bi})^{-3/2}}{2}}{I_{pc} - I_{ph} - I_{leak}}\,dV_{ph}$$

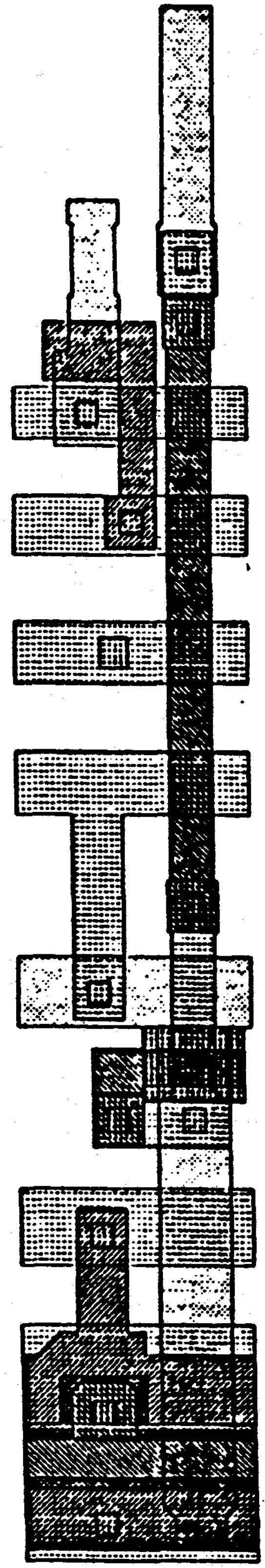
DYNA3 PHOTODETECTOR STRUCTURE



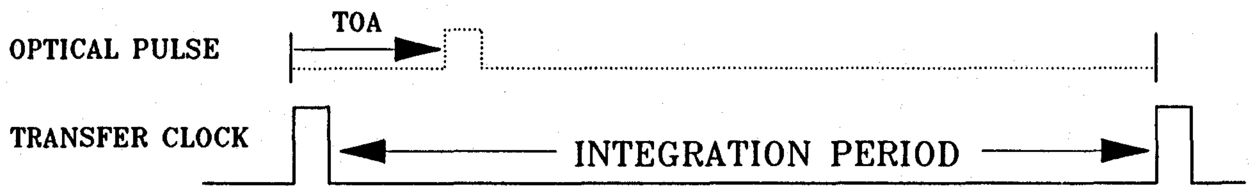


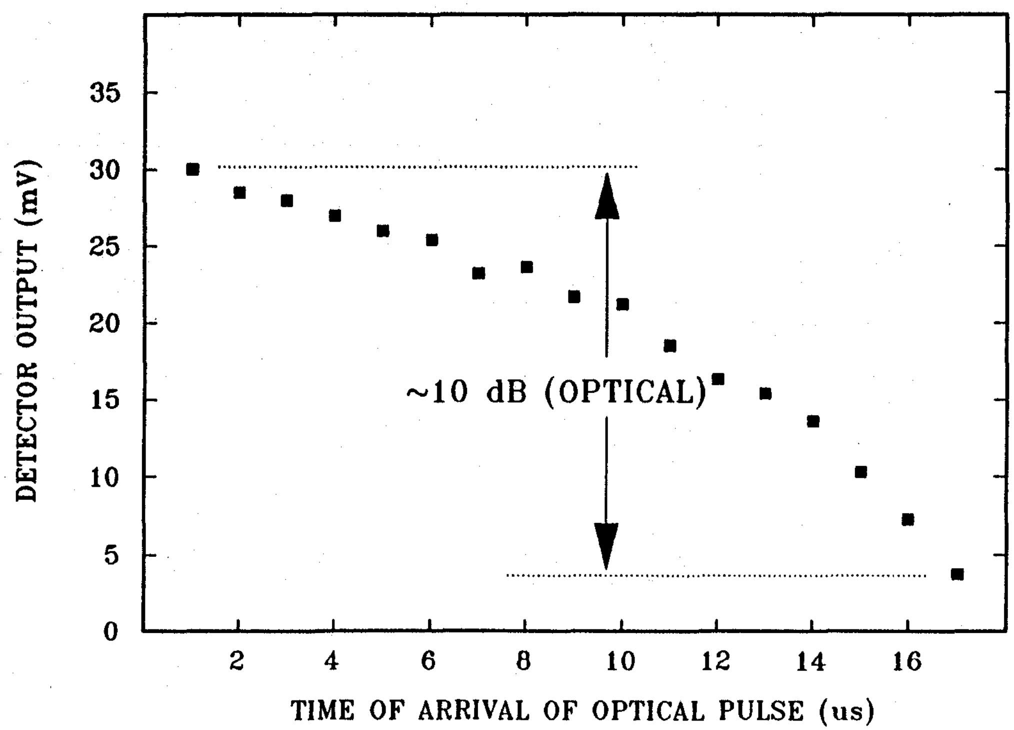
1.00
0.10
0.01
0.001
CCD OUTPUT (V)
~ 35 dB LINEAR
~ 15 dB
COMPRESSION
RMS NOISE FLOOR: 153 uV
10e2
10e4
10e6
OPTICAL POWER (RELATIVE)

DYNA3 PHOTODETECTOR LAYOUT



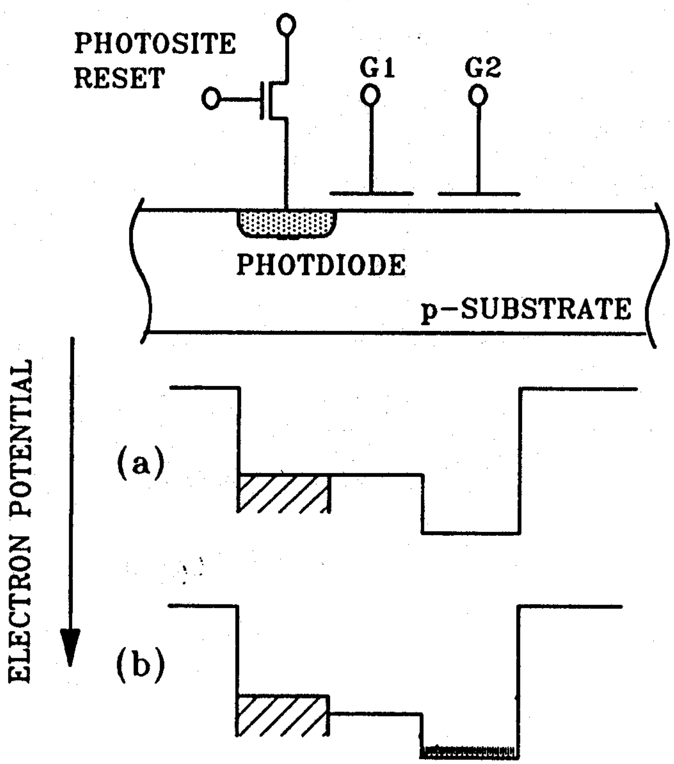
DALSA IL-A3
TEMPORAL RESPONSE

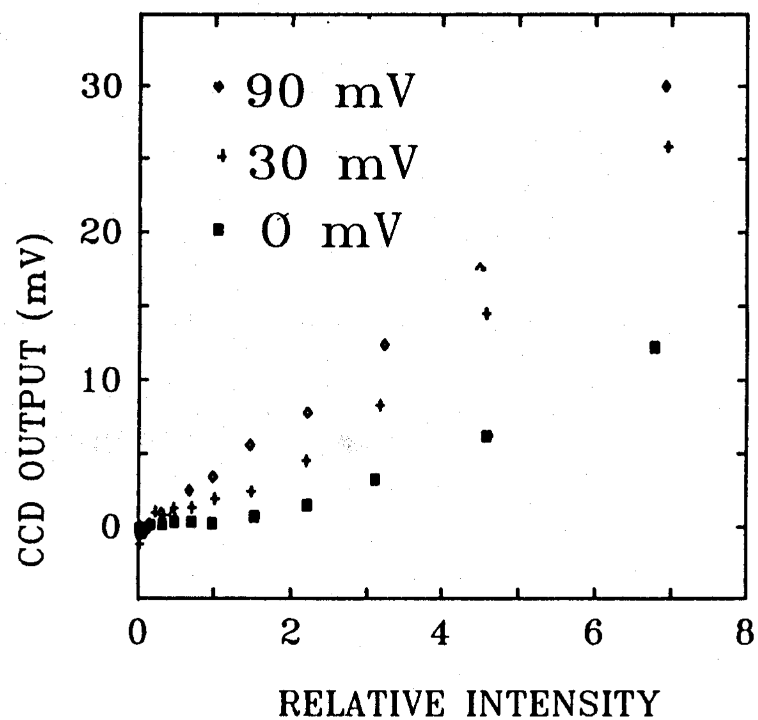




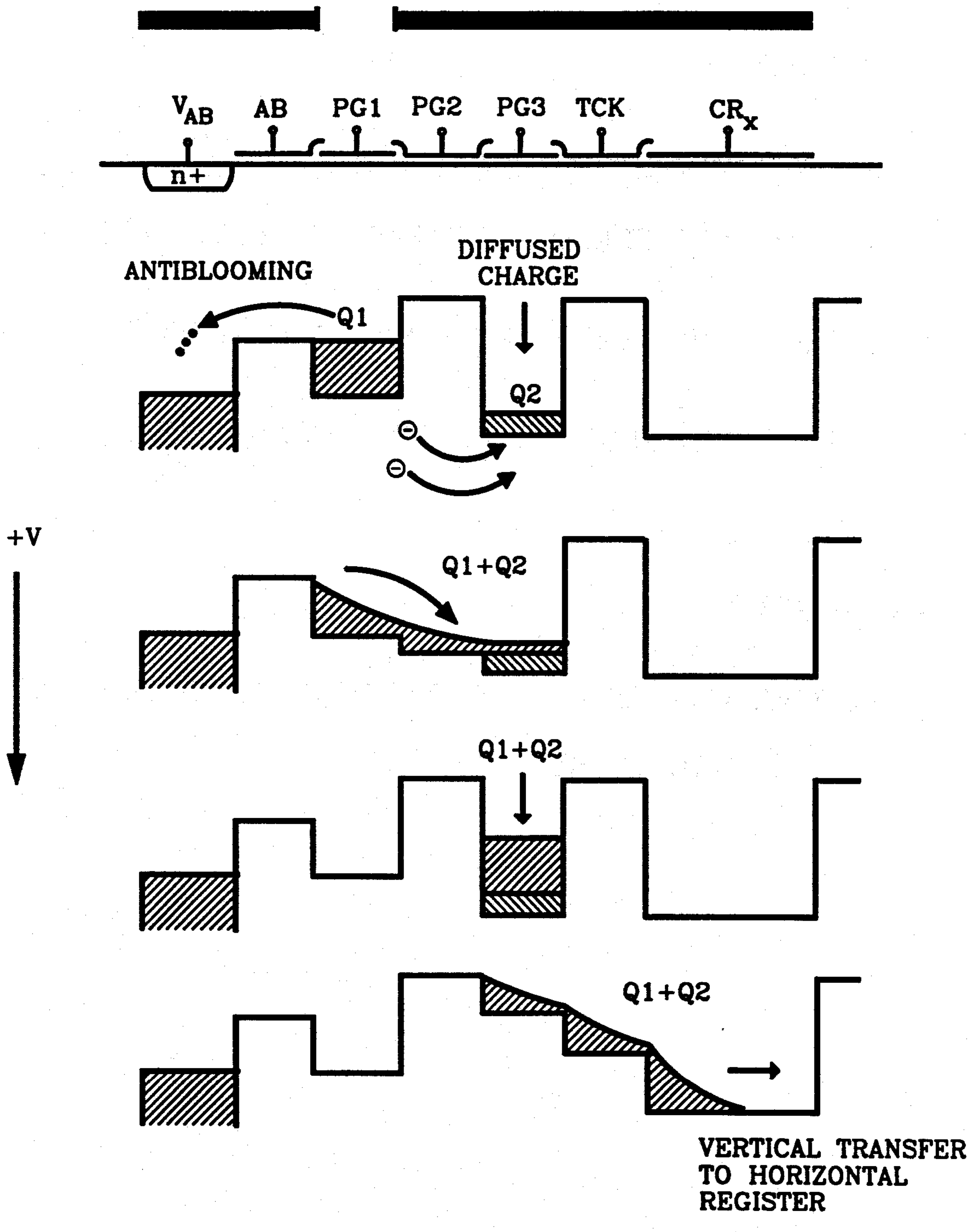
DALSA IL-A3

QUANTUM EFFICIENCY





CHARGE DIFFUSION DETECTOR



CHARGE PARTITION DETECTOR

ADVANTAGES:

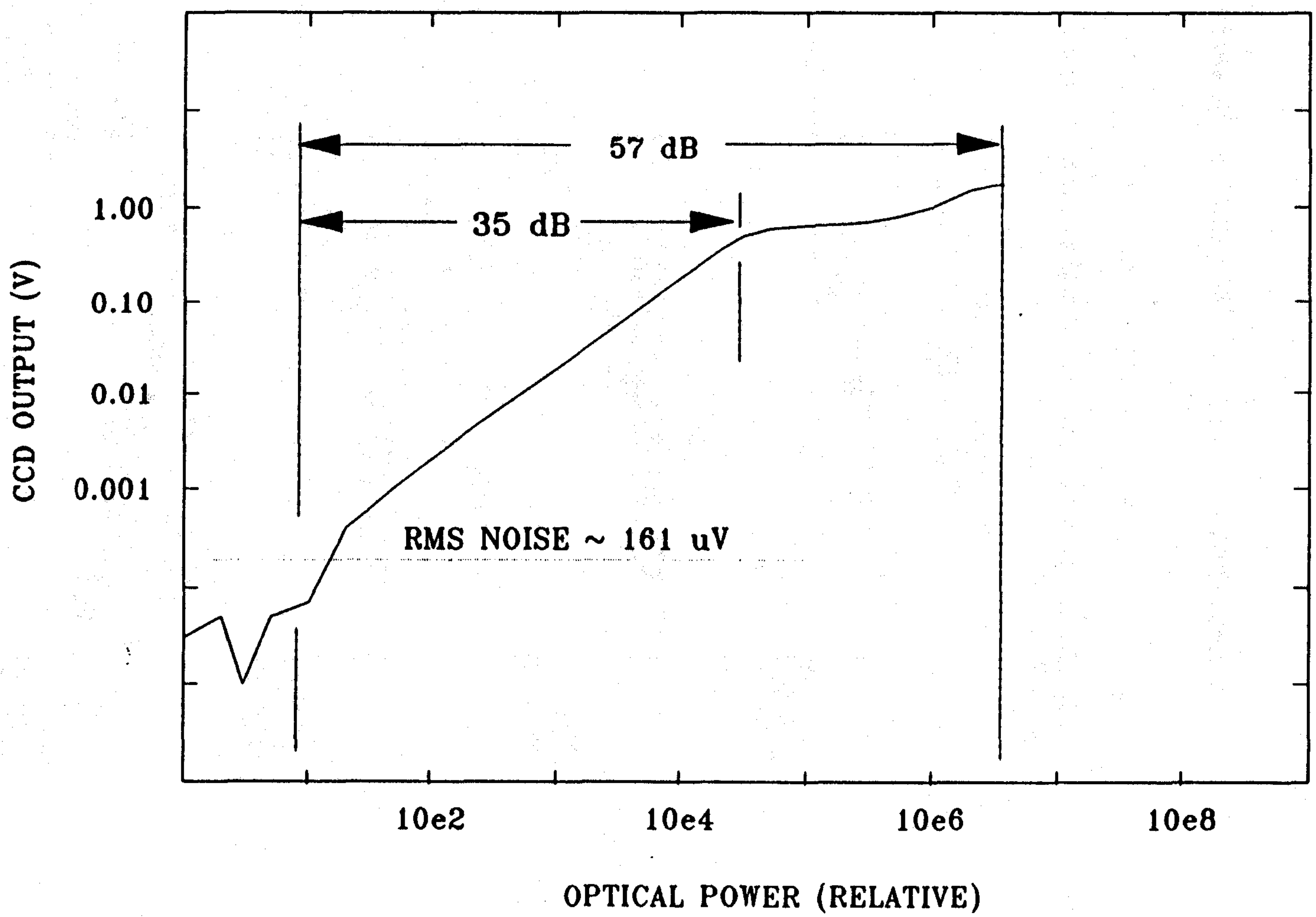
- FULL BURIED CHANNEL PHOTOGATE STRUCTURE FOR HIGH SPEED COMPLETE CHARGE TRANSFER.
- HIGH UNIFORMITY OVER PHOTODIODE TYPE DEVICE.
- LINEAR ENERGY DETECTOR DOWN TO NEE.

DISADVANTAGES:

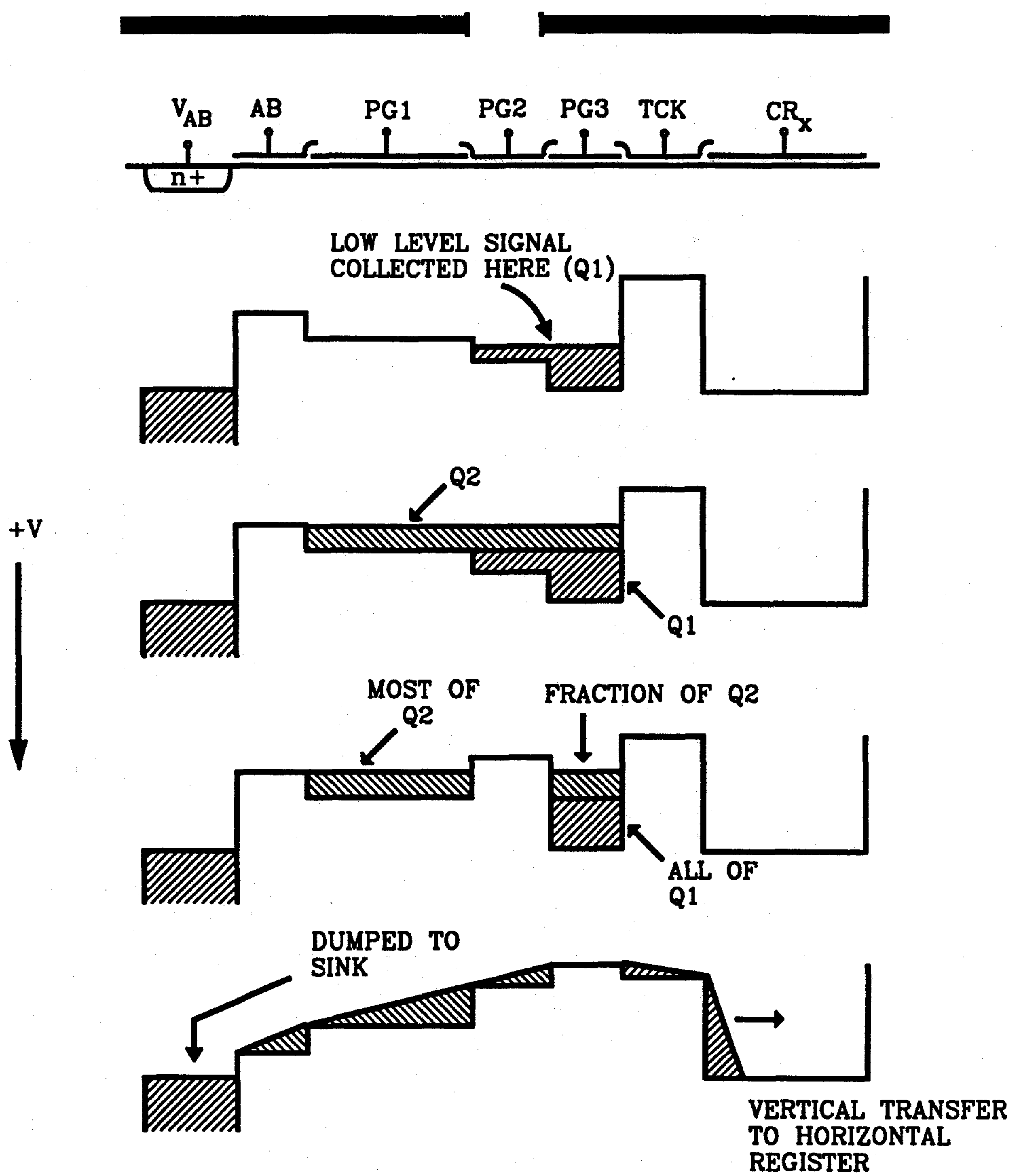
- PRACTICAL SIZE OF PHOTOGATE LIMITS DYNAMIC RANGE TO 55 dB.

LORAL-FAIRCHILD CCD 660

OPTICAL TRANSFER FUNCTION



CHARGE PARTITION DETECTOR



FLOATING GATE DETECTOR

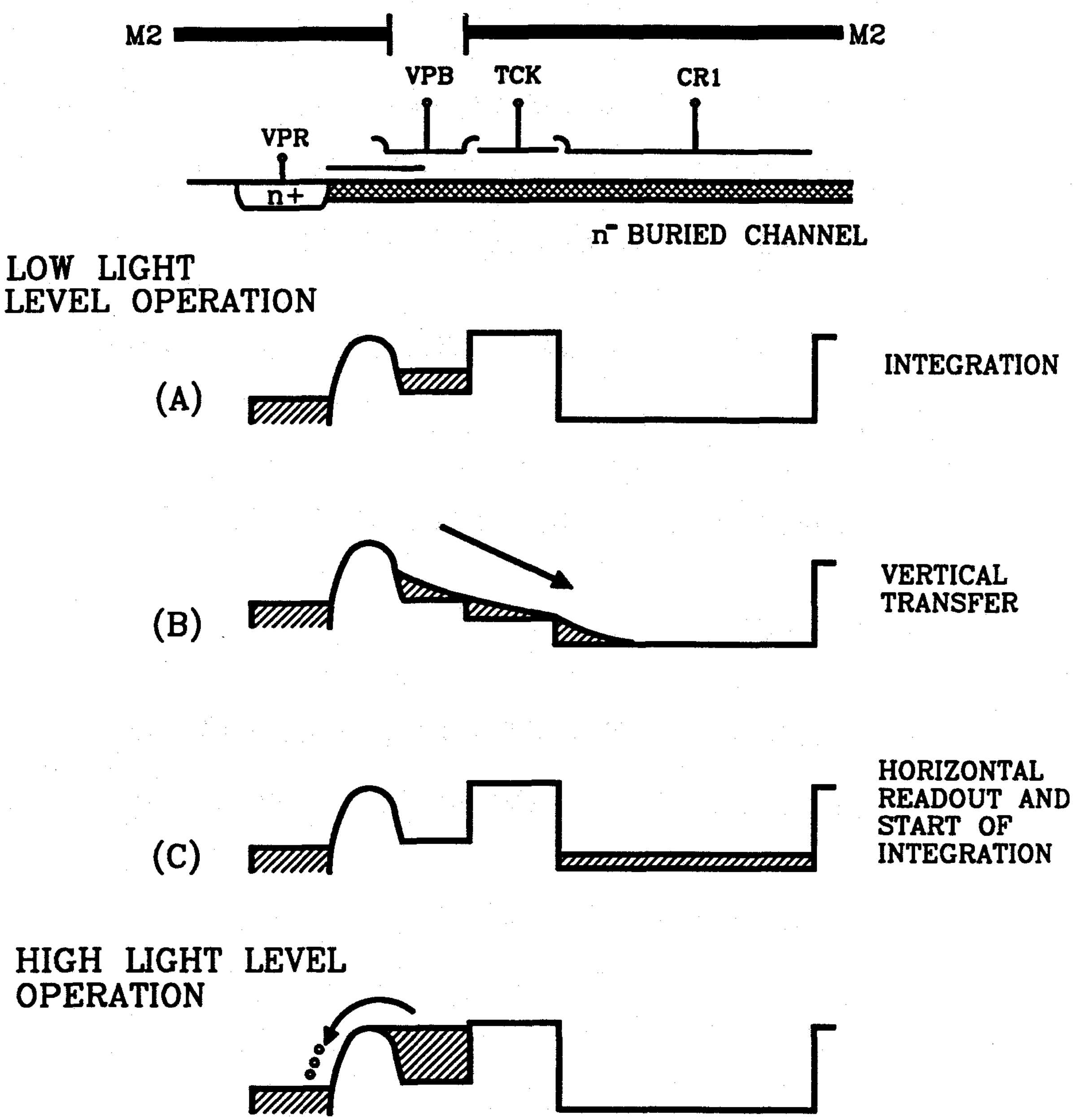
ADVANTAGES:

- FULL BURIED CHANNEL PHOTOGATE STRUCTURE: NO IMAGE LAG, EXCELLENT LOW LIGHT LEVEL PERFORMANCE AND HIGH SPEED.
- LOGARITHMIC COMPRESSION AT HIGH LIGHT LEVELS.
- LINEAR ENERGY DETECTOR DOWN TO NEE.

DISADVANTAGES:

- POSSIBLE UNIFORMITY ISSUES AT HIGH LIGHT LEVELS DUE TO THRESHOLD VOLTAGE VARIATION.

FLOATING GATE DETECTOR



SUBTHRESHOLD CONDUCTION OVER FLOATING GATE PROVIDES ATTENUATION AT HIGH LIGHT LEVELS.

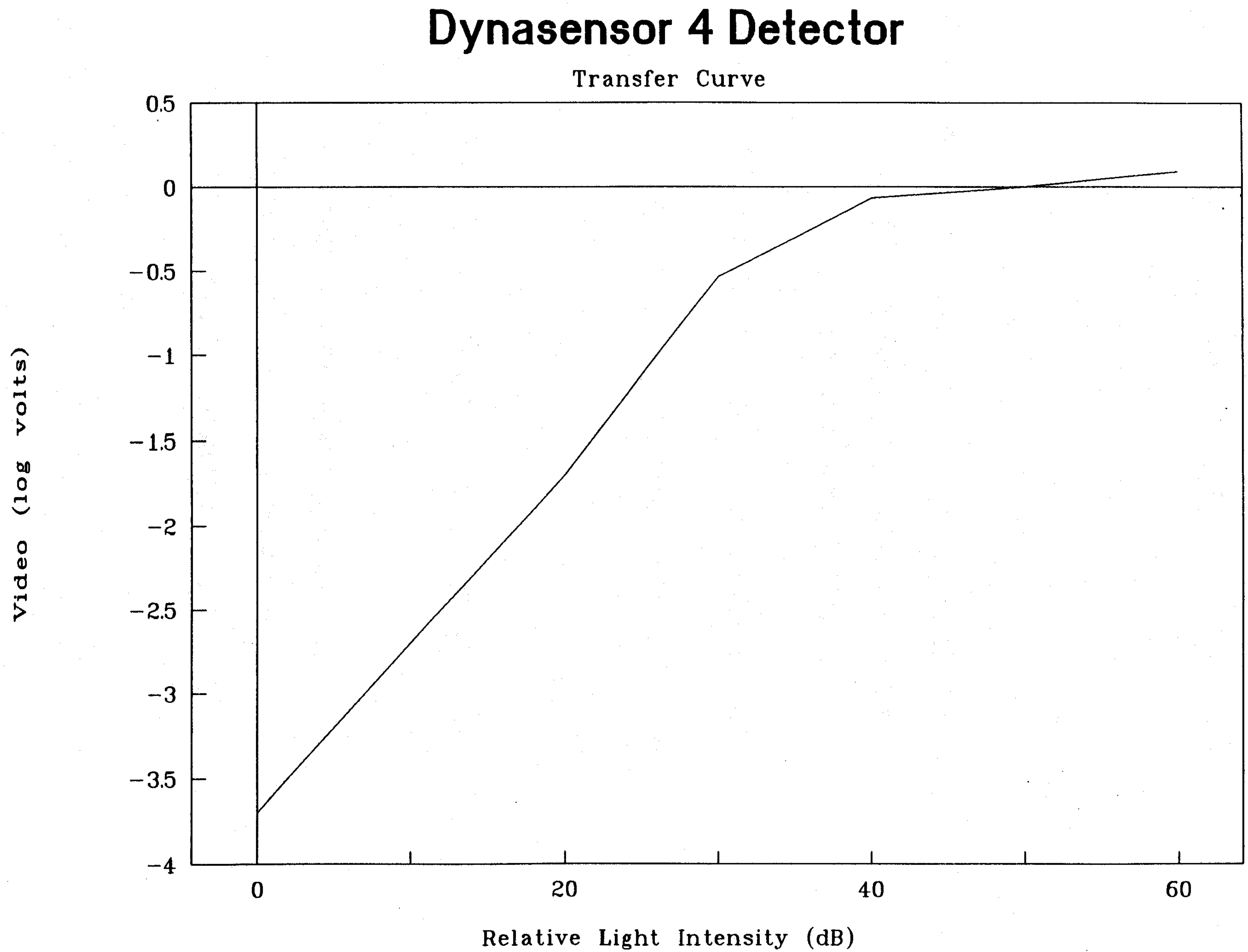
DYNASENSOR 4 DETECTOR

ADVANTAGES:

- PHOTOGATE CHARGE COLLECTION REGION FOR COMPLETE CHARGE TRANSFER AT LOW AND INTERMEDIATE LIGHT LEVELS.
- LOGARITHMIC COMPRESSION AT HIGH LIGHT LEVELS.
- TEMPORAL RESPONSE OF DYNA3 ELIMINATED.

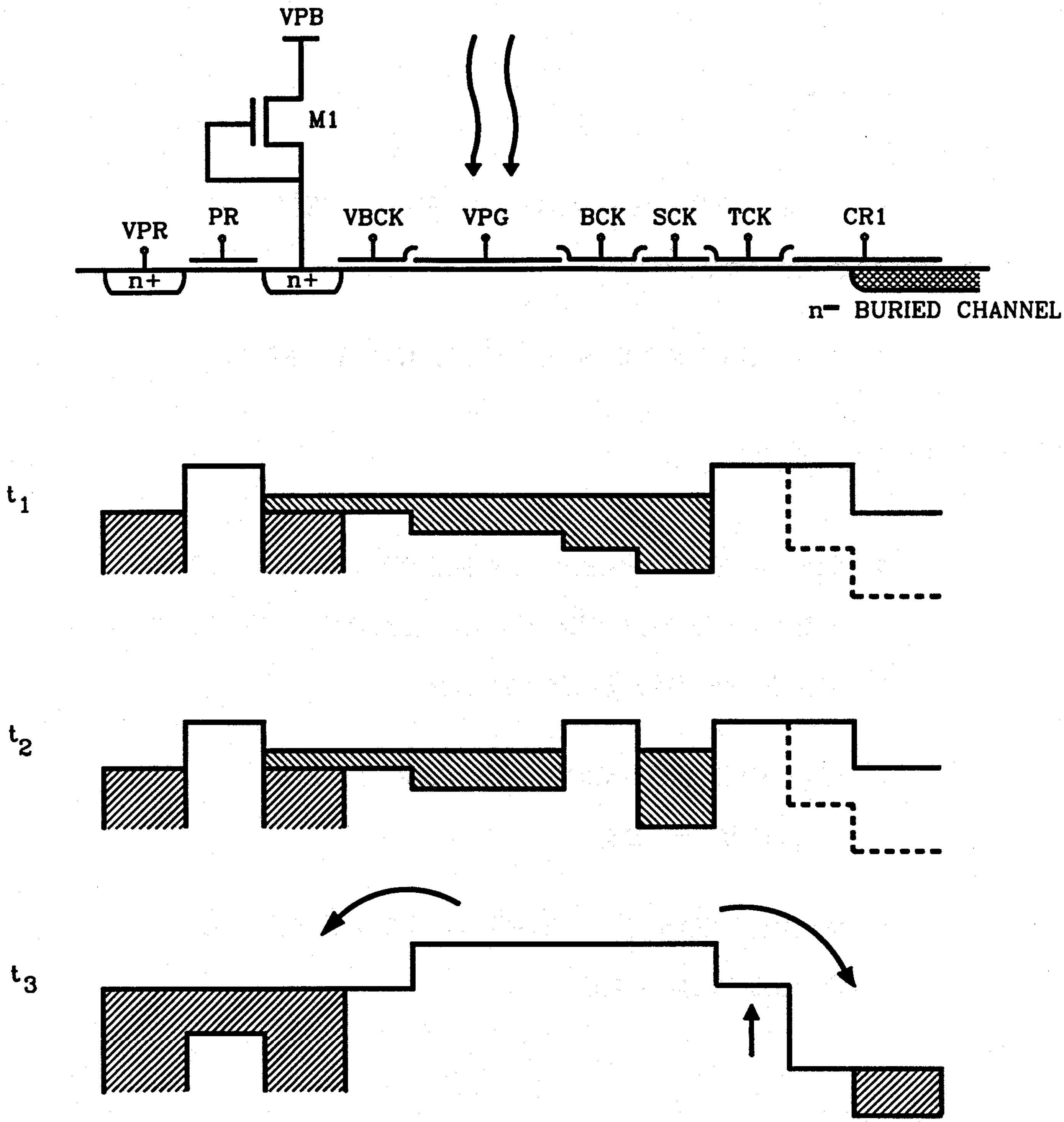
DISADVANTAGES:

- REQUIRED FAT ZERO HAS ASSOCIATED INJECTION NOISE.
- SURFACE CHANNEL STRUCTURE PERMITS SIGNAL CHARGE TRAPPING AT THE SURFACE AND REDUCES FRINGE FIELDS BETWEEN ADJACENT ELECTRODES.



Dynasensor 4 Detector
Transfer Curve
0.5
0
−0.5
−1
−1.5
−2
−2.5
−3
−3.5
−4
Video (log volts)
0
20
40
60
Relative Light Intensity (dB)

DYNA4 PHOTODETECTOR STRUCTURE



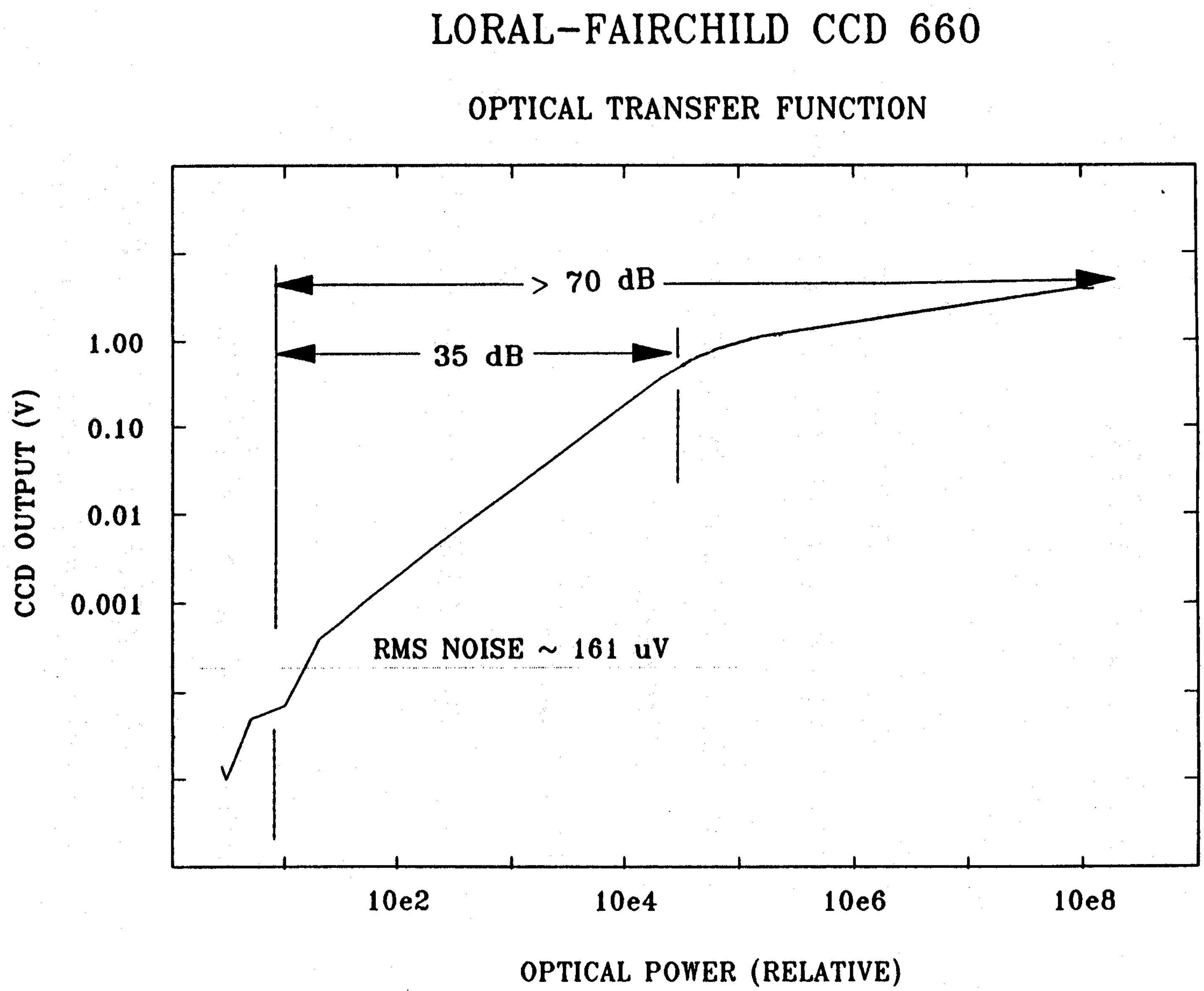
DYNASENSOR 3 DETECTOR

ADVANTAGES:

- EXCELLENT PHOTOSITE TO SHIFT REGISTER CROSSTALK.
- LOG COMPRESSION AT HIGH LIGHT LEVELS.

DISADVANTAGES:

- INCOMPLETE CHARGE TRANSFER AT LOW LIGHT LEVELS CAUSES TEMPORAL RESPONSE EFFECTS AND POOR QUANTUM EFFICIENCY.
- REQUIRED FAT ZERO HAS ASSOCIATED INJECTION NOISE.
- DYNAMIC RANGE LIMITED TO 50 dB AT 1 μs INTEGRATION TIME.



LORAL-FAIRCHILD CCD 660
OPTICAL TRANSFER FUNCTION
> 70 dB
35 dB
RMS NOISE ~ 161 uV
1.00
0.10
0.01
0.001
CCD OUTPUT (V)
10e2
10e4
10e6
10e8
OPTICAL POWER (RELATIVE)

CHARGE DIFFUSION DETECTOR

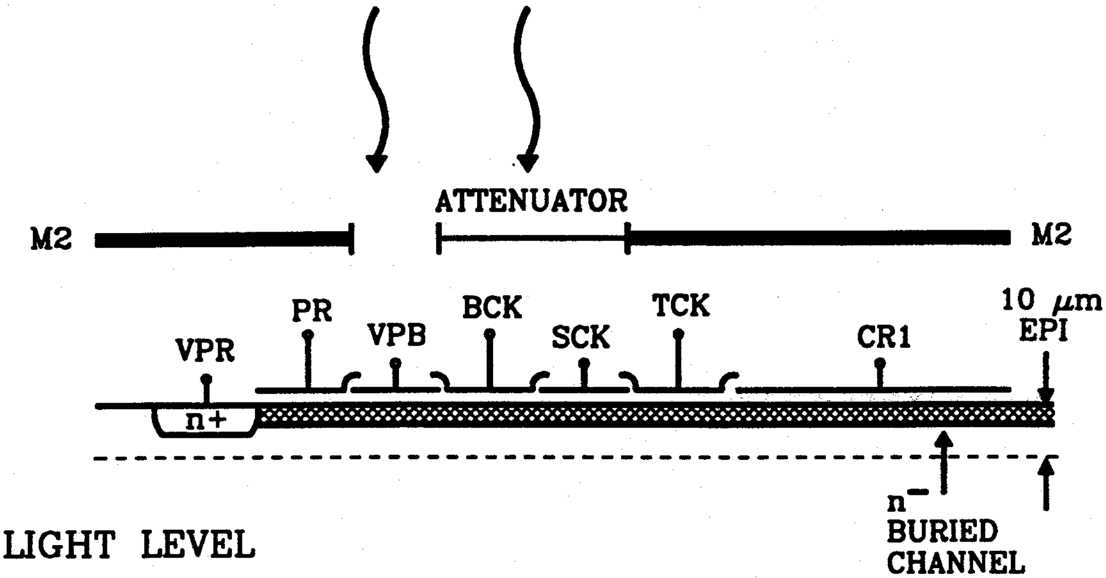
ADVANTAGES:

- FULL BURIED CHANNEL PHOTOGATE STRUCTURE FOR HIGH SPEED COMPLETE CHARGE TRANSFER.
- GREATER THAN 80 dB DYNAMIC RANGE HAS BEEN REPORTED.
- HIGH UNIFORMITY.
- LINEAR ENERGY DETECTOR DOWN TO NEE.

DISADVANTAGES:

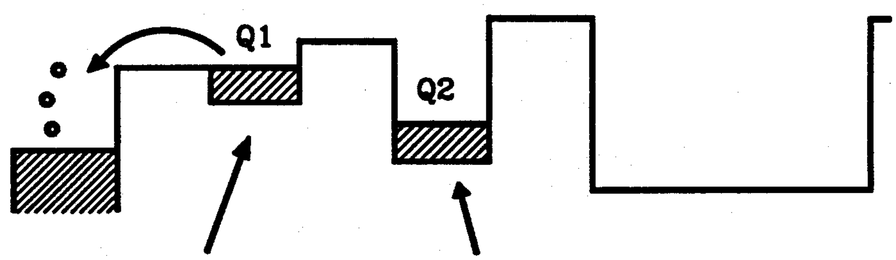
- DYNAMIC RANGE IS WAVELENGTH DEPENDENT.
- PIPELINE DELAY NECESSARY TO ELIMINATE PHOTOSITE TO SHIFT REGISTER CROSSTALK.
- METHODS TO IMPROVE OPTICAL CROSSTALK ISOLATION REDUCE THE EFFECTIVENESS OF THIS ARCHITECTURE.

MULTI–RESPONSE DETECTOR



HIGH LIGHT LEVEL OPERATION:

INTEGRATION



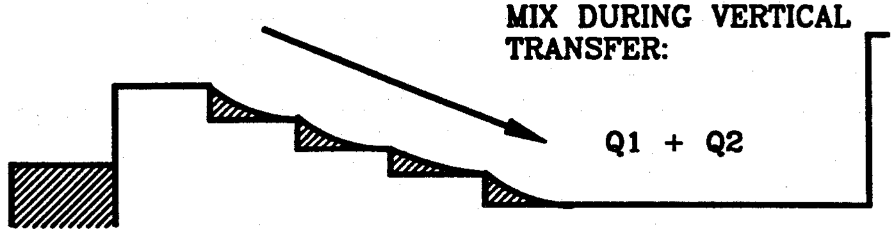
PRIMARY WELL SATURATES

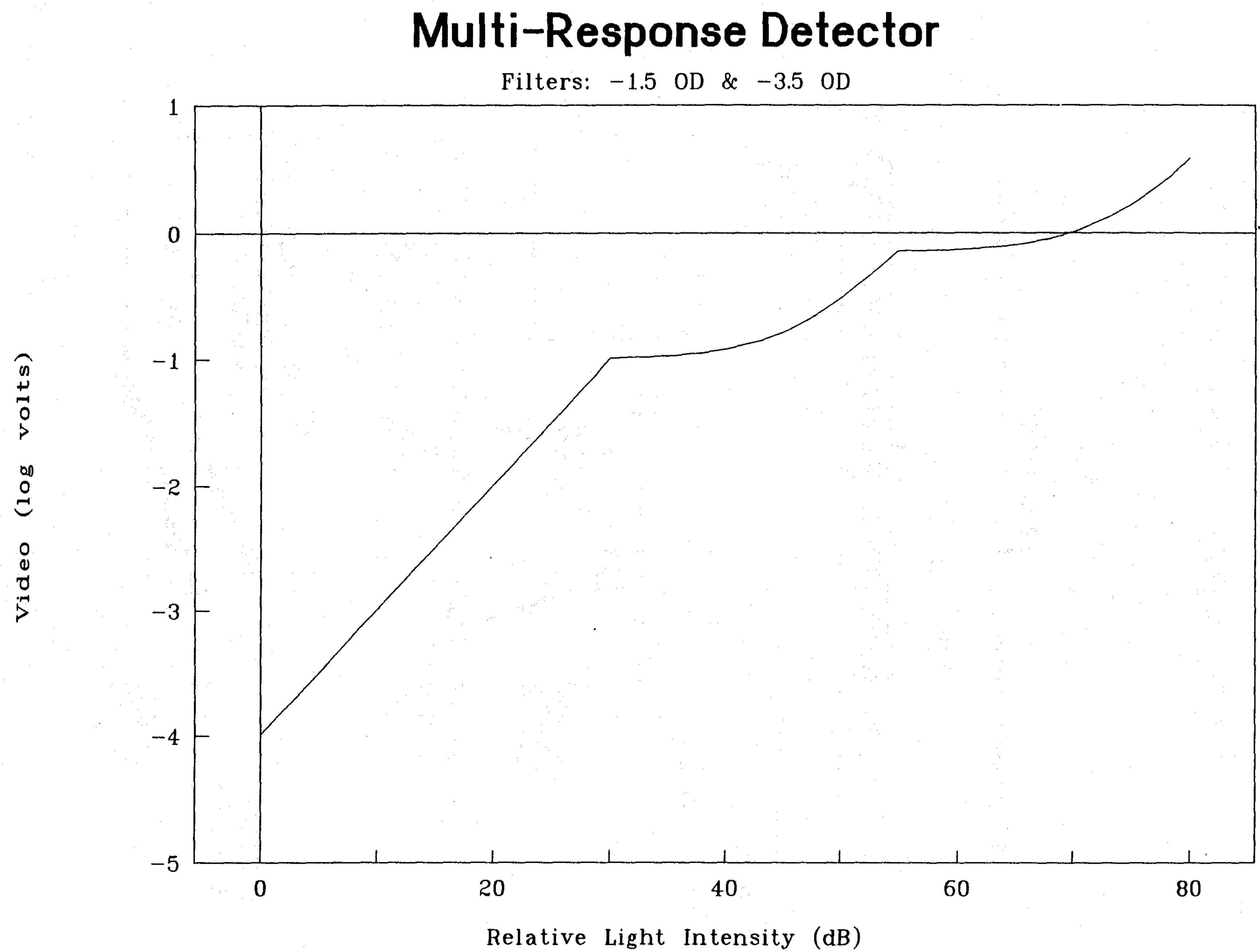
SECONDARY WELL COLLECTS AT

$$QE_2 = \frac{1}{100} QE_1$$

VERTICAL TRANSFER

THE TWO COMPONENTS MIX DURING VERTICAL TRANSFER:




Multi-Response Detector
Filters: −1.5 OD & −3.5 OD
Video (log volts)
1
0
−1
−2
−3
−4
−5
0
20
40
60
80
Relative Light Intensity (dB)

MULTI-RESPONSE DETECTOR

ADVANTAGES:

- DYNAMIC RANGE OF 80 dB IS EXPECTED.
- FULL BURIED CHANNEL PHOTOGATE STRUCTURE FOR COMPLETE CHARGE TRANSFER.
- HIGH UNIFORMITY.
- WIDE DYNAMIC RANGE AT ALL VISIBLE WAVELENGTHS.
- LINEAR ENERGY DETECTOR DOWN TO NEE.
- METHODS FOR CROSSTALK REDUCTION DO NOT AFFECT DYNAMIC RANGE.

DISADVANTAGES:

- REQUIRES LARGER APERTURE HEIGHT.

"SECONDARY" PERFORMANCE ISSUES AND POSSIBLE DESIGN IMPROVEMENTS

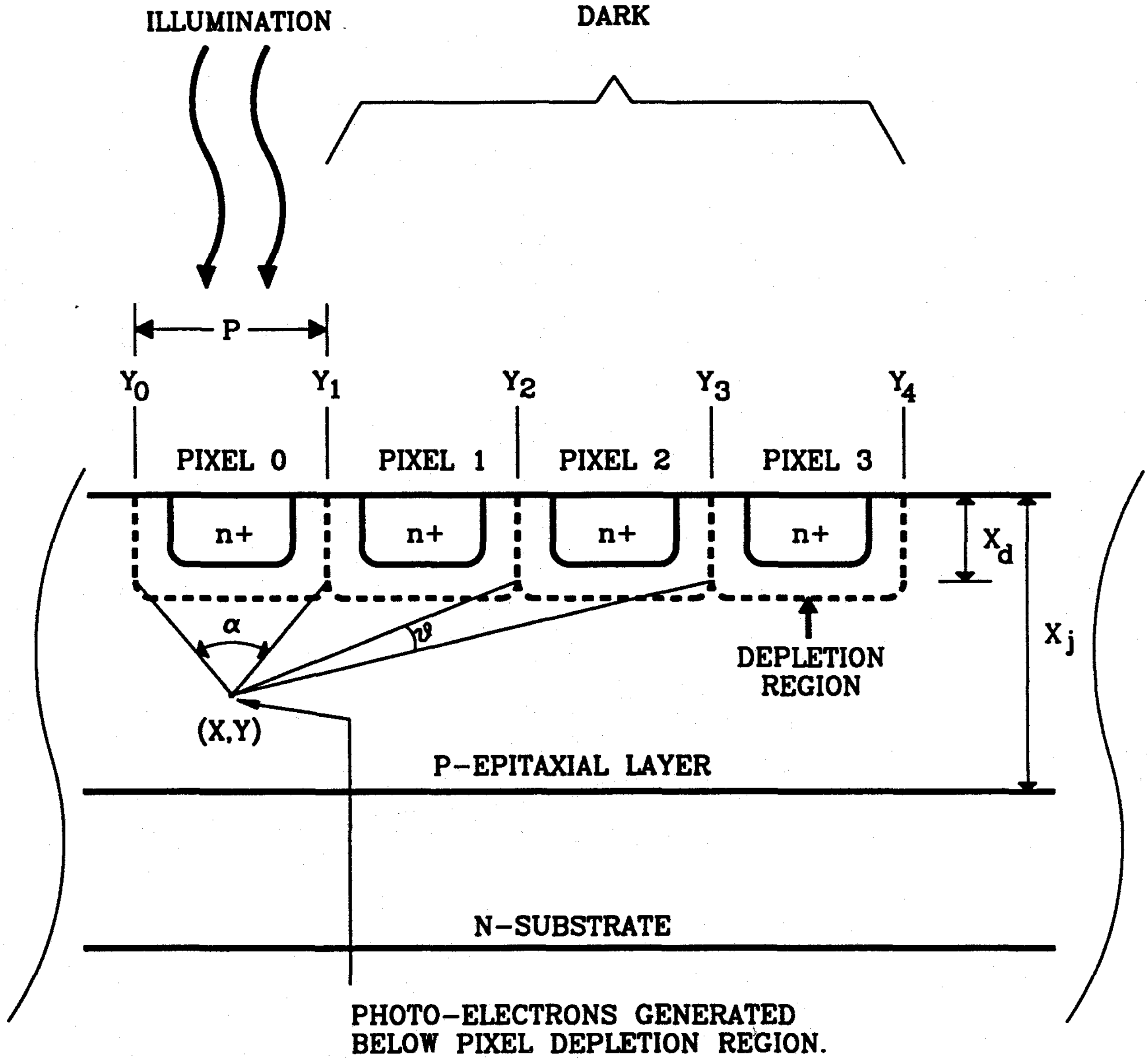
INITIAL DEVELOPMENT EFFORTS FOR DETECTOR ARRAYS HAVE FOCUSED ON INCREASING THE OPTICAL DYNAMIC RANGE.

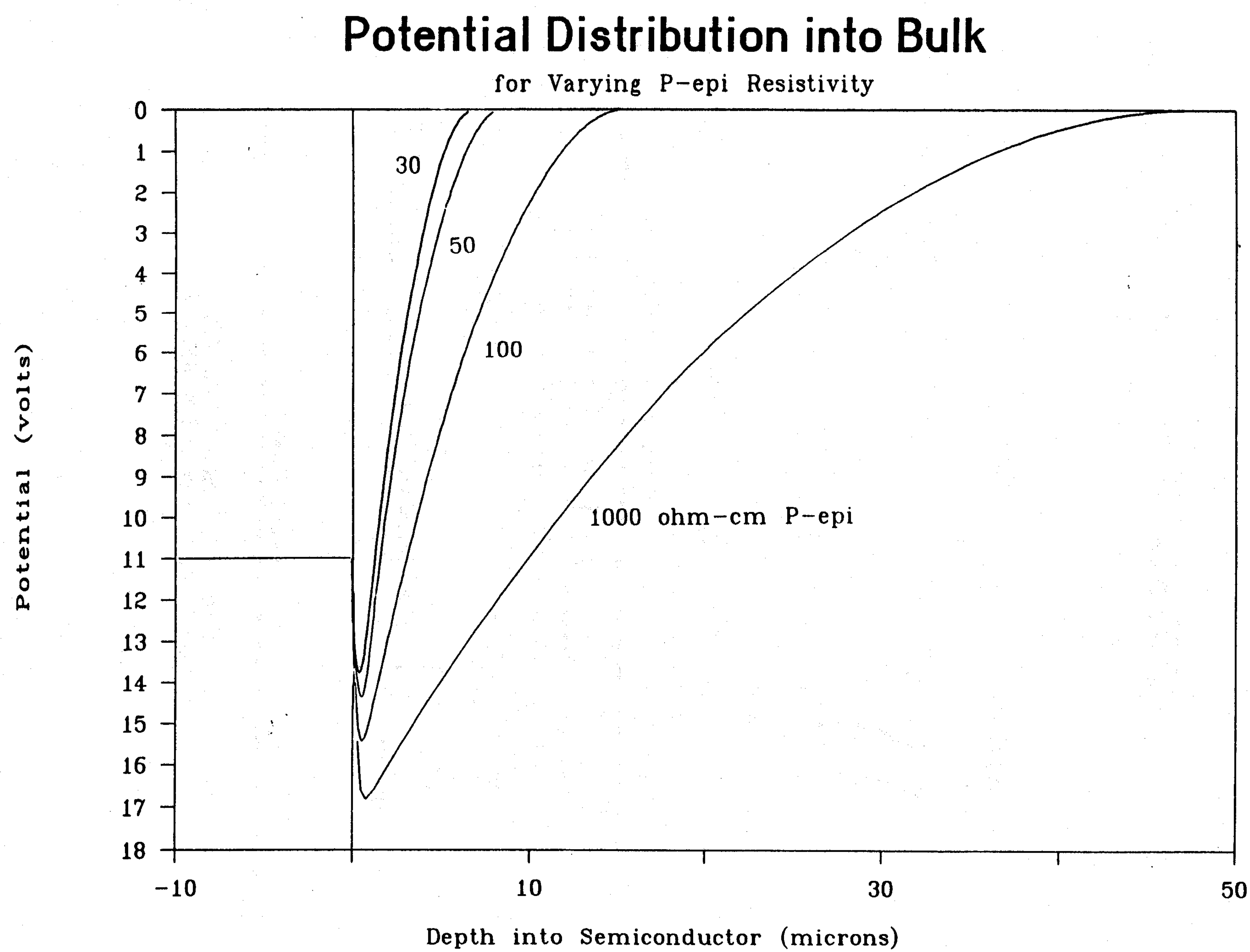
WITH STATE-OF-THE-ART ARRAYS REPORTING > 70 dB ODR, SECONDARY PERFORMANCE ISSUES NOW REQUIRE ATTENTION. THESE INCLUDE CROSSTALK, OUTPUT SPEED, AND SENSITIVITY.

MANY RECENT DEVELOPMENTS HAVE OCCURRED IN CCD'S DESIGNED FOR OTHER APPLICATIONS (ESPECIALLY SCIENTIFIC AND HDTV) WHICH ARE APPROPRIATE FOR AO DETECTOR ARRAYS. THE FOLLOWING ISSUES ARE ADDRESSED IN THIS SECTION:

- OPTICAL AND ELECTRICAL CROSSTALK REDUCTION
- QUANTUM EFFICIENCY IMPROVEMENTS
- OUTPUT STRUCTURE/AMPLIFIER IMPROVEMENTS

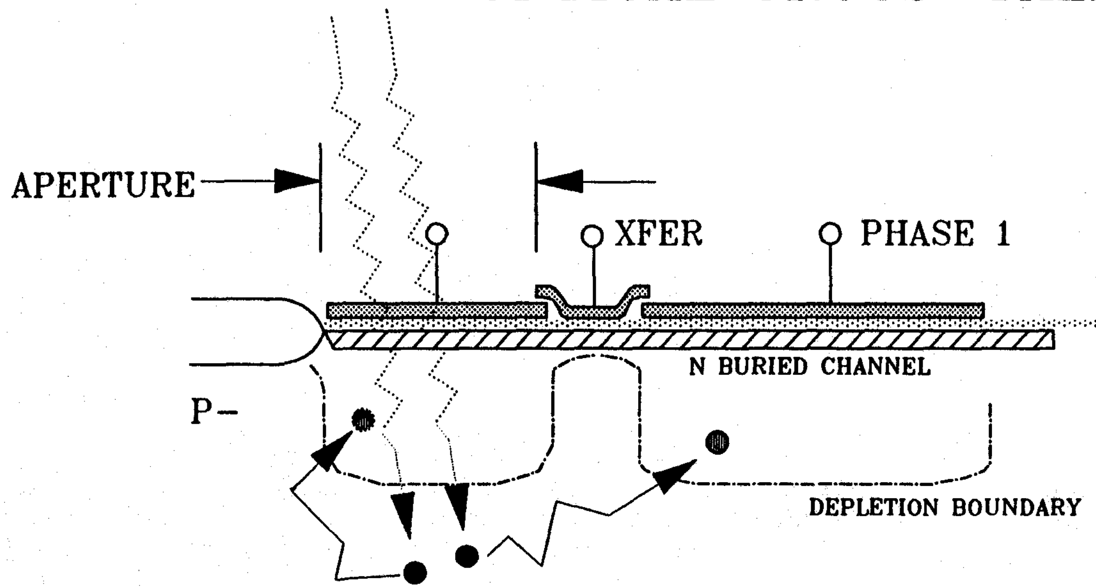
CROSSTALK MODEL





Potential Distribution into Bulk
for Varying P-epi Resistivity
Potential (volts)
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
30
50
100
1000 ohm-cm P-epi
-10
10
30
50
Depth into Semiconductor (microns)

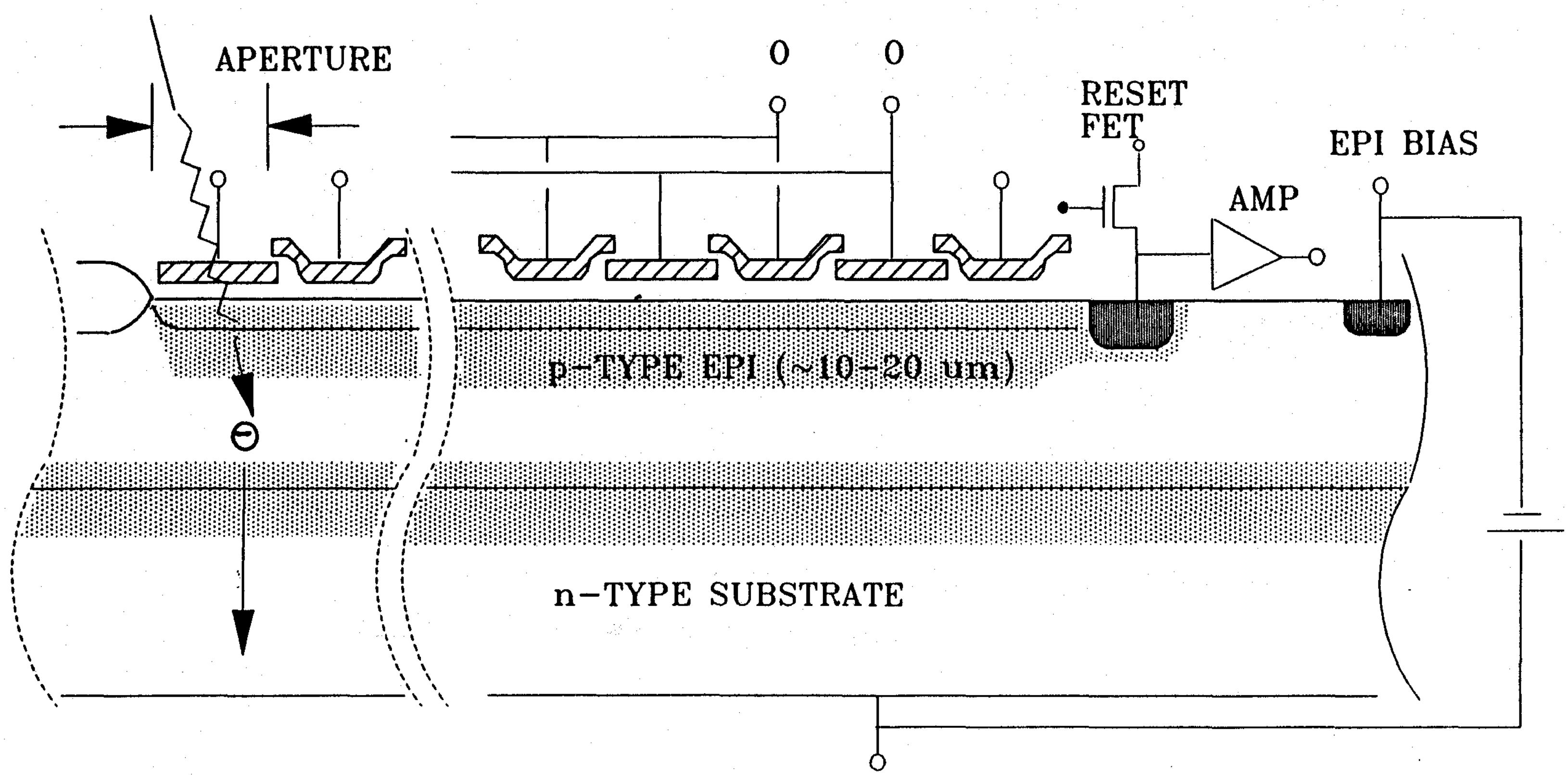
OPTICAL CROSS-TALK



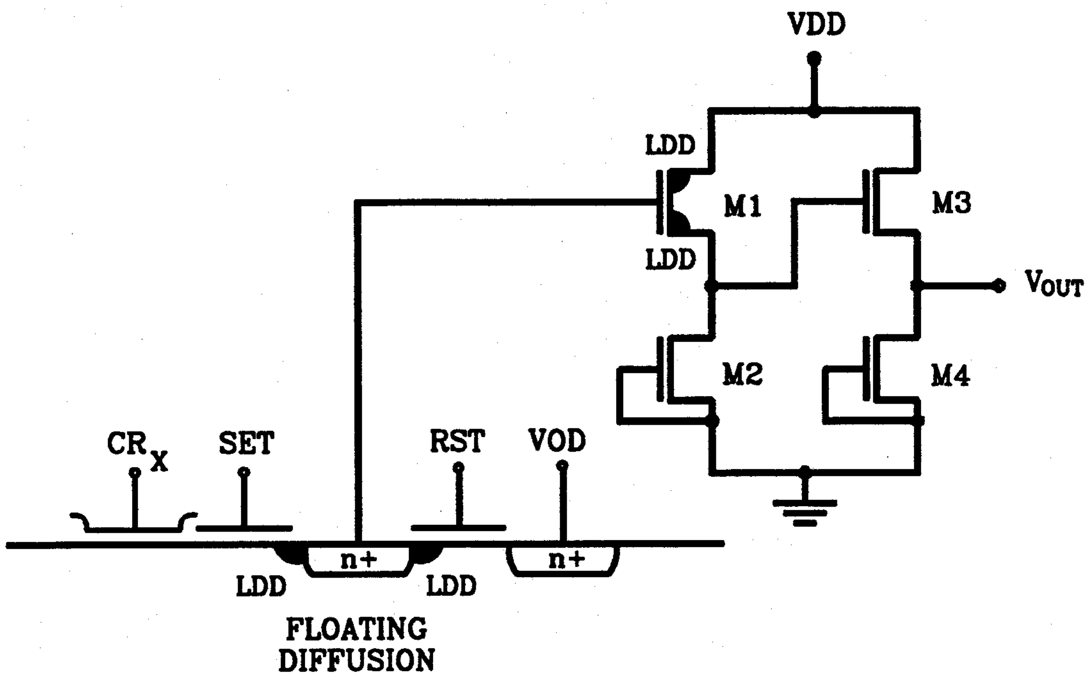
PERFORMANCE

DEVICE	PIXEL-PIXEL (2NN)	PIXEL-SHIFT REGISTER
DALSA IL-A3	−45 dB	< −65 dB
LF 660	< −43 dB	−40 dB

PHOTO-COUPLING TO SENSE NODE IN "p on n" SUBSTRATE STRUCTURES

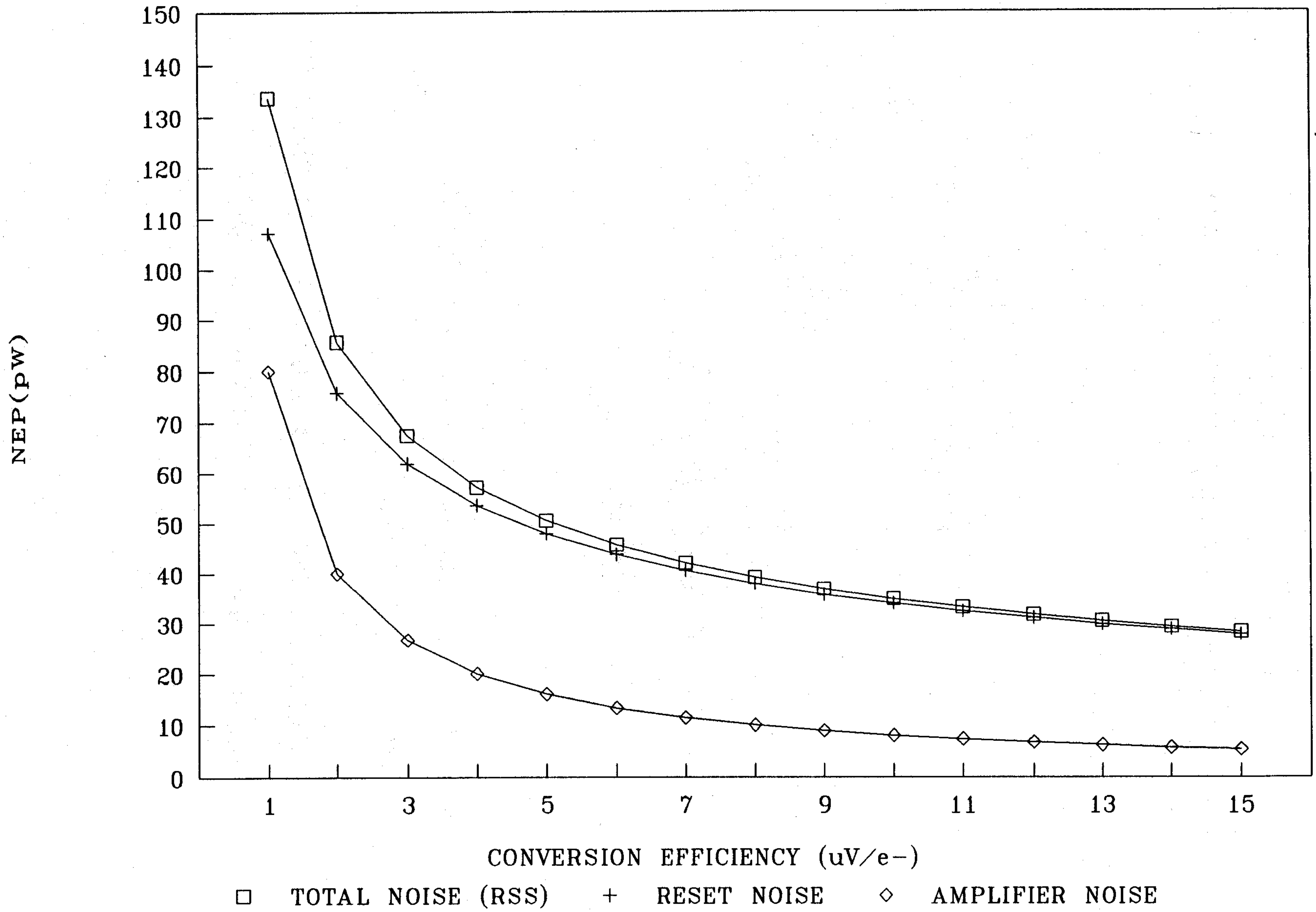


CONVERSION EFFICIENCY IMPROVEMENT



- DEVELOP A SELF-ALIGNED LDD PROCESS (OVERLAP COMPONENT).
- MINIMIZE M1 GATE AREA AND FLOATING DIFFUSION AREA AND MAINTAIN BANDWIDTH OF OUTPUT BUFFER.

1 usec NEP vs Conversion Efficiency



ON-FOCAL PLANE ARRAY SIGNAL PROCESSING

A TYPICAL 2 GHz, 100 CHANNEL RECEIVER MUST PROCESS SOME 100 MEGABYTES PER SECOND AND FIT INTO A VOLUME OF LESS THAN FIVE CUBIC INCHES.

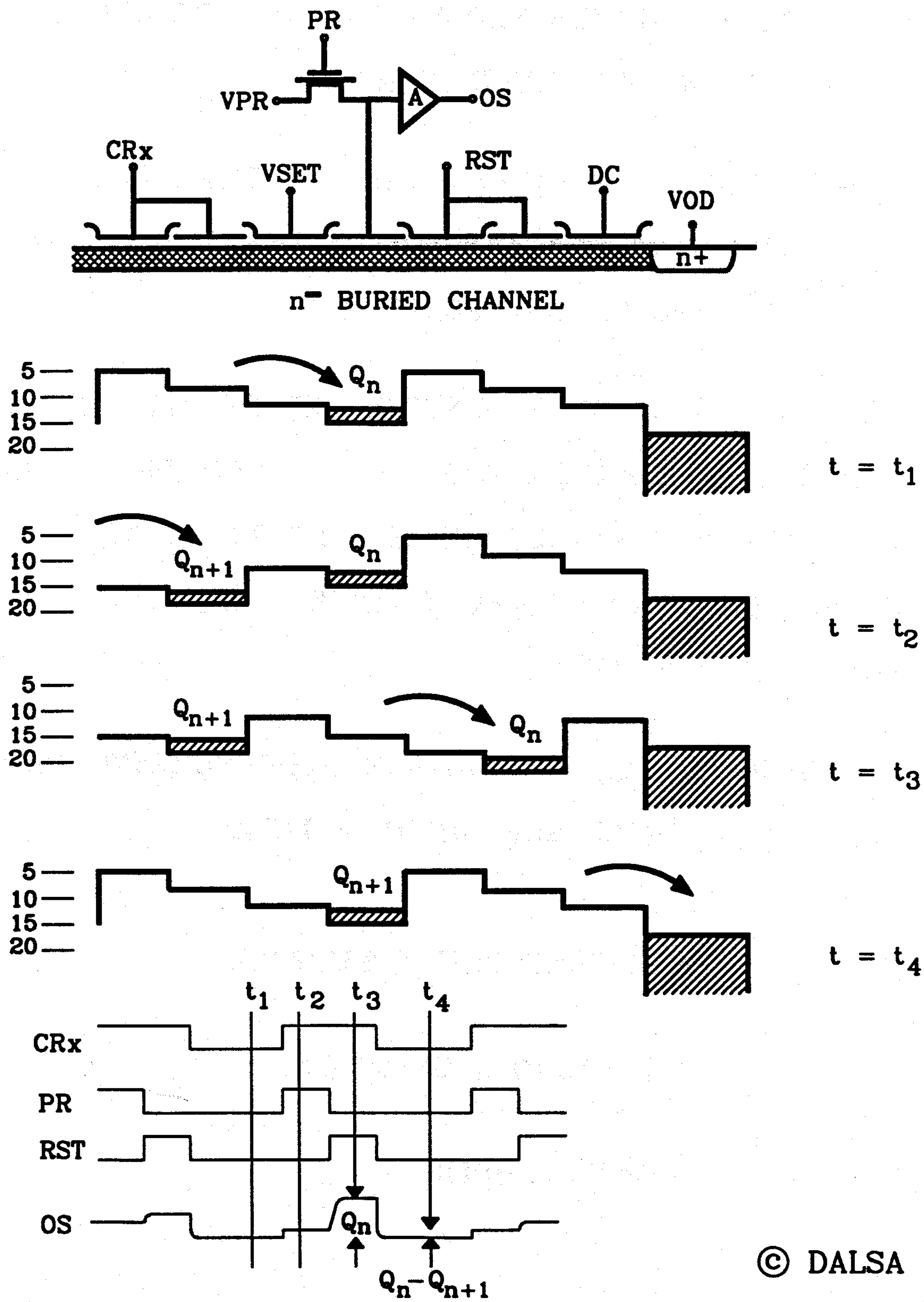
WITH FUTURE GENERATION SYSTEMS CALLING FOR EVEN MORE AGGRESSIVE REQUIREMENTS, SIGNAL PRE-PROCESSING ON-FPA BECOMES AN ATTRACTIVE FEATURE.

ONE SUCH PROCESSING FUNCTION, ESSENTIALLY A QUEUING SCHEME IS PRESENTED. THIS METHOD PROVIDES A CENTROID OPERATION ON THE TRANSFORMED RF SIGNAL TO A RESOLUTION OF ONE PIXEL (CHANNEL), AND AN ABSOLUTE THRESHOLD OPERATION.

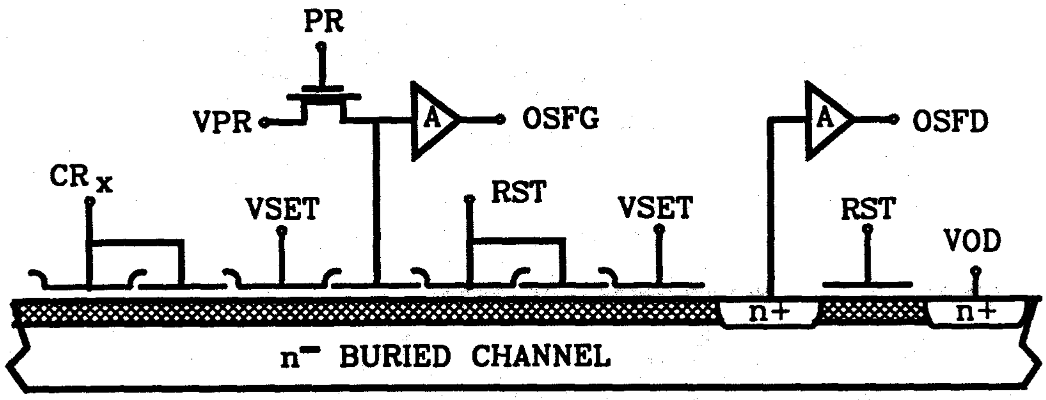
DISCUSSED IN THIS SECTION ARE BASIC BUILDING BLOCKS FOR SUCH A PROCESSOR WHICH INCLUDE:

- DIFFERENCING STRUCTURE
- THRESHOLD OPERATION
- SENSE AMPLIFIER

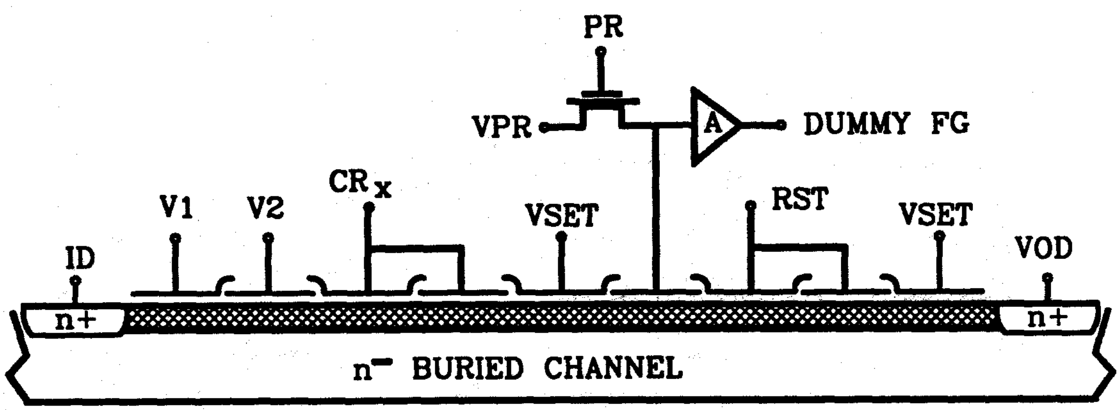
DIFFERENCING OUTPUT STRUCTURE



CENTROID IMPLEMENTATION

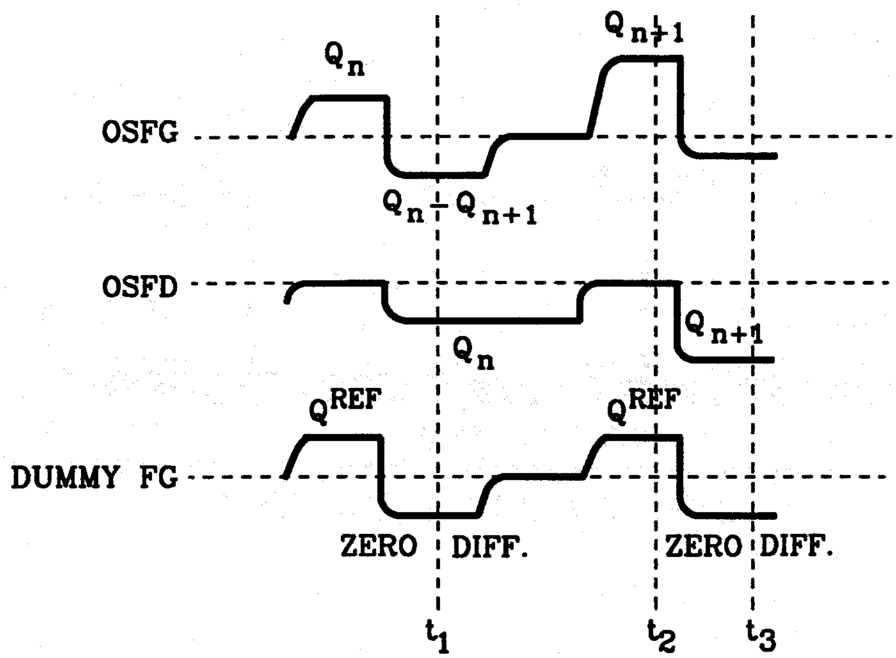


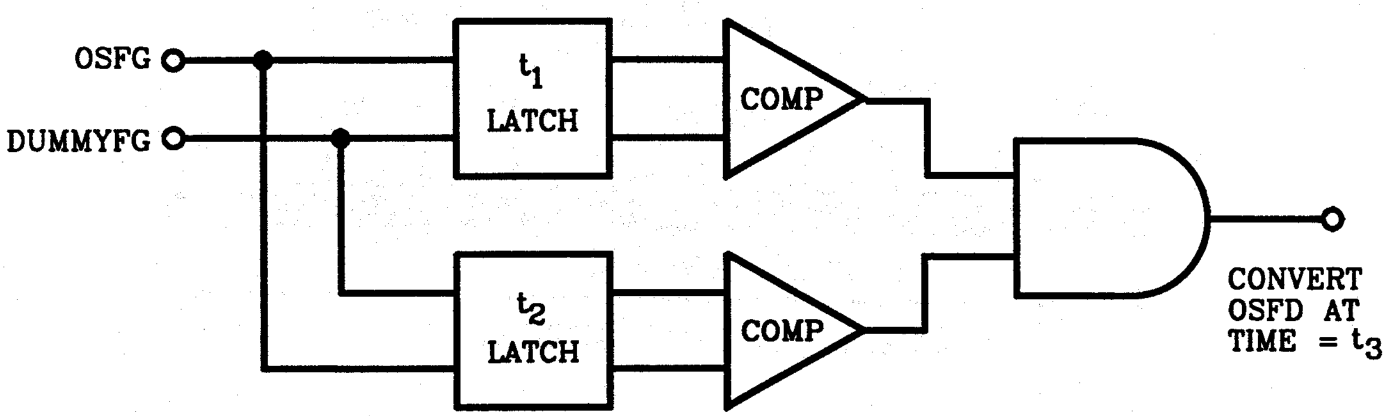
SIGNAL OUTPUT STRUCTURE



DUMMY OUTPUT STRUCTURE

CENTROID IMPLEMENTATION





SUMMARY

PROGRESS TO DATE:

- IMAGE LAG FREE DYNAMIC RANGE > 80 dB HAS BEEN DEMONSTRATED.
- 150 pW NEP (1 μsec) HAS BEEN ACHIEVED. IMPROVEMENT NEEDED TO 10 pW.
- 2NN OPTICAL CROSSTALK OF −40 dB HAS BEEN DEMONSTRATED ON 30−50 $\Omega \bullet$cm P−EPI. FABRICATION ON 1000 $\Omega \bullet$cm SHOULD DECREASE CROSSTALK TO −60 dB.
- METHODS FOR ON−FPA SIGNAL PROCESSING ARE FEASIBLE.

BOTTOM LINE:

- CCD TECHNOLOGY IS CAPABLE OF MEETING THE DEMANDING REQUIREMENTS OF AO RECEIVERS.