

**APPLICATION OF CCD TECHNOLOGY  
TO  
HIGH SPEED SAMPLED ANALOG SIGNAL PROCESSING**

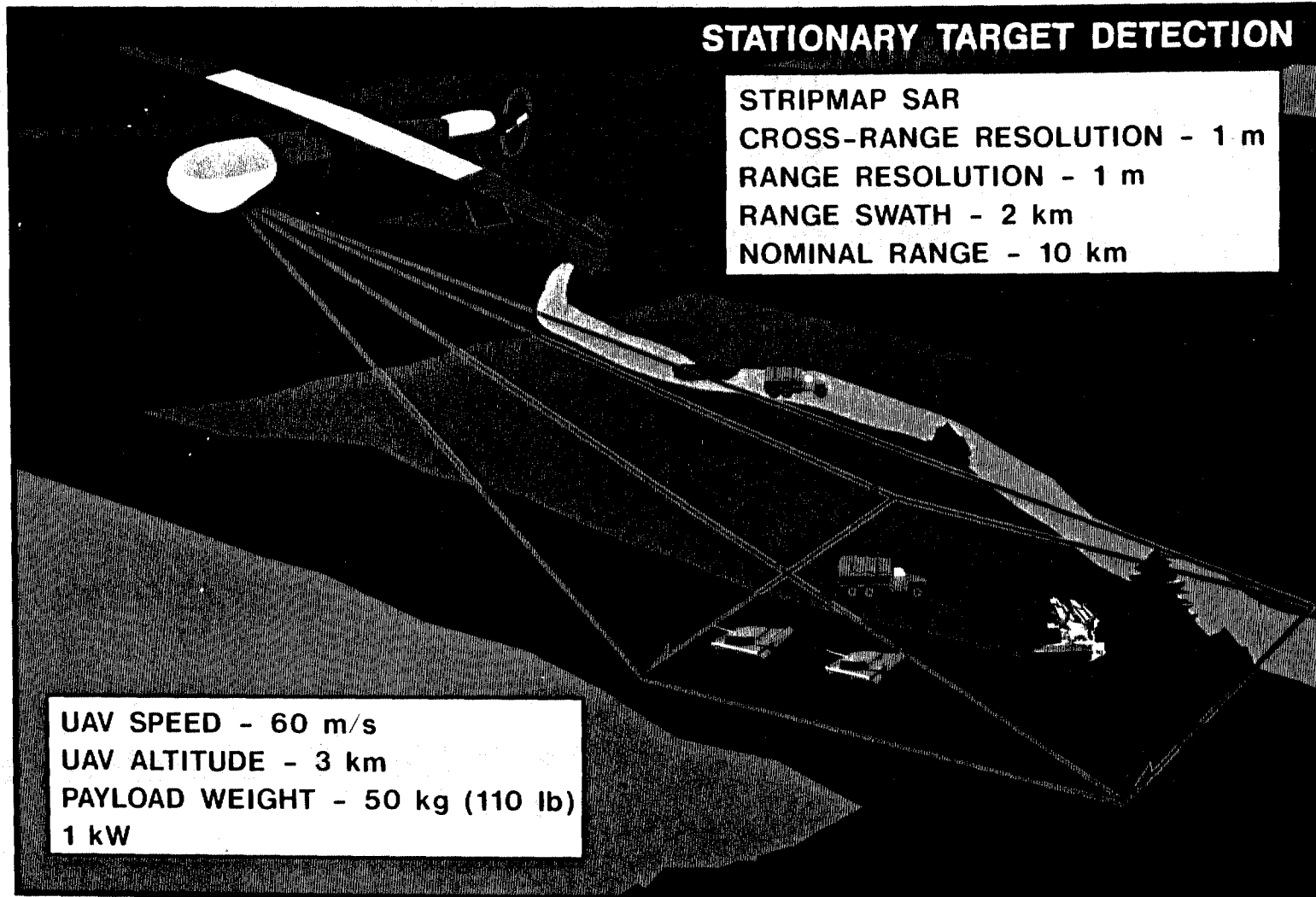
**J. Strombosky, R. Whiting, C. Christensen,  
D. McClure, R. Wixted**  
Lincoln Laboratory, M.I.T.  
Lexington, MA

**OUTLINE**

- **APPLICATIONS AND EXAMPLES**
- **SYSTEM REQUIREMENTS**
- **CRITICAL DESIGN ISSUES**
- **EXPERIMENTAL RESULTS**
- **TECHNOLOGY DEVELOPMENT**



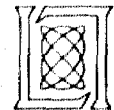
# UAV SYNTHETIC APERTURE RADAR MODE



## STATIONARY TARGET DETECTION

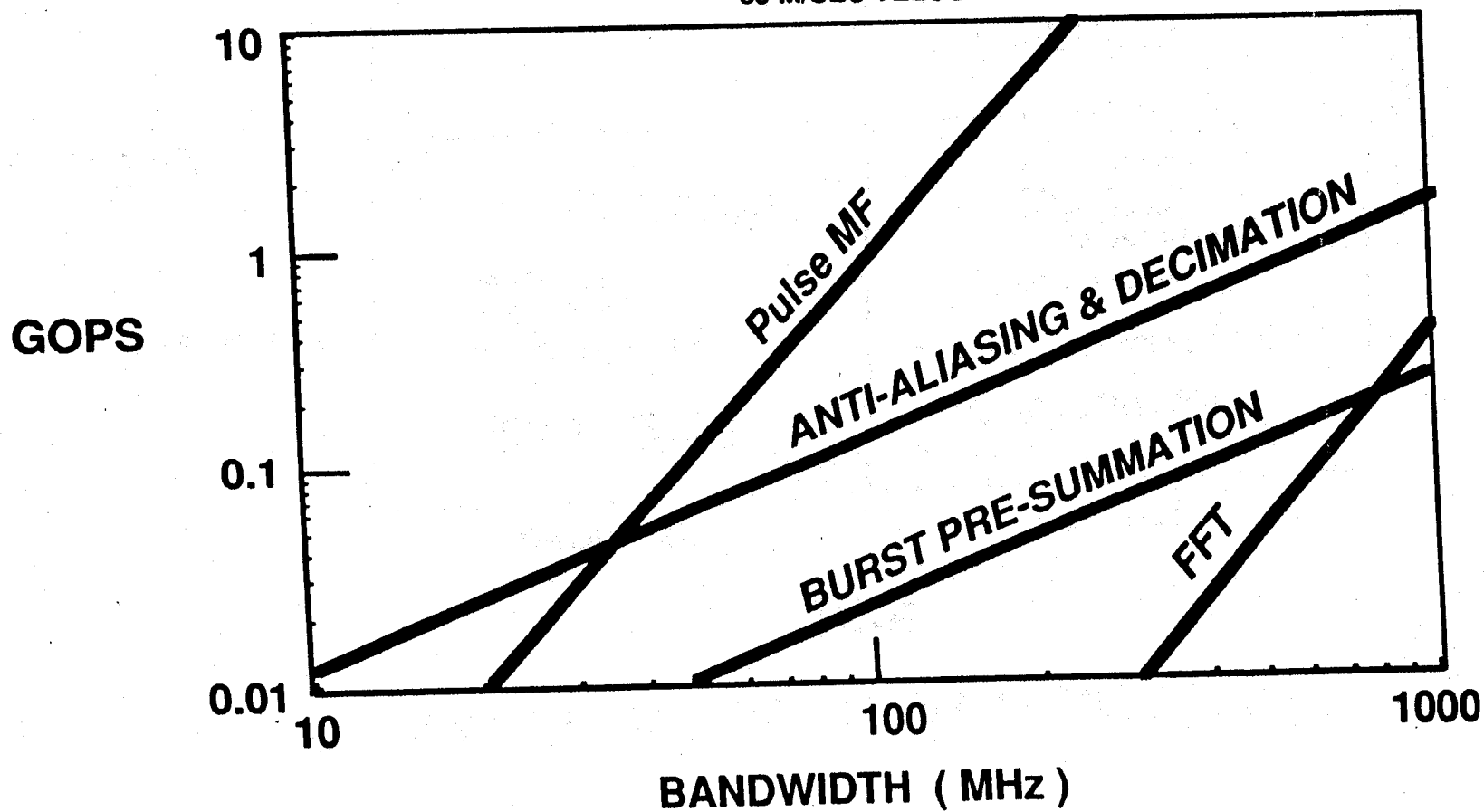
STRIPMAP SAR  
CROSS-RANGE RESOLUTION - 1 m  
RANGE RESOLUTION - 1 m  
RANGE SWATH - 2 km  
NOMINAL RANGE - 10 km

UAV SPEED - 60 m/s  
UAV ALTITUDE - 3 km  
PAYLOAD WEIGHT - 50 kg (110 lb)  
1 kW

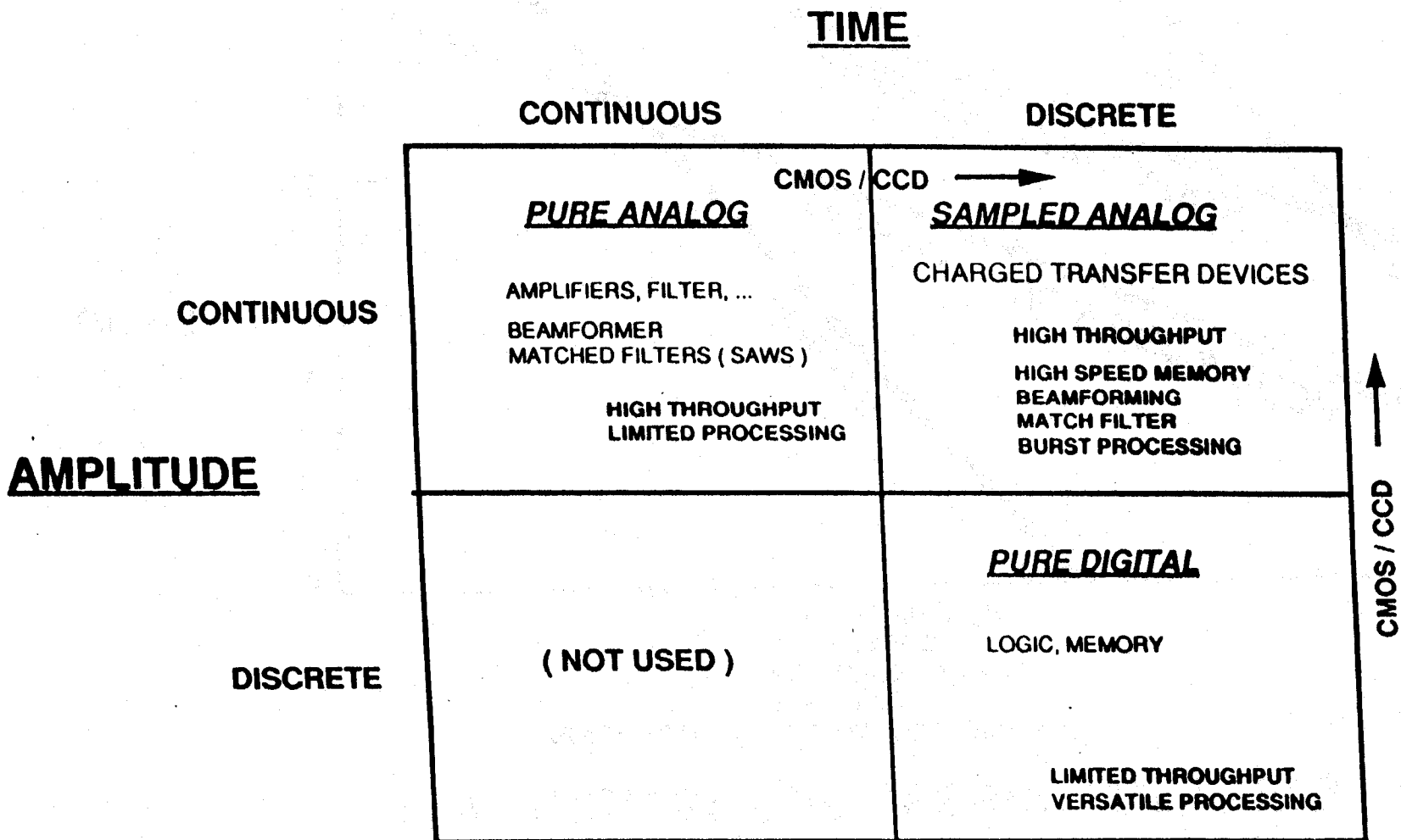


# UAV - DIGITAL PROCESSING OPTIONS

Assumptions: 10  $\mu$  sec PULSEWIDTH  
PRF = 4000  
2 K RANGE SWATH  
3K ALTITUDE  
60 M/SEC VELOCITY



# SIGNAL PROCESSING ALTERNATIVES



# CCD SIGNAL PROCESSING CHARACTERISTICS

## STRENGTHS:

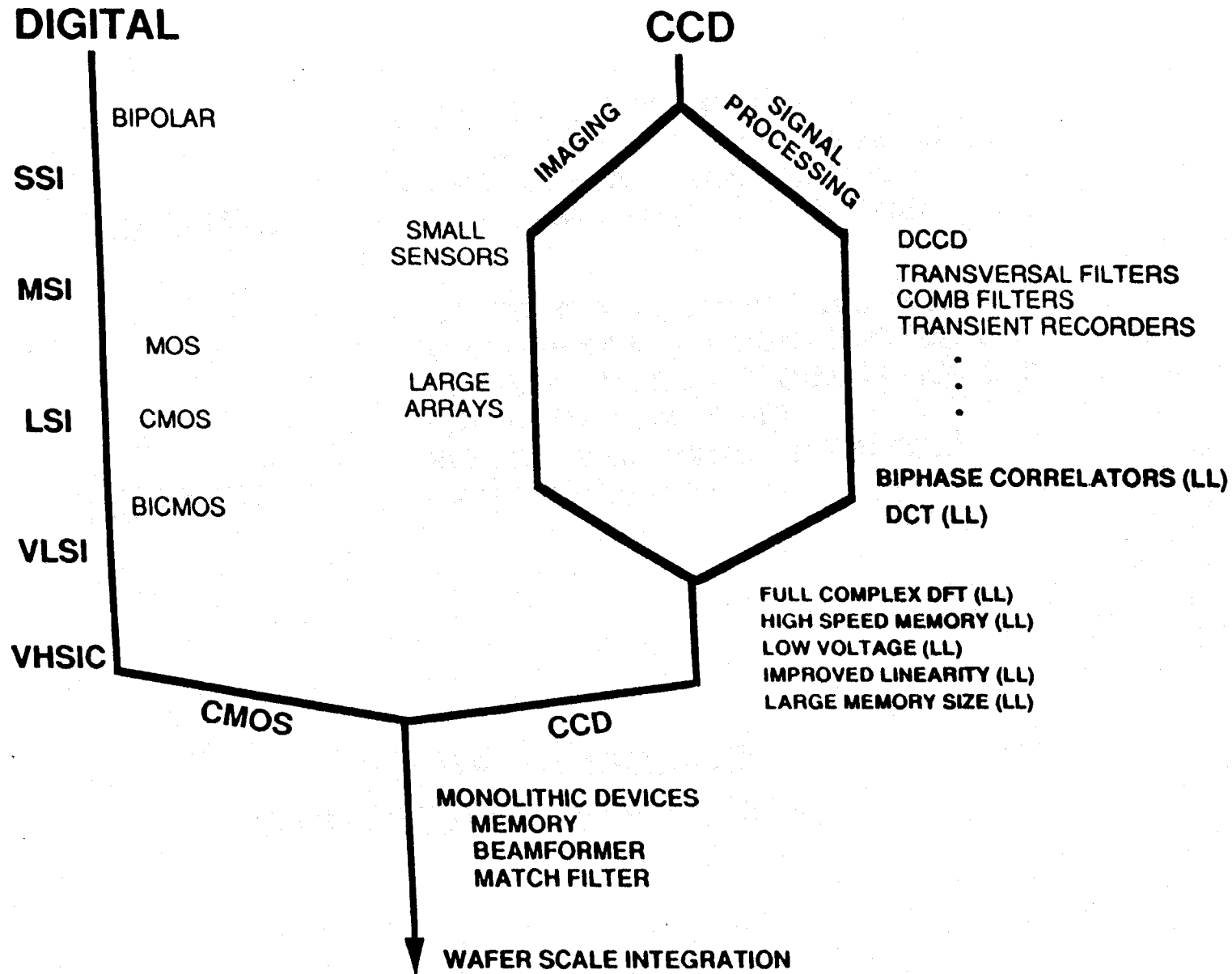
- HIGH THROUGHPUT
- HIGH DENSITY ( SAMPLED ANALOG)
- LOW POWER AND WEIGHT
- INTEGRATED TECHNOLOGY ( CMOS/CCD)
- CONVENTIONAL SILICON PROCESSES
- COMMERCIALY DRIVEN TECHNOLOGY

## LIMITATIONS:

- LOW DYNAMIC RANGE AND LINEARITY
- SHORT SIGNAL STORAGE TIMES
- LIMITED MATHEMATICAL VERSATILITY
- MASK PROGRAMMABLE

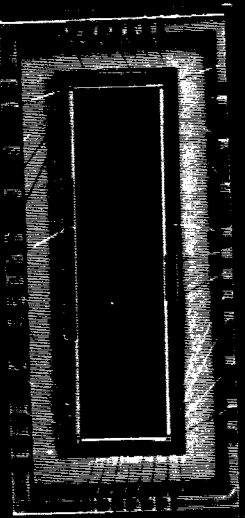
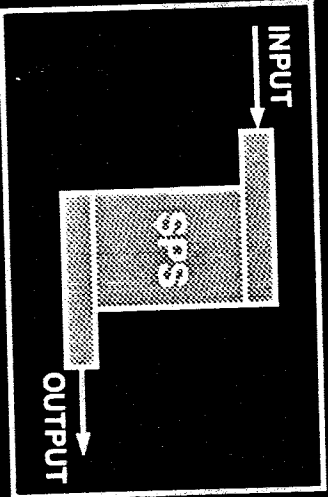


# TECHNOLOGY EVOLUTION

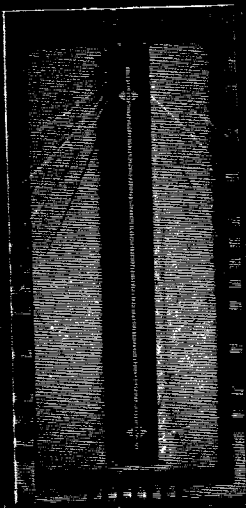
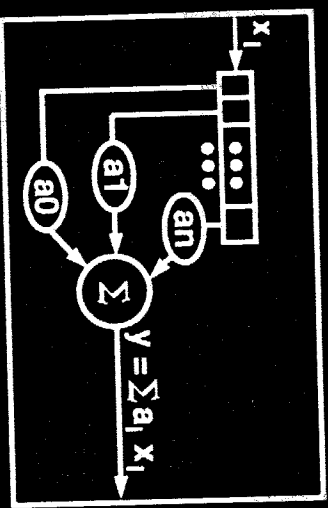


# CCD SIGNAL PROCESSING TECHNOLOGY

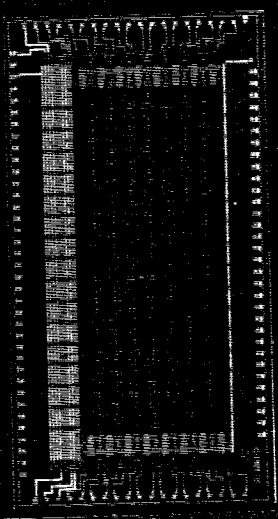
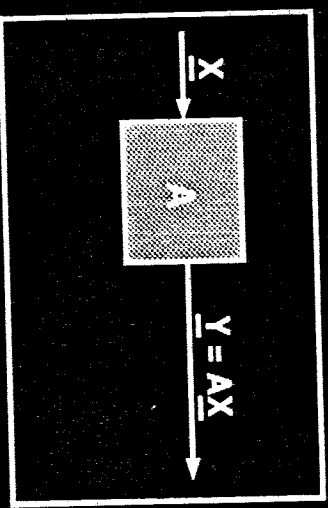
## HIGH SPEED MEMORY



## MATCHED FILTER



## DFT/BEAMFORMER



## SERIAL PARALLEL SERIAL SHIFT REGISTER

- 150-200 MHz INPUT
- 64-K SAMPLE STORAGE
- > 55 dB DYNAMIC RANGE
- LINEARITY > 8 BITS (Full Diff)
- > 1-SECOND DWELL

## TRANSVERSAL FILTER

- BI-PHASE CORRELATOR
- CHIP LENGTH 512/1024
- 10-20 MHz/10-20 BOPS
- LINEARITY > 7 BITS
- CMOS CIRCUIT INTEGRATION

## VECTOR MATRIX PRODUCT

- FULL DIFFERENTIAL DFT
- 10-20 MHz/10-20 BOPS
- > 50-dB DYNAMIC RANGE
- LINEARITY > 8 BITS (Full Diff)
- CMOS CIRCUIT INTEGRATION



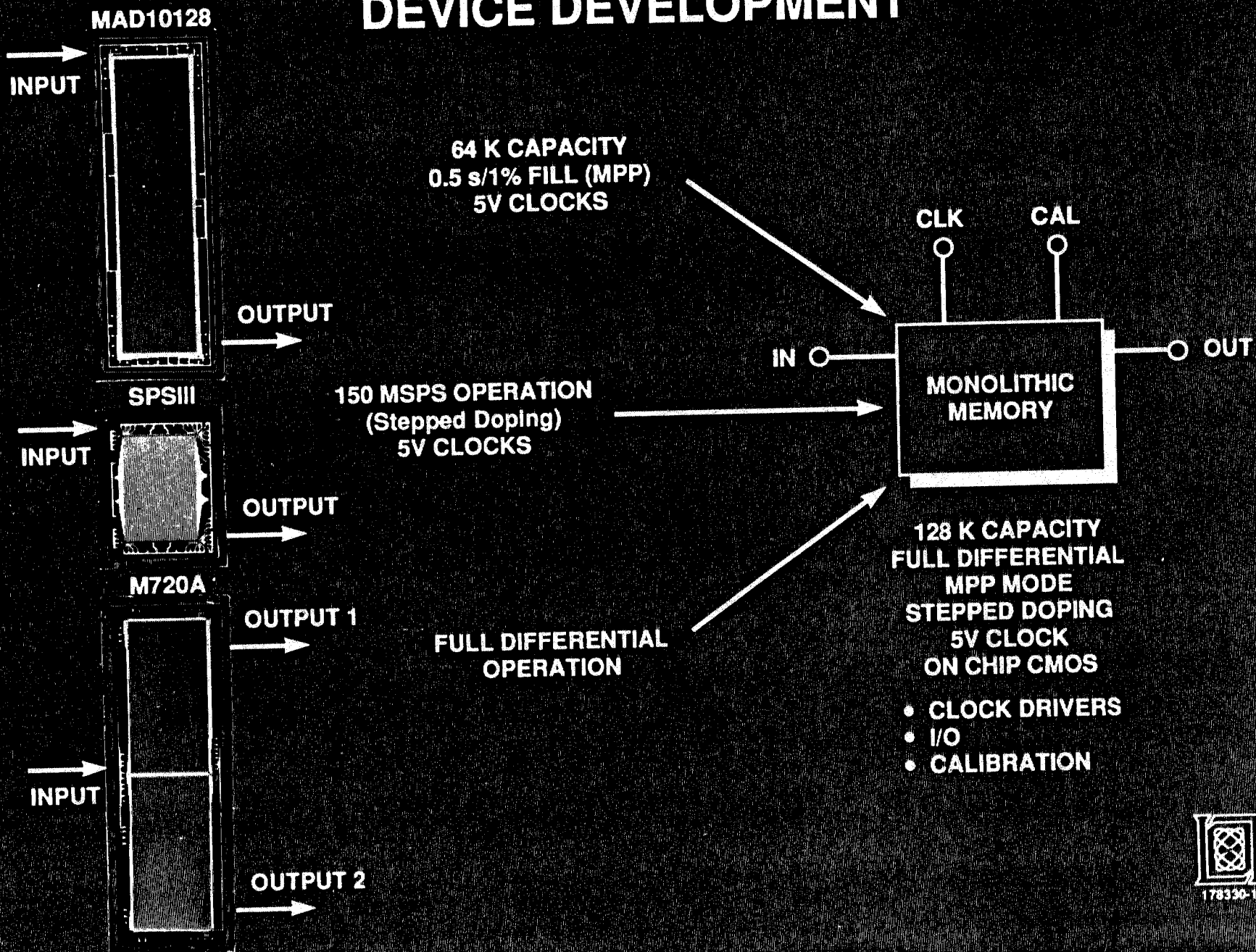
178986-3

## **SPS MEMORY REQUIREMENTS**

- **LARGE STORAGE SIZE (>128K)**
- **150-200MSPS INPUT RATE**
- **10MSPS OUTPUT RATE**
- **>100mS DWELL-TIME (<1% FILL)**
- **> 50dB LINEAR RANGE**
- **LOW POWER**
- **SELF CONTAINED/MONOLITHIC**



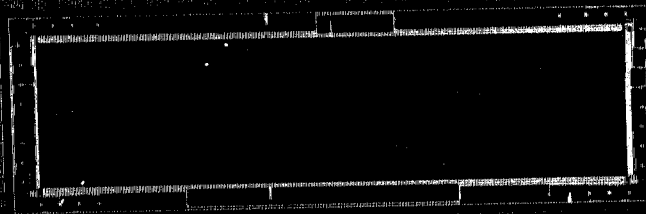
# SERIAL PARALLEL SERIAL MEMORY DEVICE DEVELOPMENT



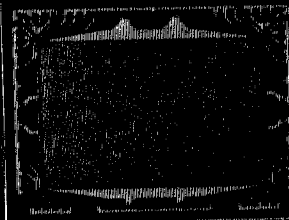
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# SERIAL PARALLEL SERIAL MEMORY DEVICES

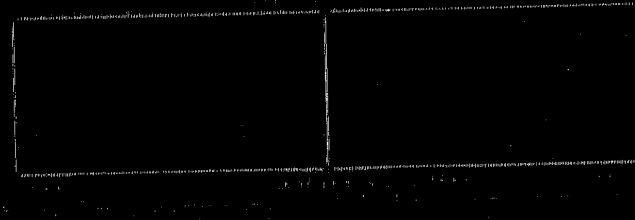
**MAD20128**



**SPS III**



**M720A**



**MAD20128**

- 64K CAPACITY
- 2 POLY
- SINGLE METAL
- BORON/PHOSPHORUS
- ON CHIP NMOS  
CLOCK DRIVERS

**SPS III**

- 16K CAPACITY
- 3 POLY
- SINGLE METAL
- ALL PHOSPHORUS
- STEPPED DOPING
- ON CHIP NMOS  
CLOCK DRIVERS

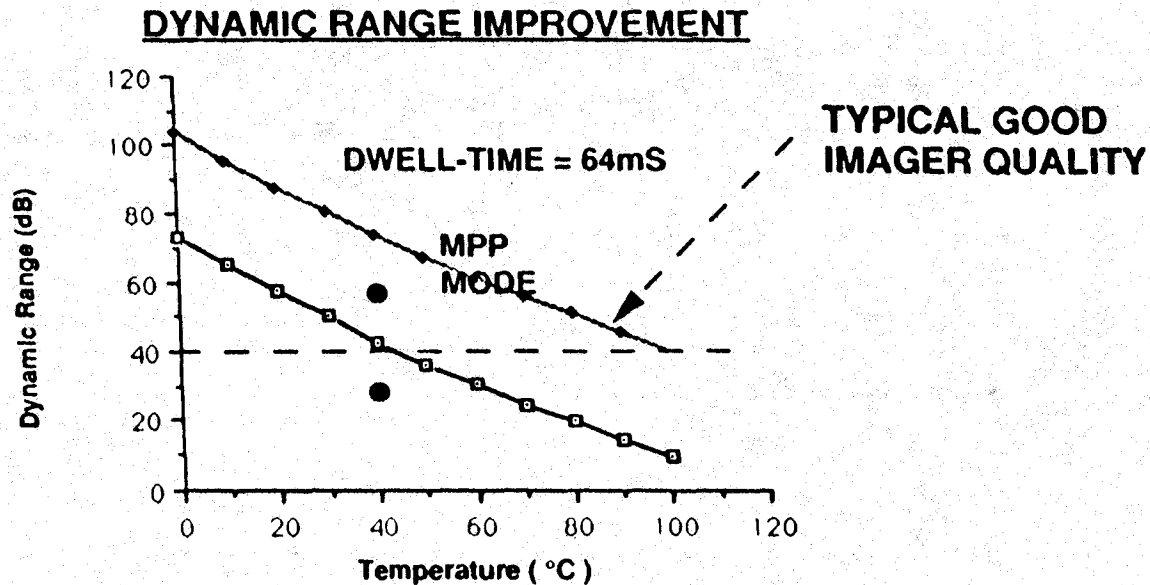
**M720**

- 2 X 32K CAPACITY
- 2 POLY
- SINGLE METAL
- ALL PHOSPHORUS
- FULL DIFFERENTIAL



178596-4

## HIGH-SPEED SPS BUFFER MEMORY MULTIPHASE-PINNED MODE OF OPERATION



- SUBSTRATE TEMP RANGE INCREASE FROM 40 TO 100°C
- LOW STANDBY POWER VIA CMOS MPP CLOCK DRIVERS



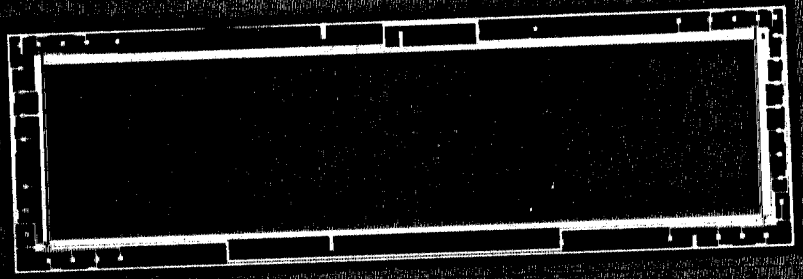
# HIGH SPEED MEMORY

## REQUIREMENTS

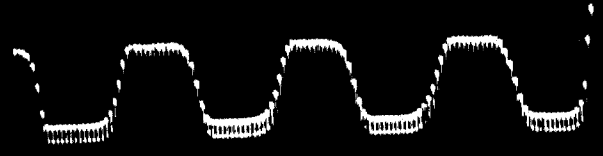
- 150 - 200 MHZ SAMPLING
- 64K SINGLE CHIP
- MONOLITHIC STRUCTURE (Low Power)

## ACHIEVEMENTS

- 150 - 200 MHZ SAMPLING
- 64K SAMPLES
- 35 DB SINGLE ENDED
- 45 DB FULL DIFFERENTIAL



64K MEMORY DIE



A3 -182 U

50mV 1 254ns

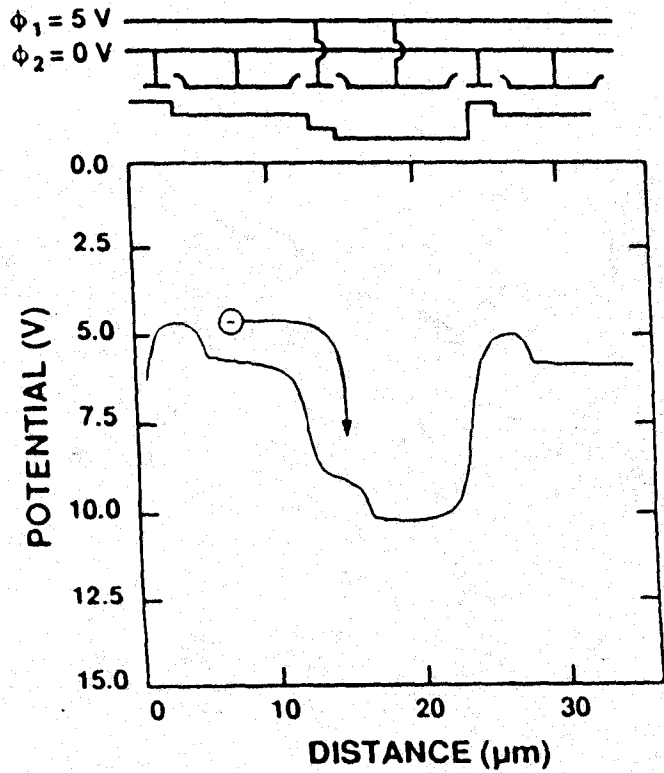
150 MSPS SAMPLING



178586-2

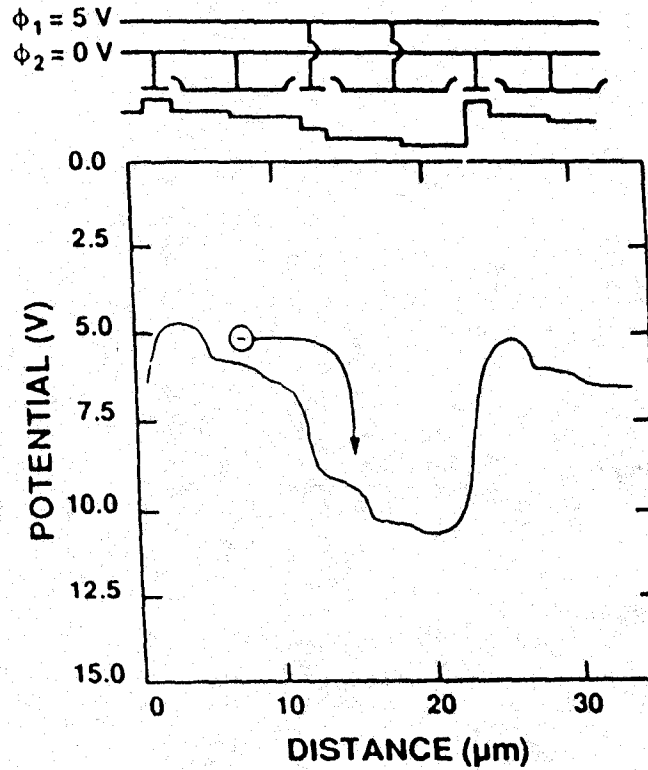
# SHORT-GATE CCDs: $L = 7 \mu\text{m}$

## UNIFORM



SINGLE ELECTRON TRANSIT  
TIME = 0.8 ns

## STEP-DOPED



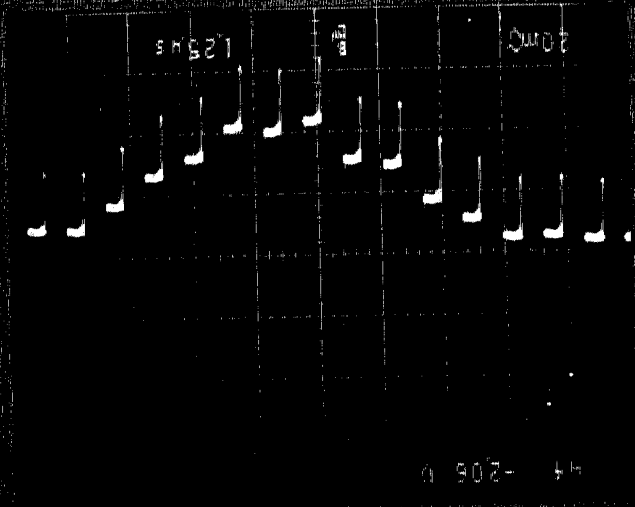
SINGLE ELECTRON TRANSIT  
TIME = 0.45 ns



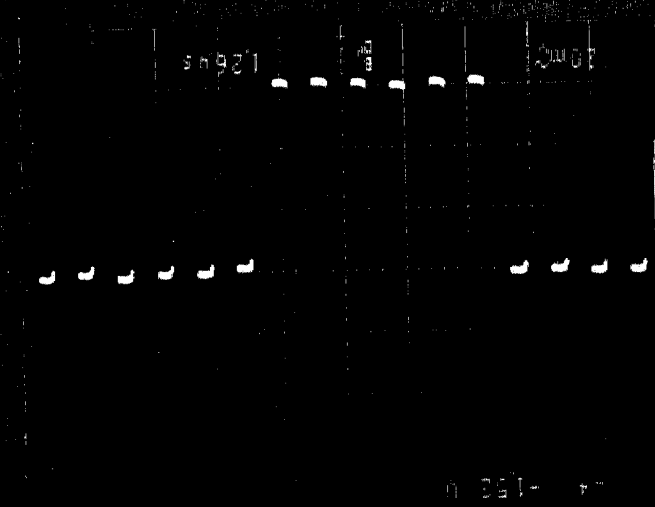
162575-1

# CCD BUFFER MEMORY SPEED ENHANCEMENTS

UNIFORM DOPING



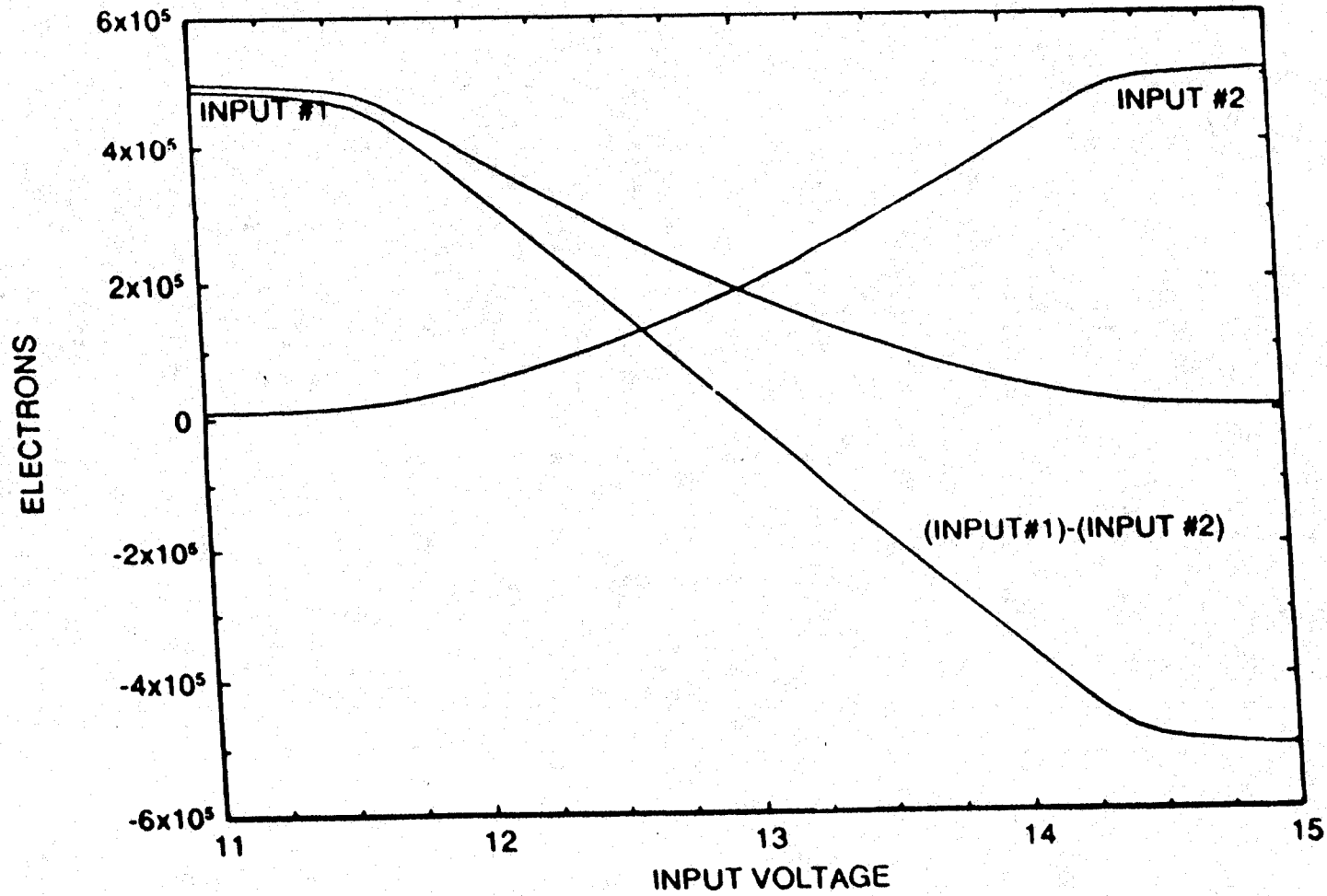
STEPPED DOPING



- IMPROVED CHARGE TRANSFER EFFICIENCY ACHIEVED USING NON-UNIFORM ION IMPLANTS
- DRIFT FIELD ENHANCEMENT ALLOWS FOR CMOS CLOCK LEVELS WHILE MAINTAINING REQUIRED SPEED

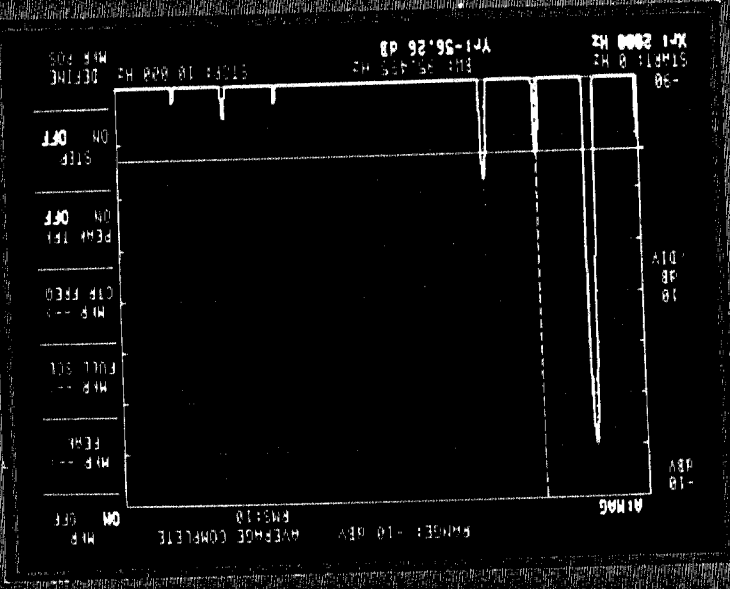


# DIFFERENTIAL OPERATION LINEARITY ANALYSIS

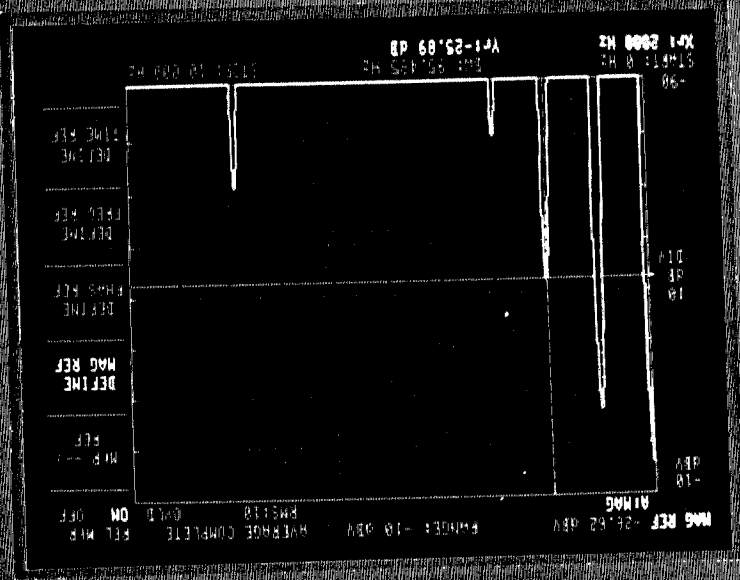




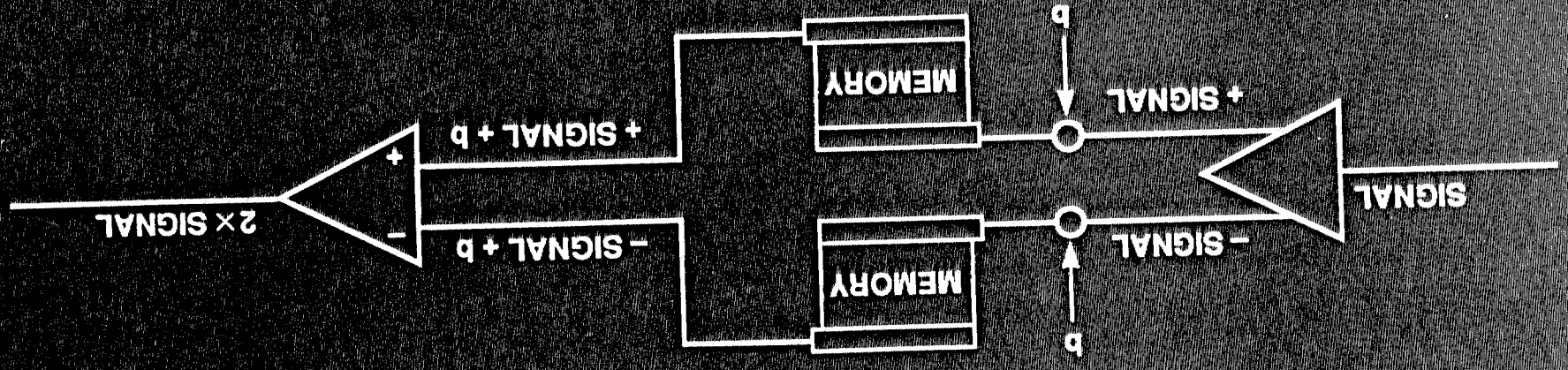
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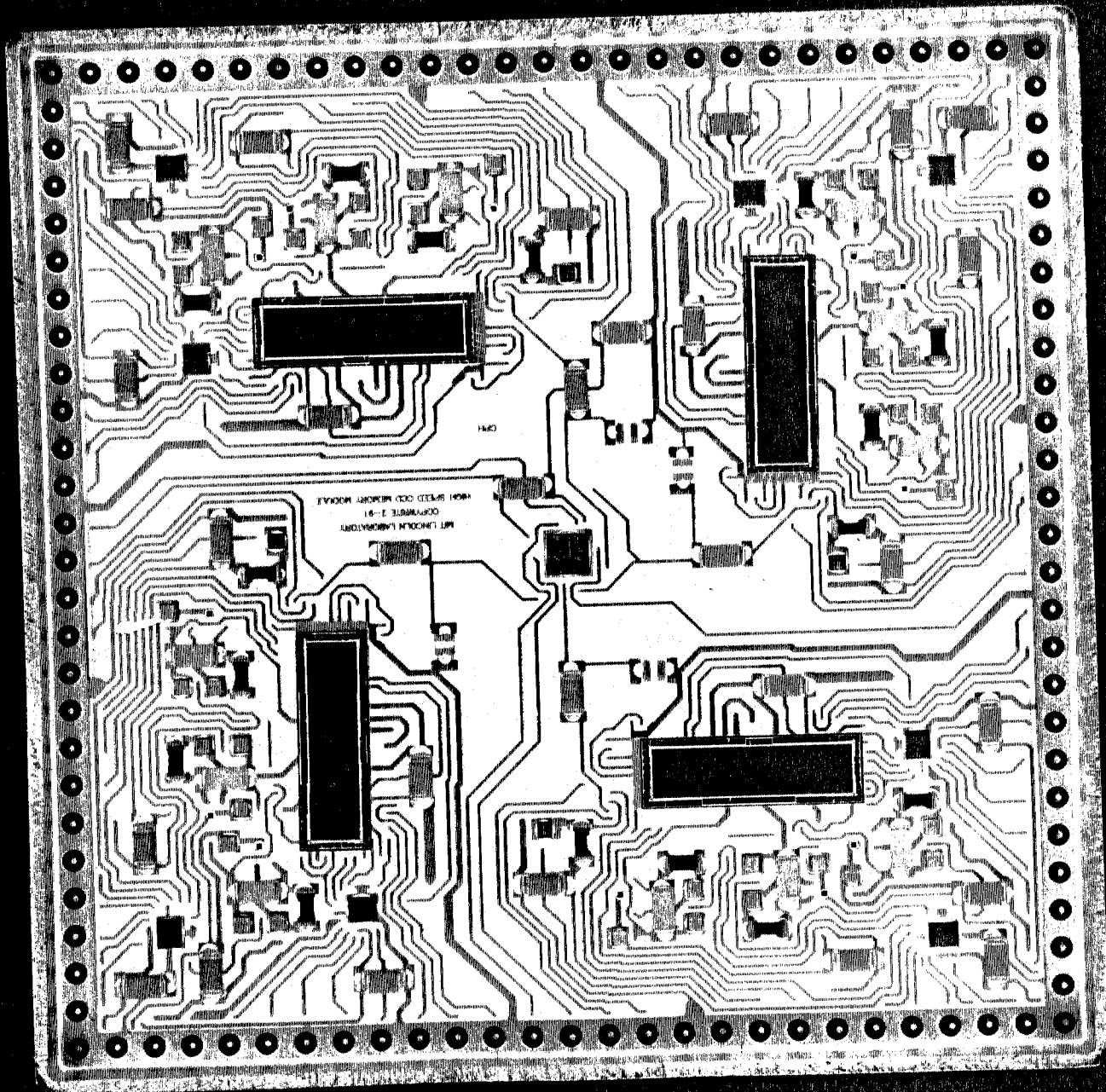
FULL DIFFERENTIAL SPS SPECTRUM



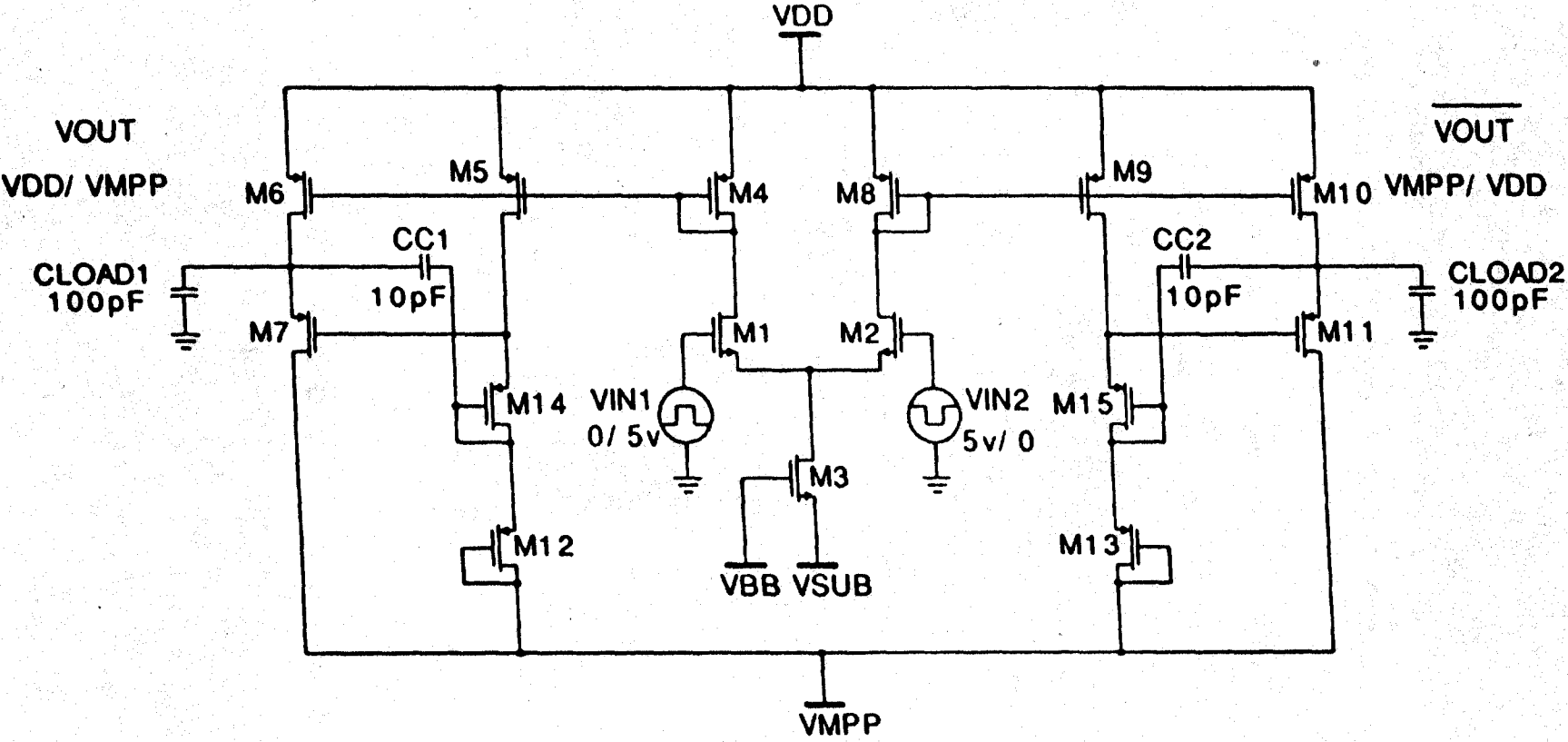
SINGLE ENDED SPS SPECTRUM



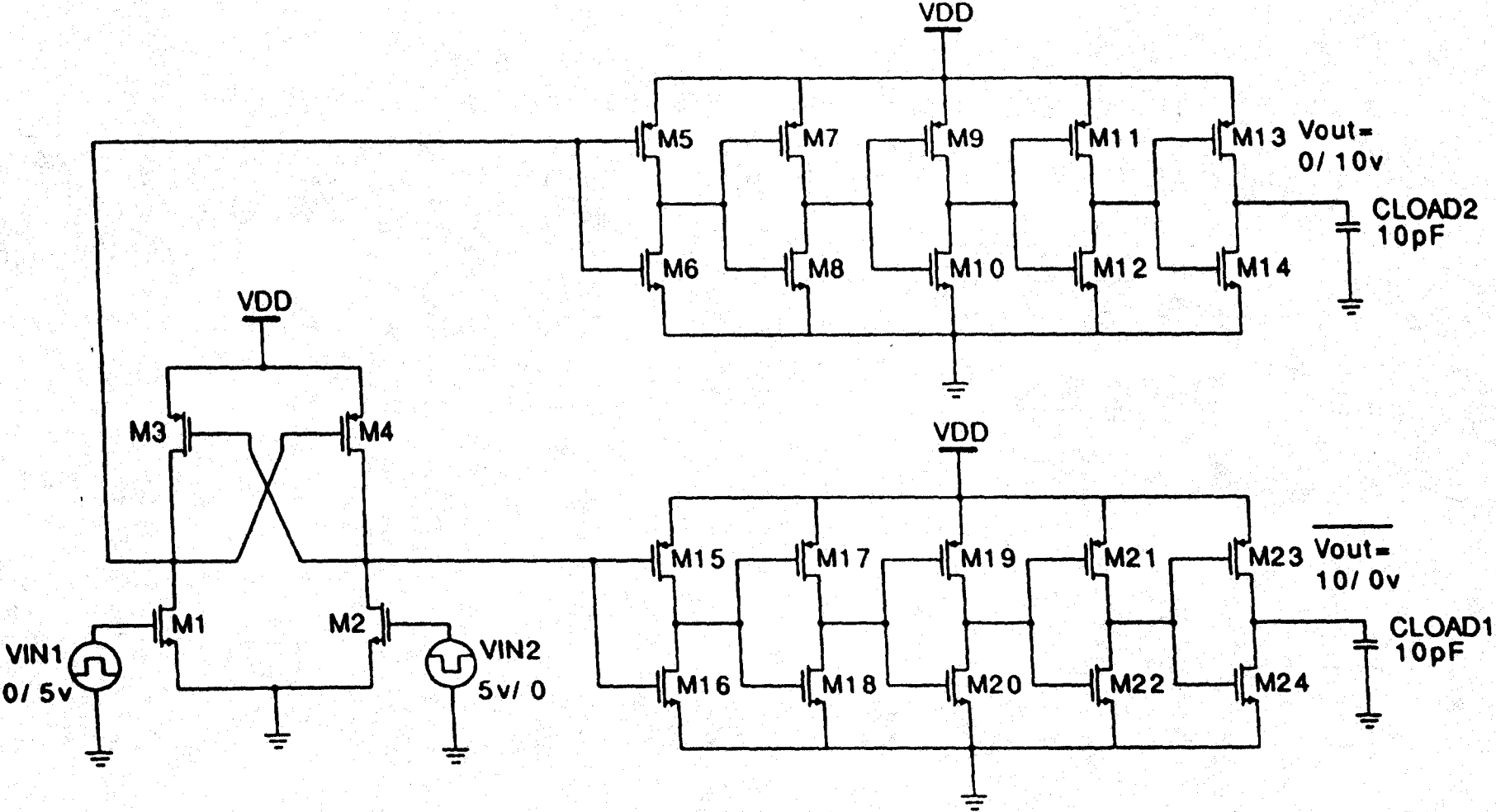
FULL DIFFERENTIAL SPS MEMORY ARCHITECTURE

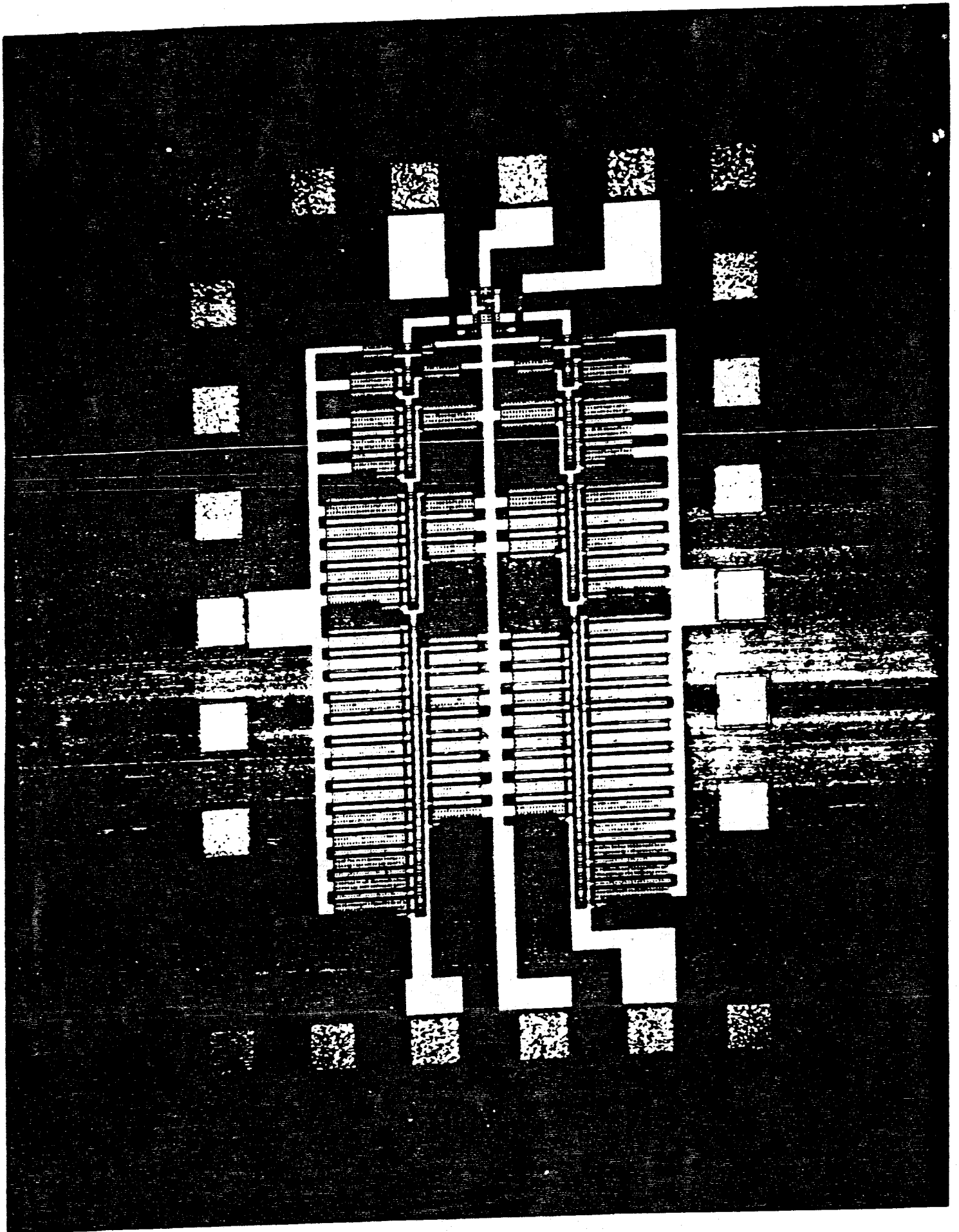


# CMOS MPP DIFFERENTIAL CLOCK DRIVER



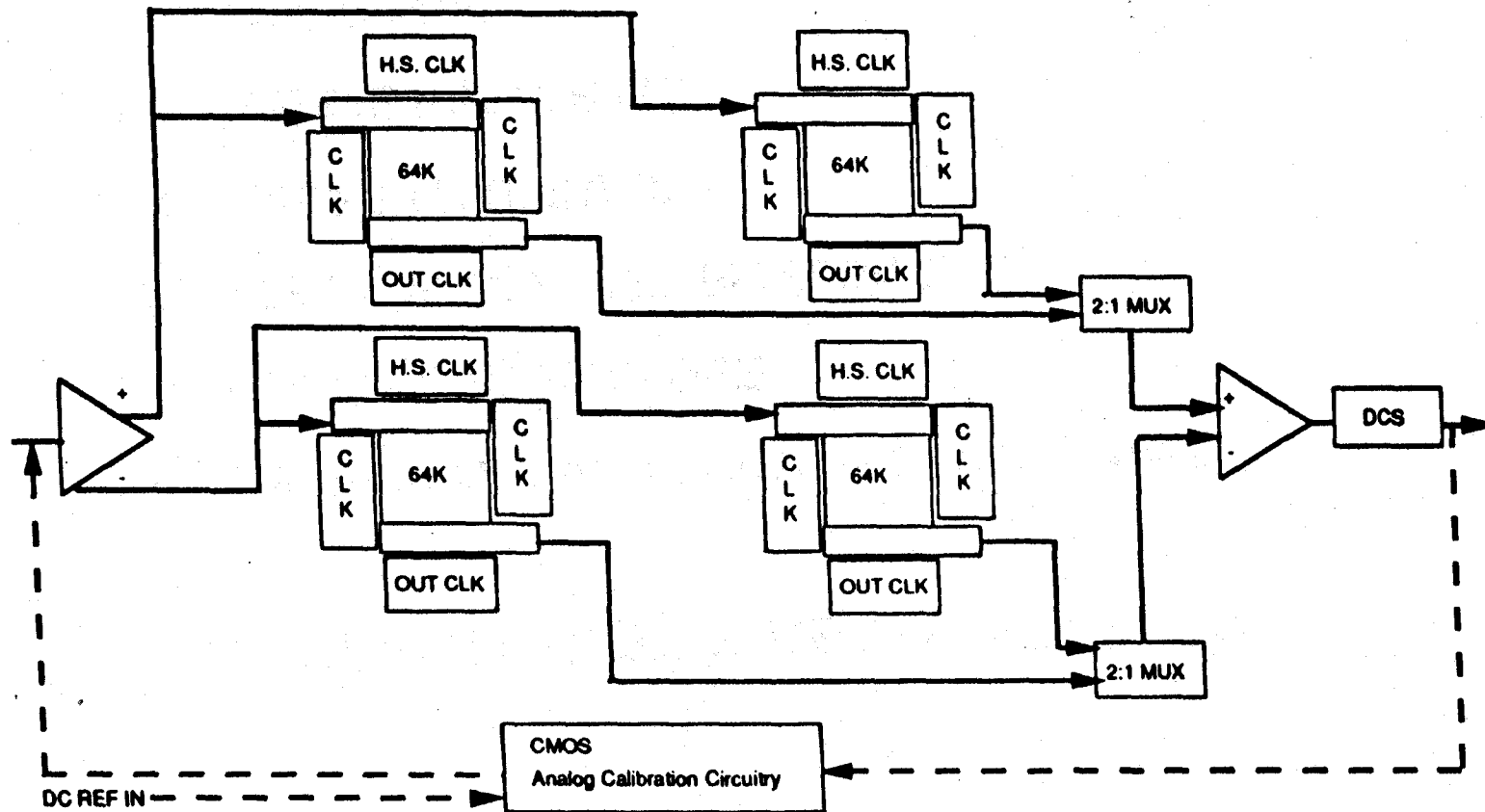
# CMOS HIGH SPEED DIFFERENTIAL CLOCK DRIVER





UNCLASSIFIED

# HIGH-SPEED SPS MONOLITHIC MEMORY



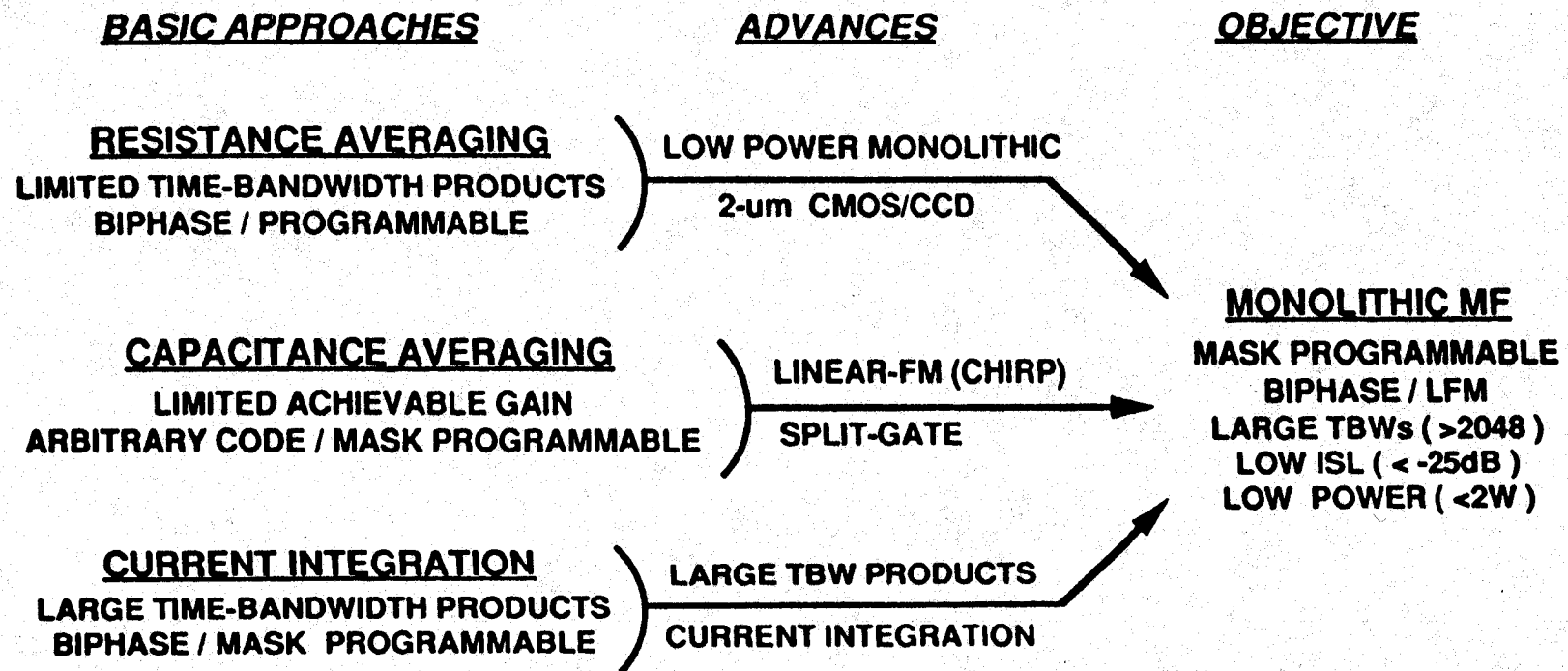
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## **MATCHED FILTER REQUIREMENTS**

- **LARGE TIME-BANDWIDTH PRODUCT (>1024)**
- **> 50dB PEAK/SIDELOBE**
- **> 25dB INTEGRATED SIDELOBE**
- **LINEAR-FM/BIPHASE**
- **10MSPS INPUT RATE**
- **LOW POWER**
- **SELF CONTAINED/MONOLITHIC**

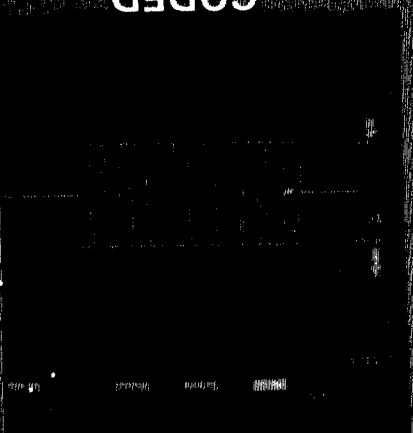


# MATCHED FILTER DEVELOPMENT OVERVIEW

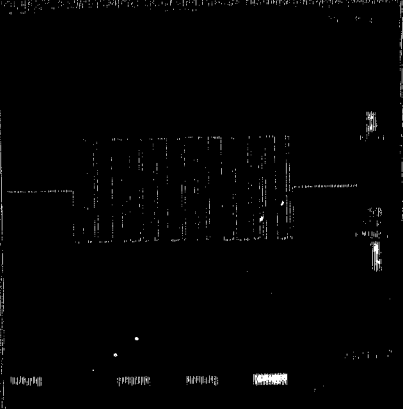


# CCD ANALOG/BINARY MATCH FILTER

CODED SIGNALS



CODE



CODE

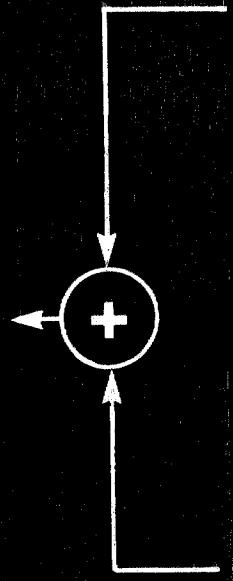
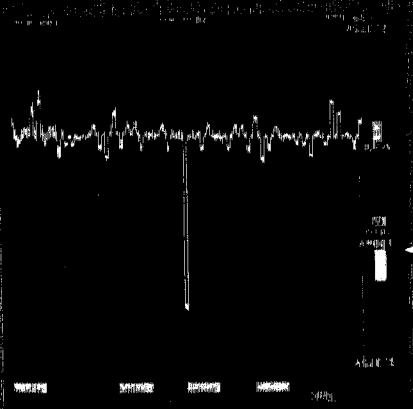
CODE



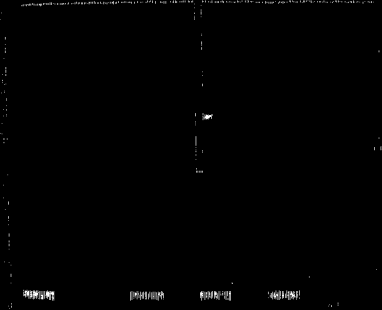
AUTOCORRELATION



CODE



FULL COMPRESSION

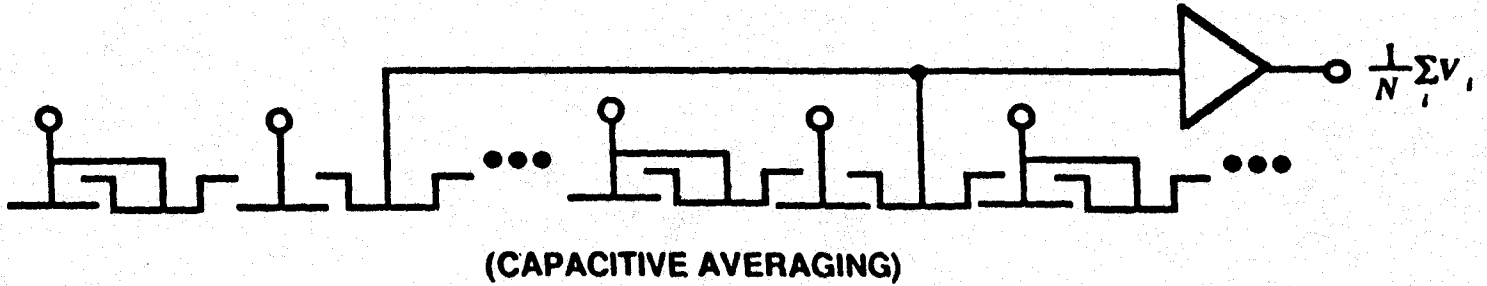


106561-2

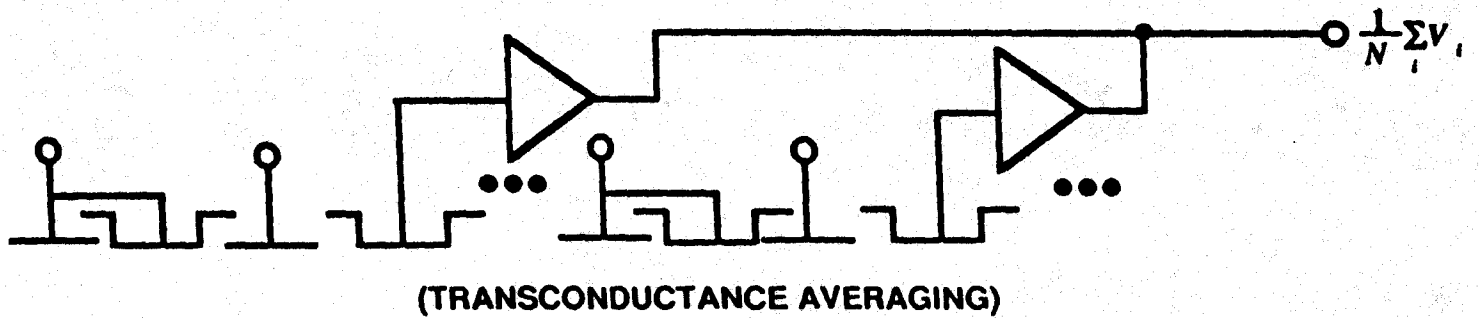


# CCD TRANSVERSAL FILTER IMPLEMENTATIONS

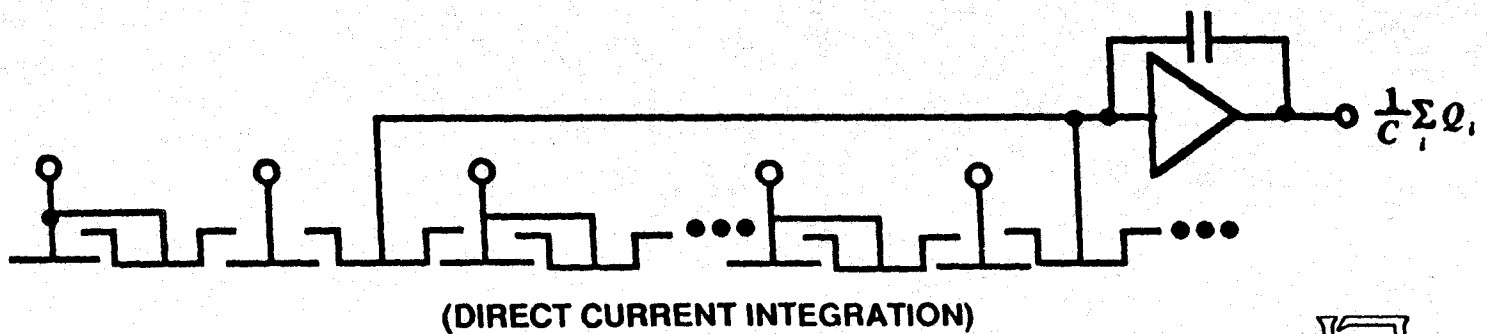
Limited  
Gain



Limited  
TB



Limited  
Speed

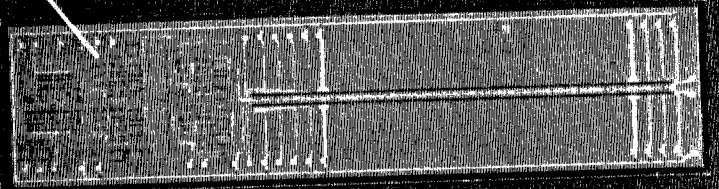




# CCD BIPHASE MATCHED FILTERING

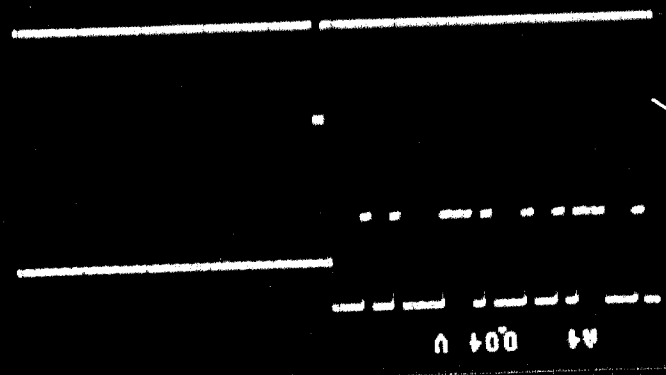


CCD/MOS IMPLEMENTATION



CCD/CMOS IMPLEMENTATION

ON CHIP  
CMOS ANALOG  
CIRCUITRY



N = 512 GOLAY CODE MATCHED FILTER

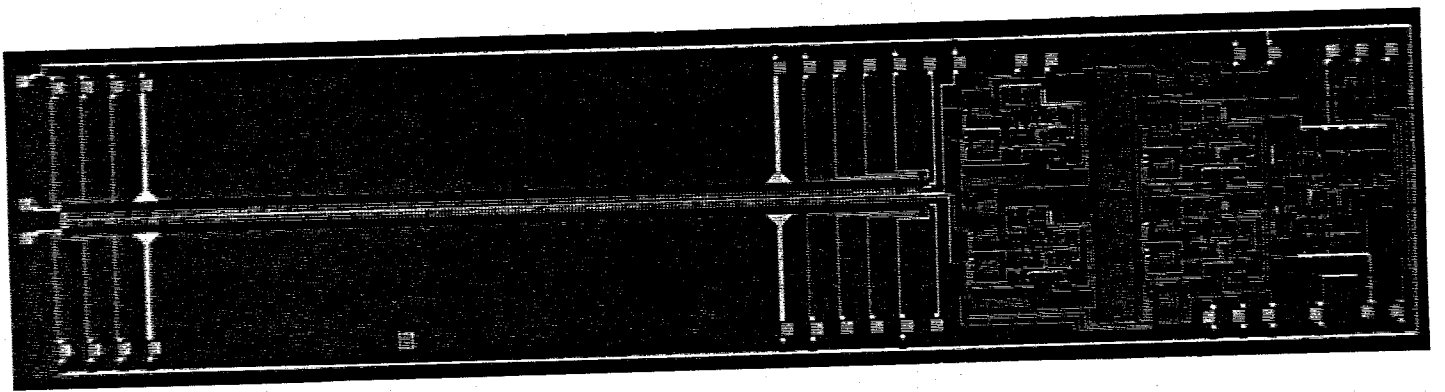
20 10 5ms

## DESIGN APPROACH

- DIFFERENTIAL CURRENT SENSING
- FLOATING GATE/CURRENT MODE
- CONCEPT EXPANDABLE TO INCORPORATE LINEAR (Nonlinear) FM

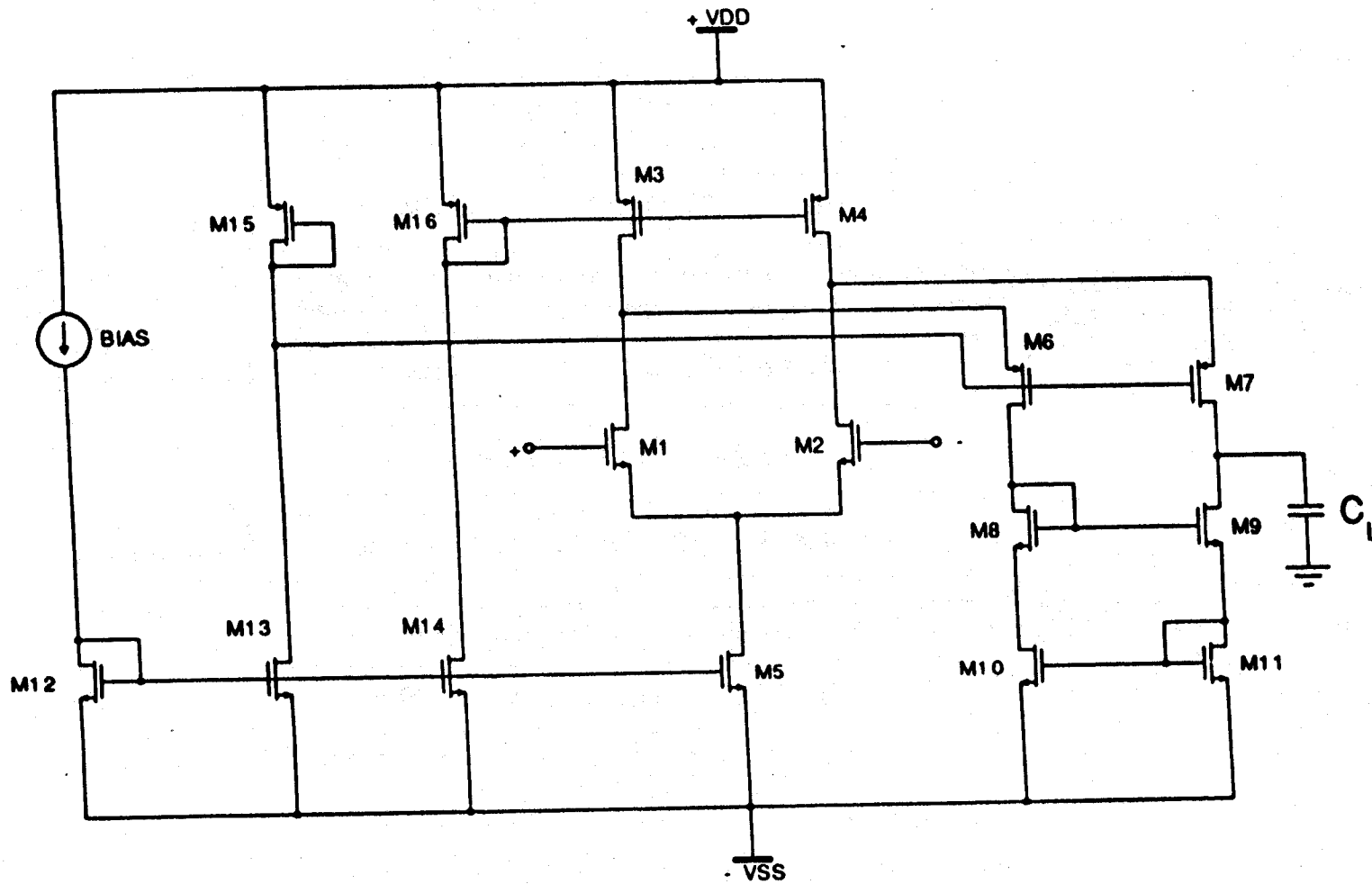
## TEST RESULTS

- 50 dB S/N
- 40 dB LINEARITY
- 60 dB DYNAMIC RANGE
- 25 dB ISL



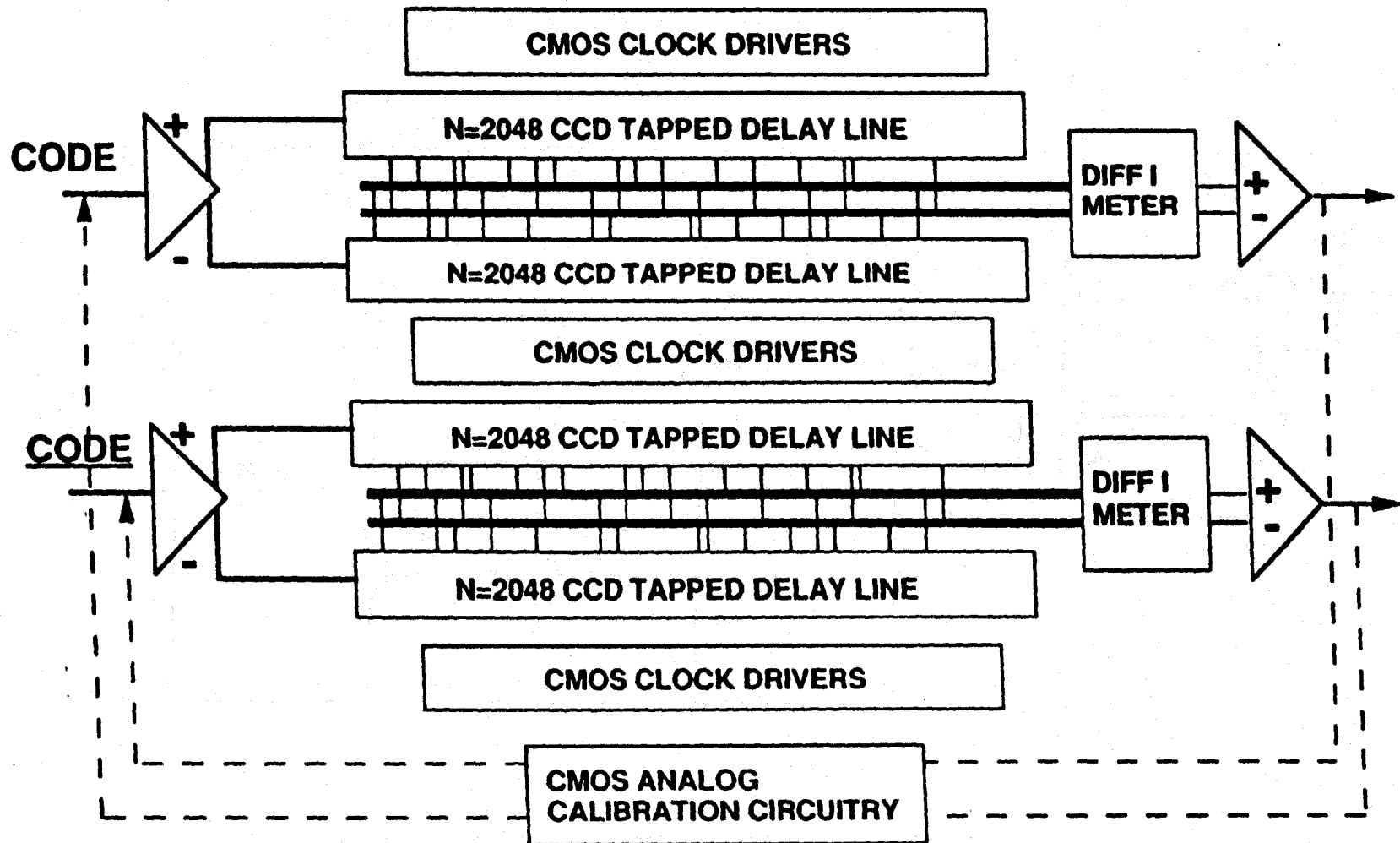


# CMOS FOLDED-CASCADE OPAMP



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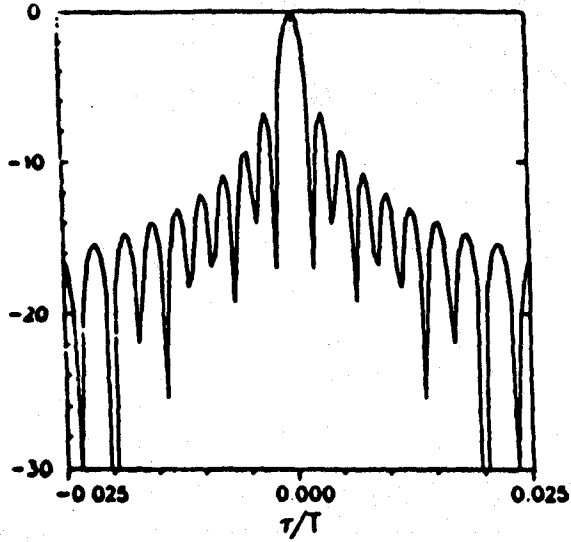
# MONOLITHIC MATCHED FILTER



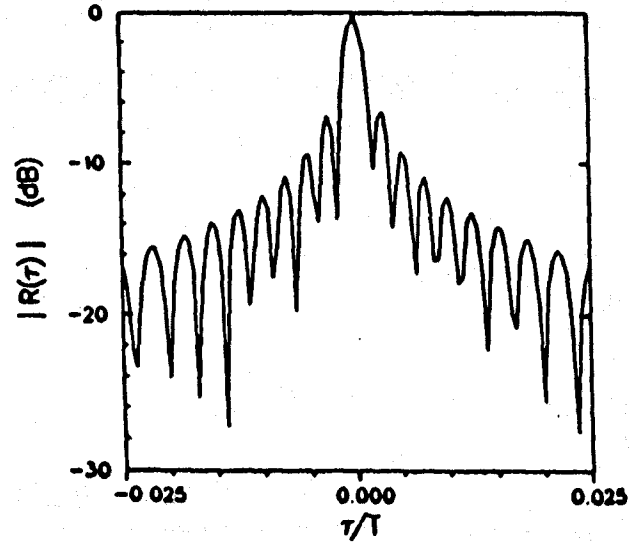
UNCLASSIFIED

2000 WELLS

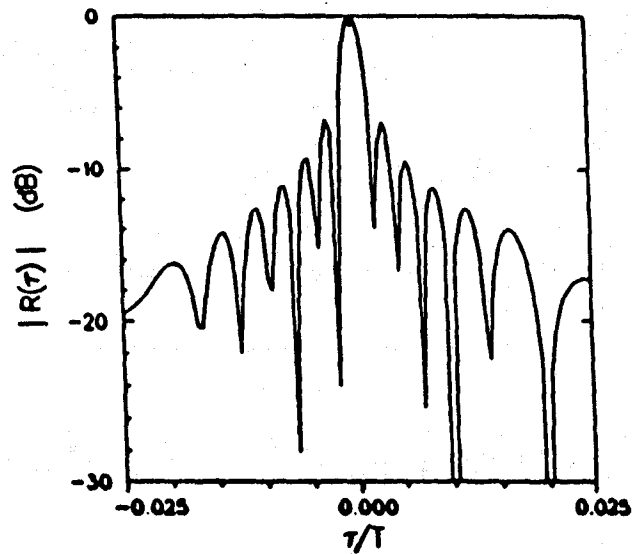
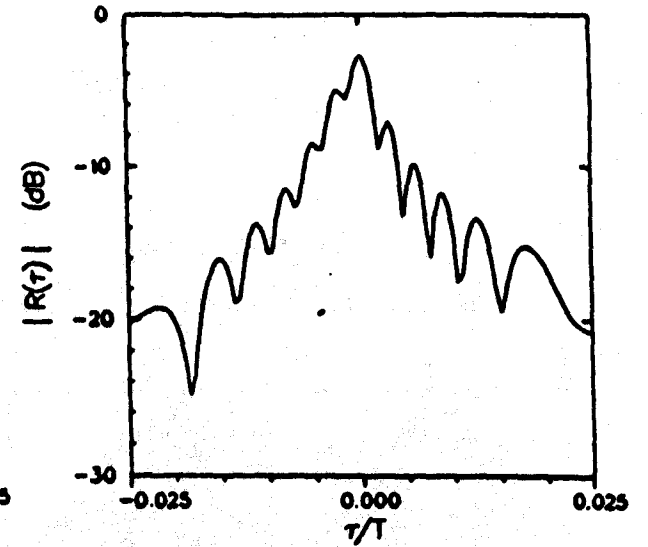
$\delta = 0.0$



$\delta = 0.00025$

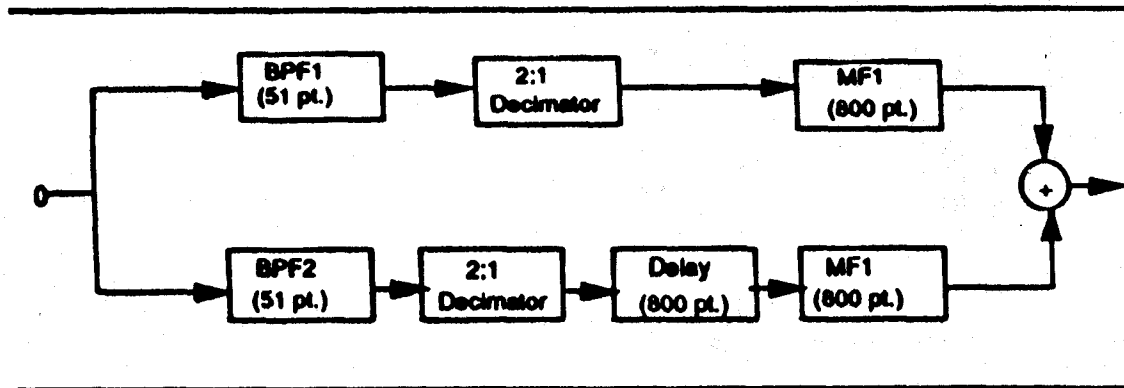


$\delta = 0.0025$

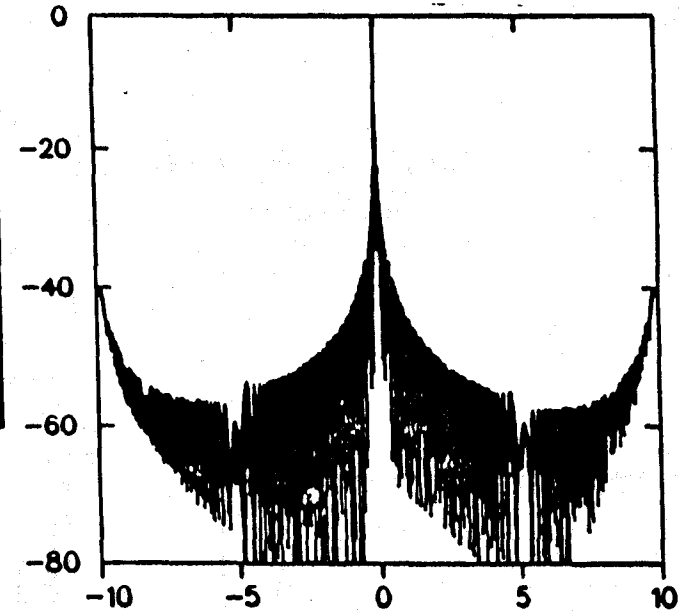


$\delta = 0.0025$   
Modified Weights

# MATCHED FILTER IMPLEMENTATION



**PARALLEL ARCHITECTURE**



**MATCHED FILTER RESPONSE  
(N=3200 LFM)**

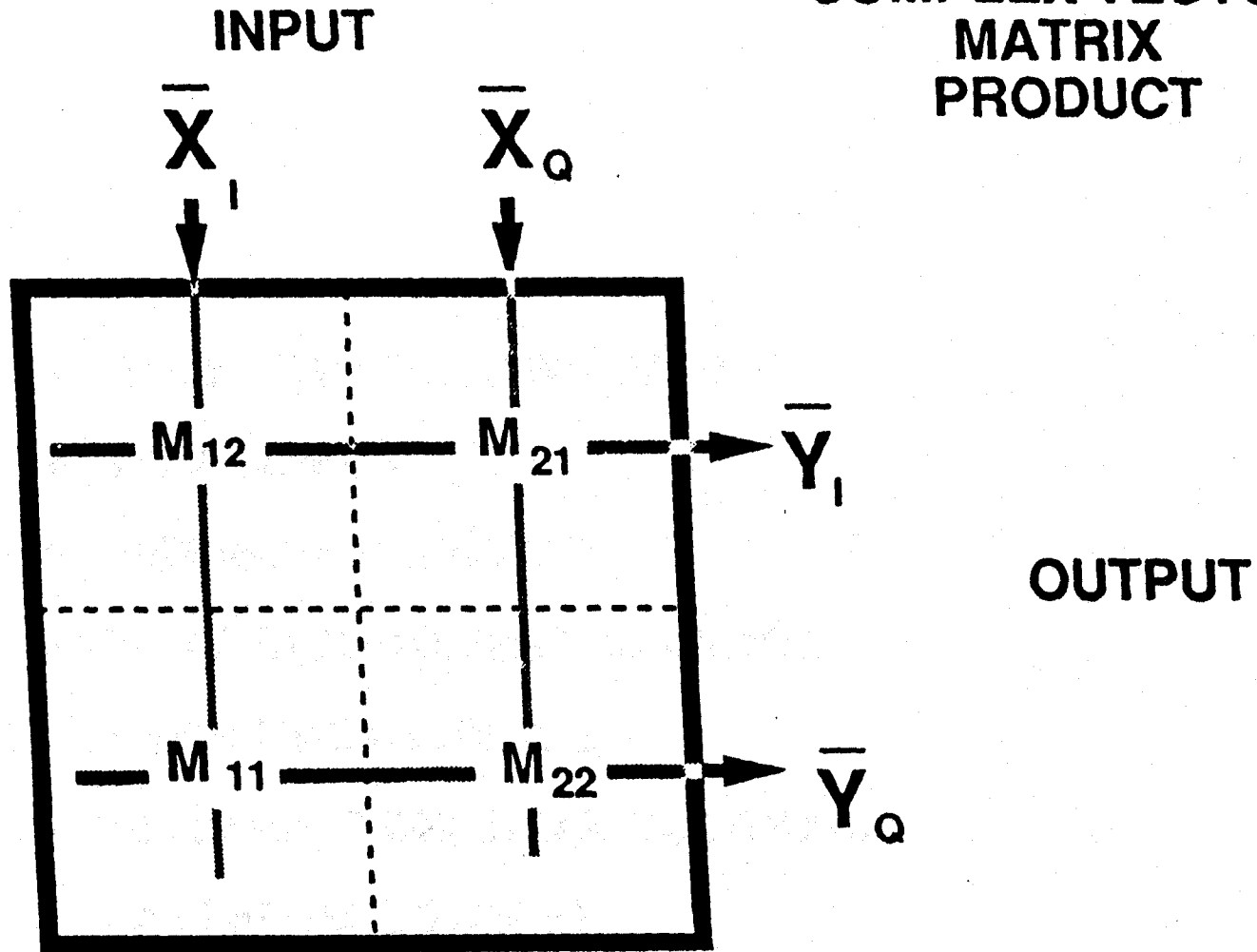
- **REQUIRED TIME-BANDWIDTH PRODUCT ACHIEVED USING AVAILABLE CMOS/CCD TECHNOLOGY**
- **APPLICABLE TO BI-PHASE/LINEAR (NON-LINEAR) FM**
- **INPUT BANDPASS FILTER CHOSEN TO MAXIMIZE PULSE COMPRESSION GAIN**

## **DFT/BEAMFORMER REQUIREMENTS**

- **16-32 POINT COMPLEX**
- **>50dB NULL DEPTH/1% ACCURACY**
- **>50dB LINEAR RANGE**
- **>60dB INSTANTANEOUS RANGE**
- **10MSPS INPUT RATE**
- **LOW POWER**
- **SELF CONTAINED/MONOLITHIC**



COMPLEX VECTOR  
MATRIX  
PRODUCT

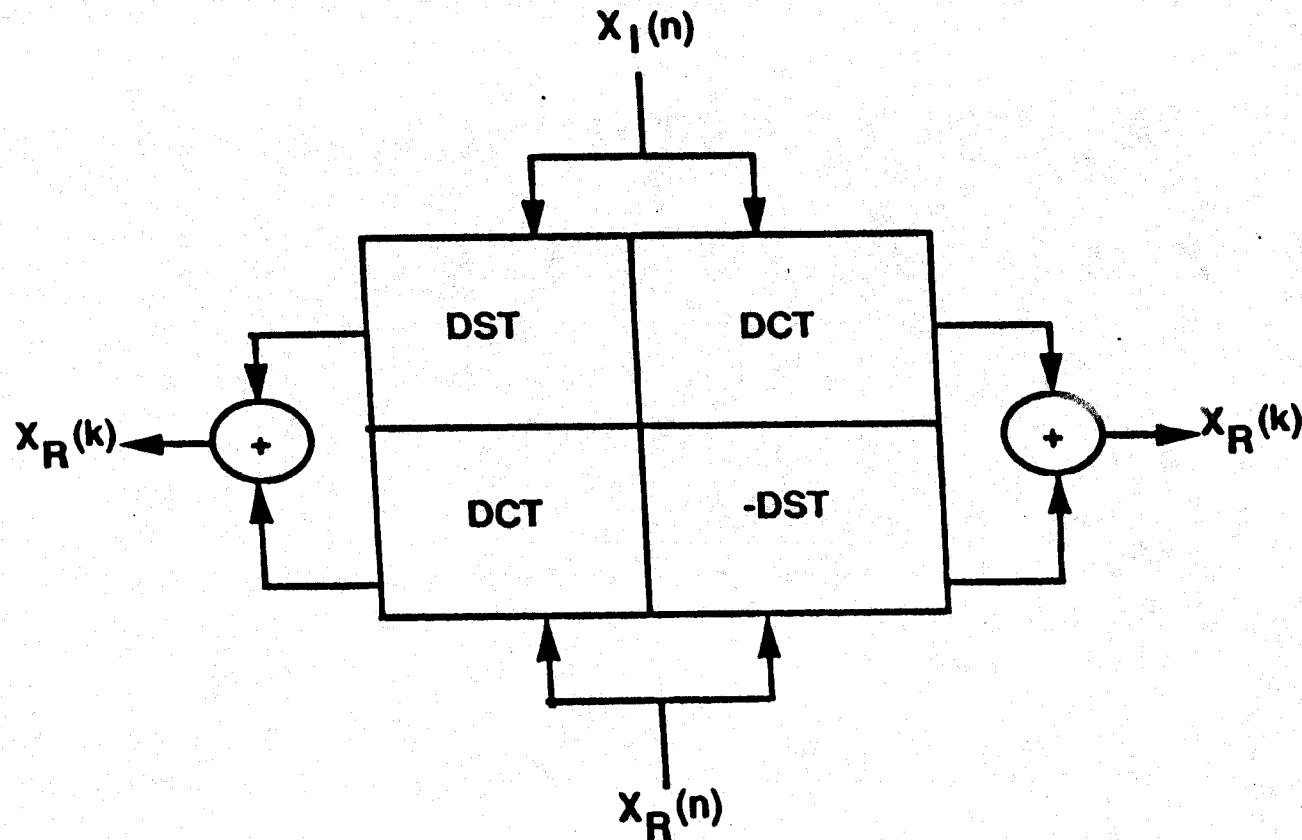


$$\begin{bmatrix} \bar{Y}_I \\ \bar{Y}_Q \end{bmatrix} = \begin{bmatrix} M_{12} & M_{21} \\ M_{11} & M_{22} \end{bmatrix} \begin{bmatrix} \bar{X}_I \\ \bar{X}_Q \end{bmatrix}$$

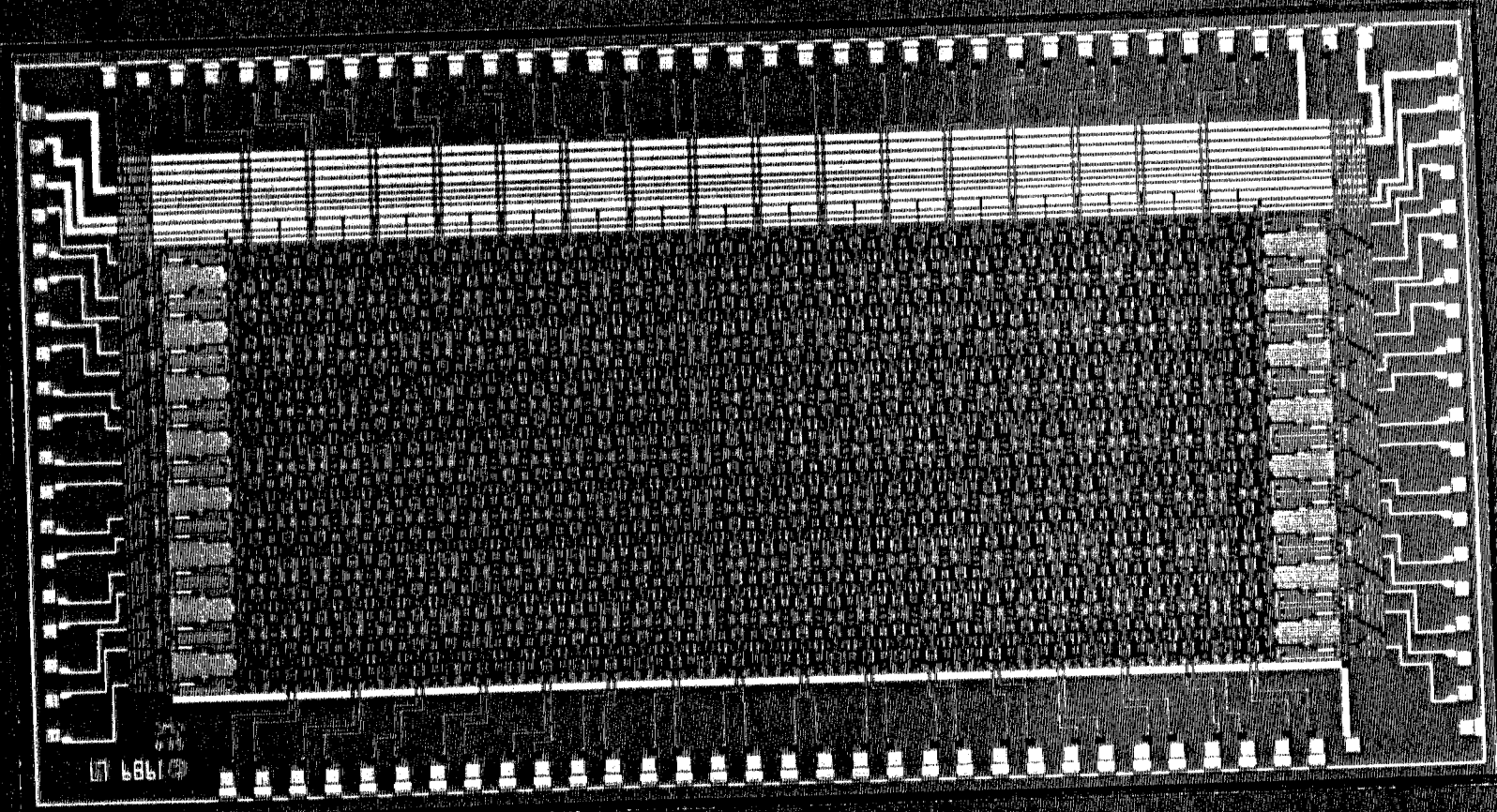
# CCD DFT IMPLEMENTATION

$$X(k) = \sum_n x(n) e^{-j \frac{2\pi nk}{N}} = \sum_n [x_R(n) + jx_I(n)] \left[ \cos\left(\frac{2\pi nk}{N}\right) - j \sin\left(\frac{2\pi nk}{N}\right) \right]$$

$$= \underbrace{\left[ \sum_n x_R(n) \cos\left(\frac{2\pi nk}{N}\right) + \sum_n x_I(n) \sin\left(\frac{2\pi nk}{N}\right) \right]}_{x_R(k)} + j \underbrace{\left[ \sum_n x_I(n) \cos\left(\frac{2\pi nk}{N}\right) - \sum_n x_R(n) \sin\left(\frac{2\pi nk}{N}\right) \right]}_{x_I(k)}$$



# ADVANCED CCD DISCRETE FOURIER TRANSFORM (DFT) DEVICE



## IMPROVEMENT FACTORS

- INCREASED LINEARITY AND DYNAMIC RANGE
- ELIMINATE BIASES
- REDUCED CLOCK LOADING
- FULL SPEED THROUGHPUT

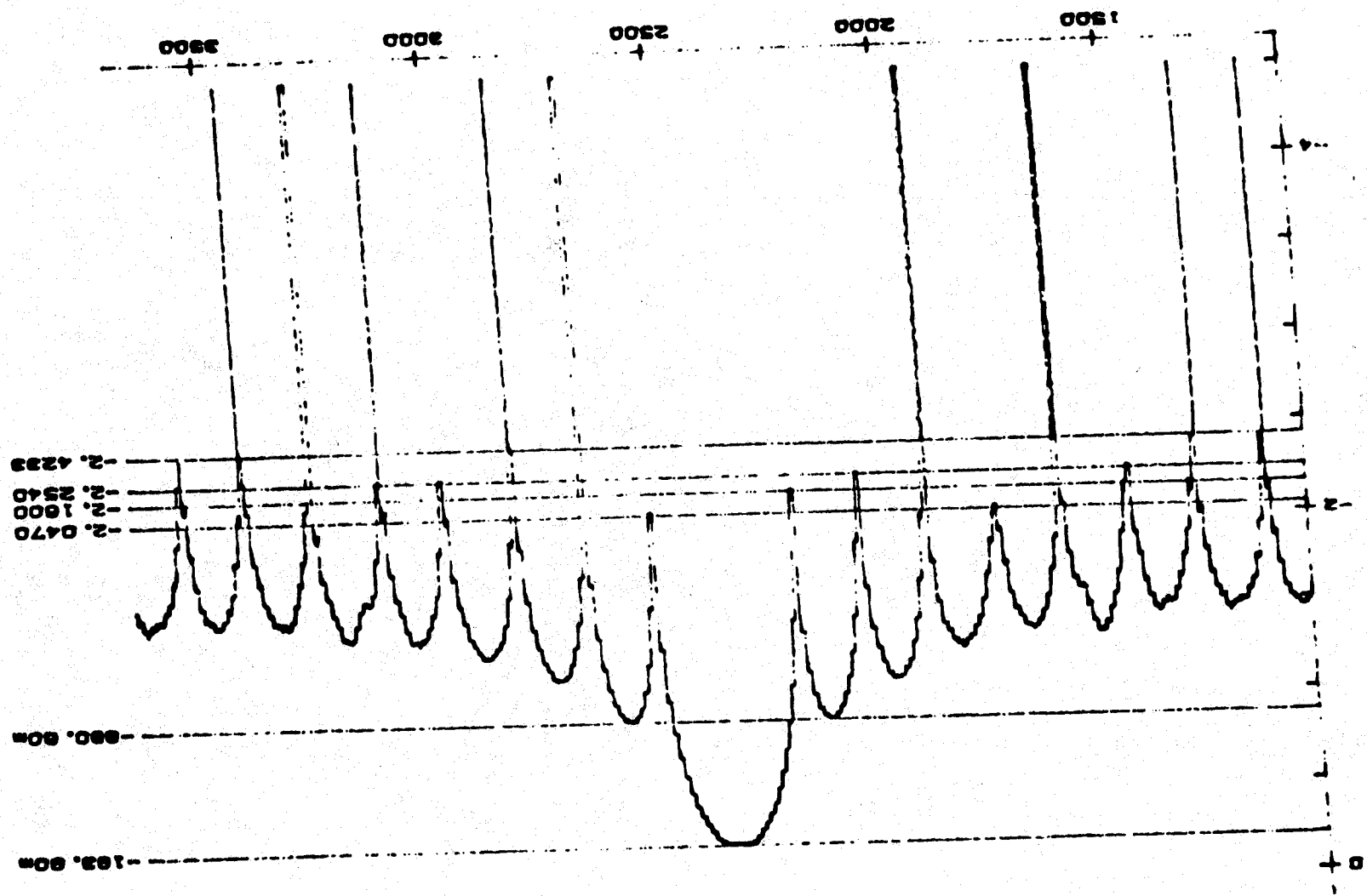
## NEW DESIGN FEATURES

- SINGLE (+) WELL TYPE
- FULLY DIFFERENTIAL INPUT/OUTPUT
- DIODE CUTOFF INPUT
- FULL METAL STRAPPING
- REFINED OUTPUT BUFFERS AND RESETS



172978-4

CLK



1.0GSQ