Low Noise Charge Sensing at the output of a CCD

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LOW NOISE CHARGE SENSING AT THE OUTPUT OF A CCD

SUBJECT HEADINGS

1. State of the art of low noise MOS-CCDs and FETs

    Noise performance of (a) JFETs and MOSFETs
    (b) typical CCD MOSFETS
    (c) systems using single (discrete) detectors

2. RTS currents in FETs

3. Noise Model and Verification

    Construction of noise spectra from RTS currents in a FET
    Noise due to bulk Si traps
        $1/f^2$ spectrum in JFET due to single bulk trap
    Noise due to oxide traps
        1/f noise and $1/f^2$ noise in MOSFETs

4. The excess 1/f noise in MOS-CCDS

    The Poole-Frenkel effect
    Dopant segregation at the oxide interface
    Charge confinement; the LOCOS process and channel depth
    The effect of deep channels; Bias conditions for low noise
    Hysteresis and aging of noise in depletion mode MOSFETs

5. Charge detecting field effect transistors (CDFETs)

    Floating gate MOSFET and the CDFET
    Predicting the behaviour from RTS current theory
    Transfer function and linearity
    MOSFET vs JFET
    Noise floors of a small fraction of 1 e- : photon counting

REFERENCES

S. Ramo, Proc. IRE **24**, 984 (1930)

A.L. McWhorter, *Semiconductor Surface Physics*, edited by R.H. Kingston, (University of Pennsylvania Press, PA, 1956), p. 219.

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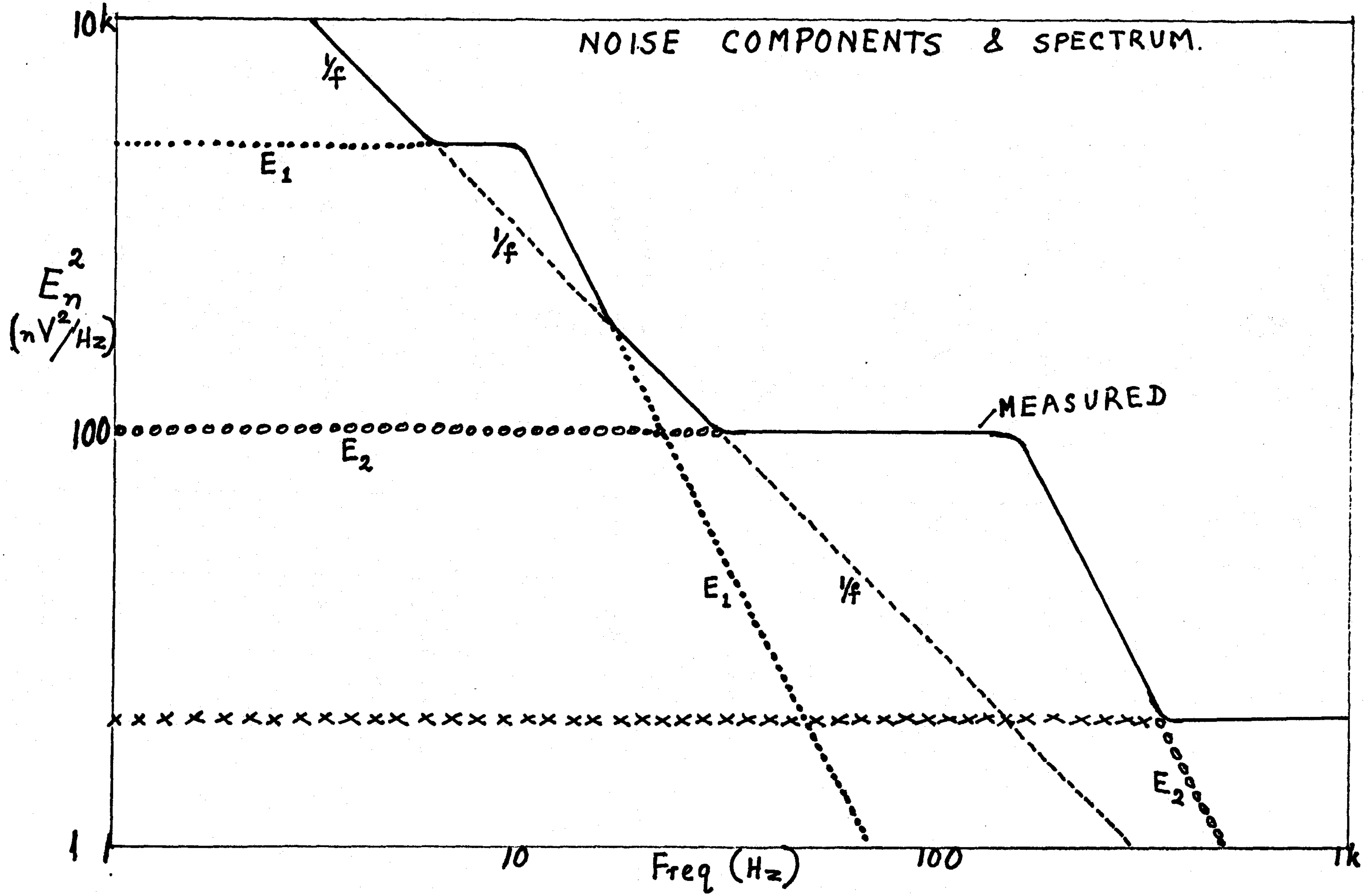
R.J. Brewer, IEEE Trans. Electron Devices, **DE-27**, 401, (1980).

J. Kemmer et al, Nucl. Inst. and Meth. **A288**, 92, (1989).

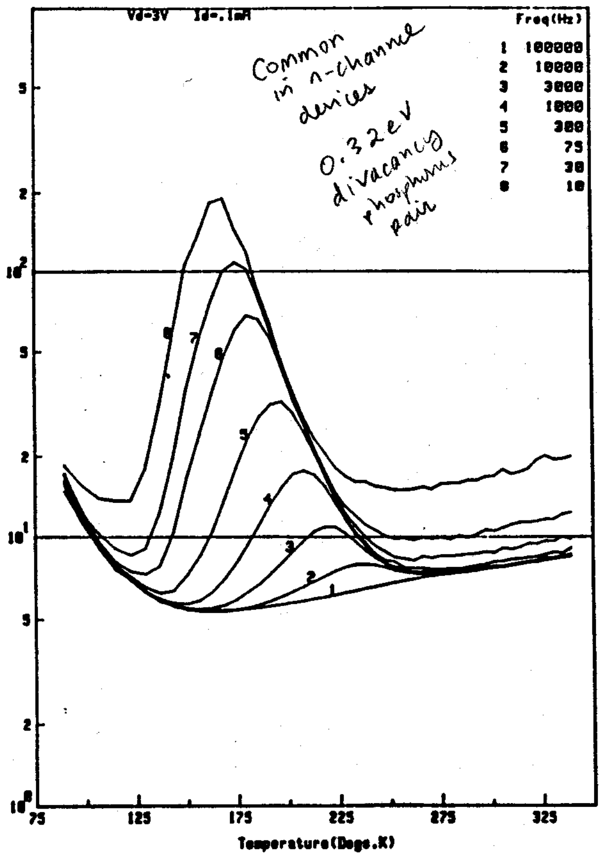
NOISE PERFORMANCE OF CCDS AND SI X-RAY DETECTOR

(electrons rms)

	Sensitivity (μv/ē)	Noise Corner (Hz)	Thermal Noise N_t at 0.1 μs	1/f Noise	N_t Ideal JFET $L = 3\mu m$ $T = 180$ K $t = 0.1$ μs $C = 2$ Cgs
Typical CCD	1	10^6	25	4	14
Low Cap CCD (A)	12	10^4	10 (20 MHz)		4
Low Cap CCD (B)	4	5×10^4	8	2	7
10 mm^2 Si Det	0.08	$<10^3$	100	<5	45


NOISE COMPONENTS & SPECTRUM.
10k
100
1
E_n^2
(nV^2/Hz)
1/f
E1
1/f
MEASURED
E2
E1
1/f
E2
10
100
1k
Freq (Hz)

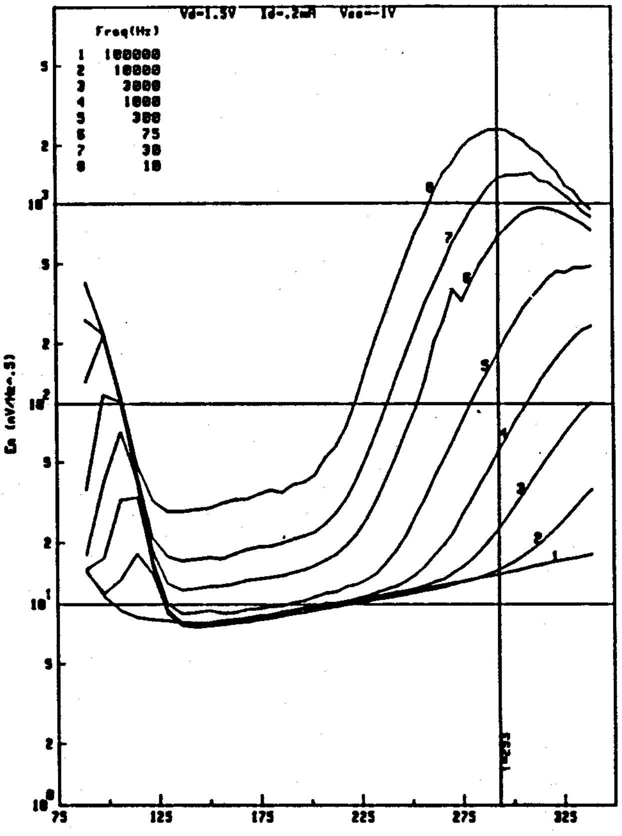
CHARACTERISTICS OF NOISE GENERATED BY A SINGLE TRAP IN JFET VX5165A



Common in n-channel devices

0.32eV divacancy phosphorus pair

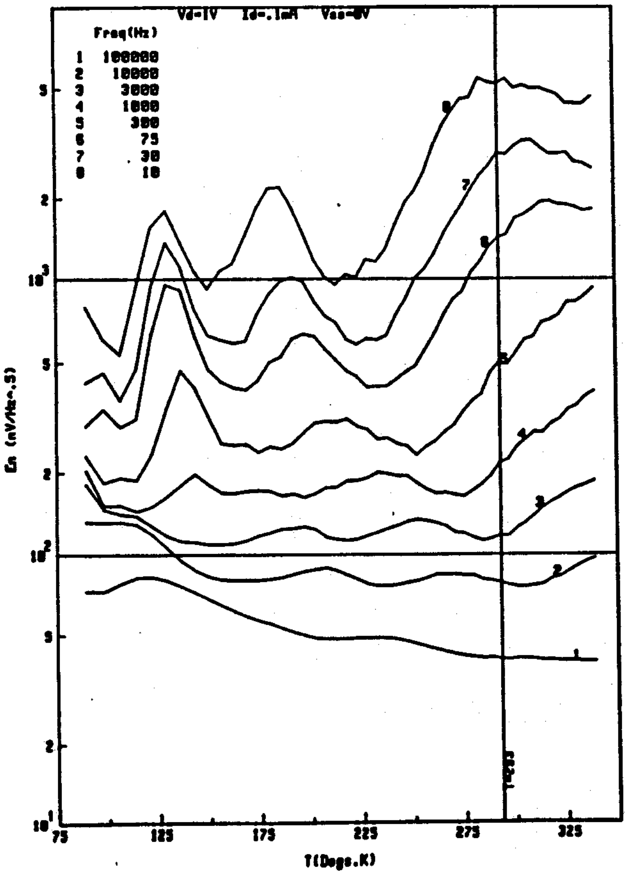
GATE REFERRED NOISE OF DEPLETION MODE MOSFET (100x15)



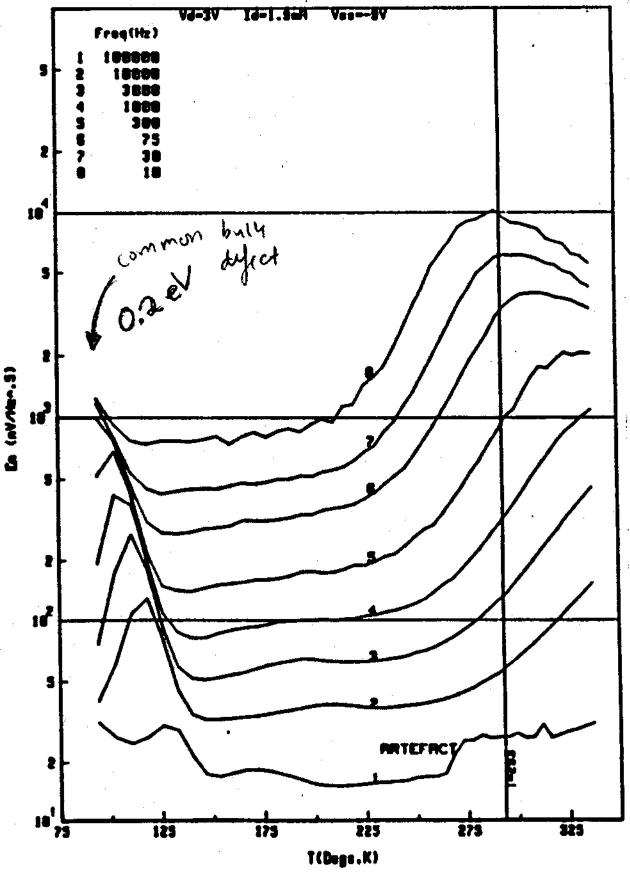
N-WELL w/V_T adj.

usually measure from few μA to 10's mA bias current

GATE REFERRED NOISE OF P-CHANNEL MOSFET (20x1.5); CMOS PROCESS



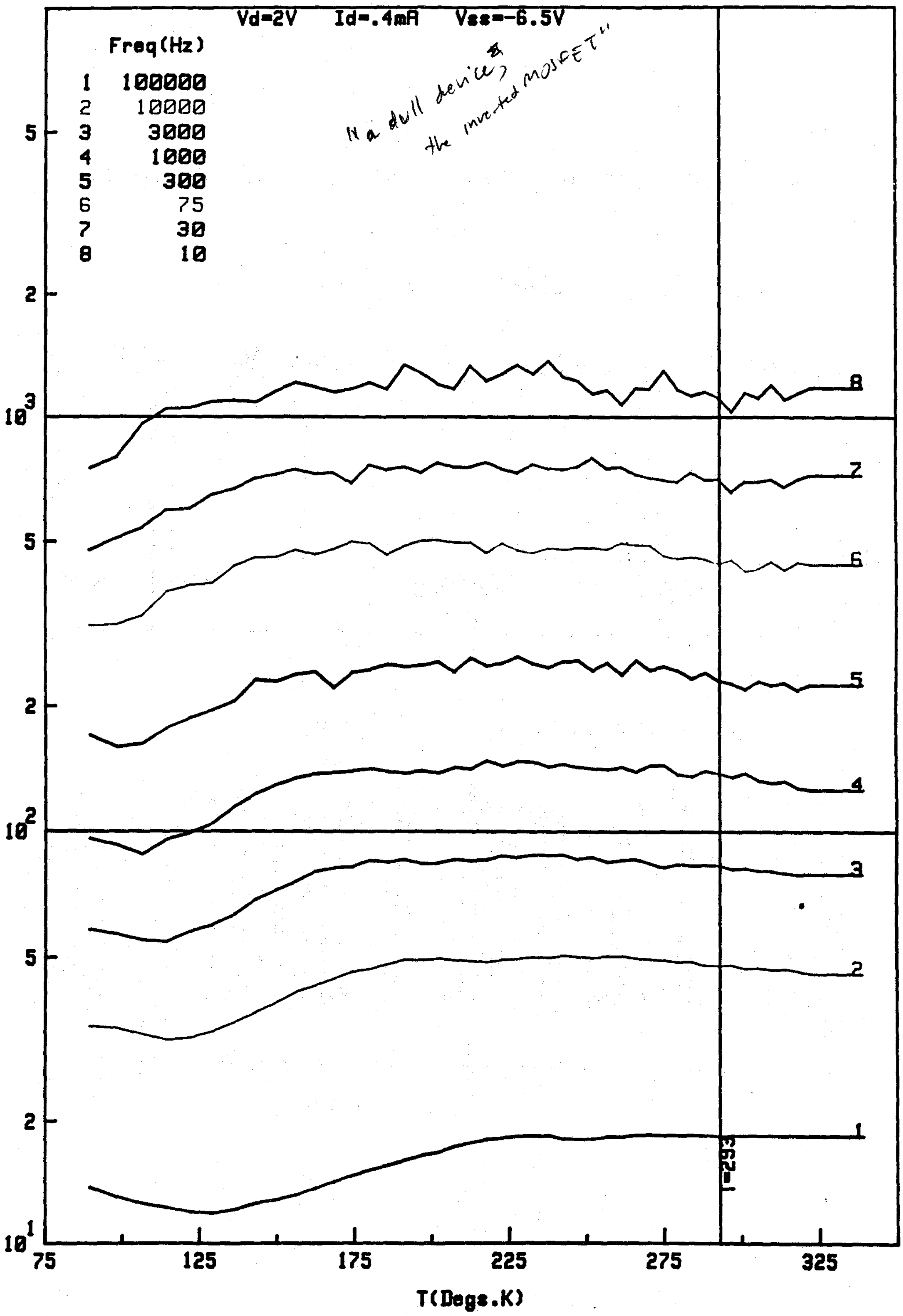
GATE REFERRED NOISE OF DEPLETION MODE MOSFET (64x8) CCD PROCESS



common bulk defect

0.2eV

GATE REFERRED NOISE OF ENHANCEMENT MODE MOSFET (100x15)



"A dull device, the inverted MOSFET" *

Fig.5 EFFECT OF TEMPERATURE (Vd=+60mV, Vg=+.65V)

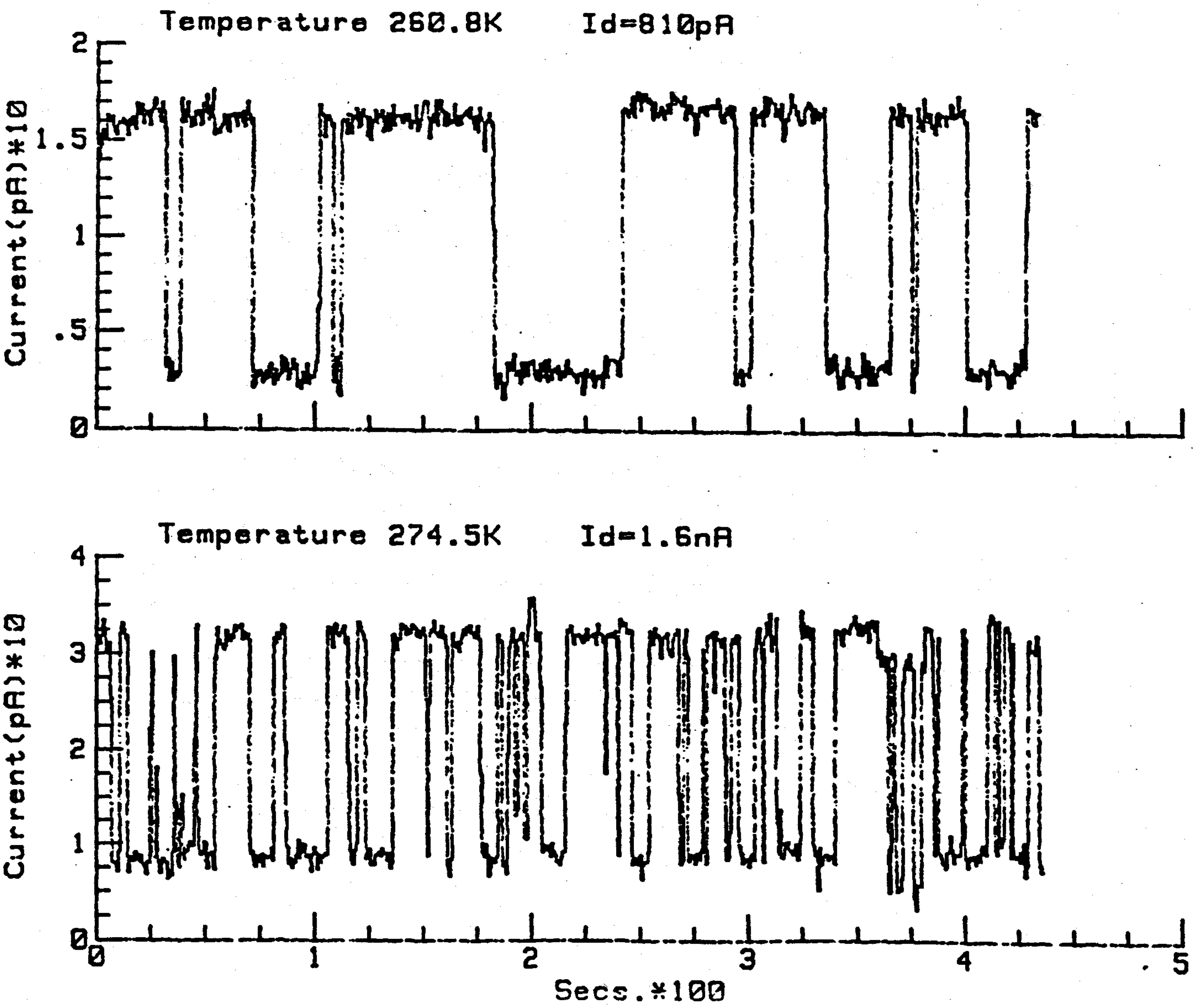
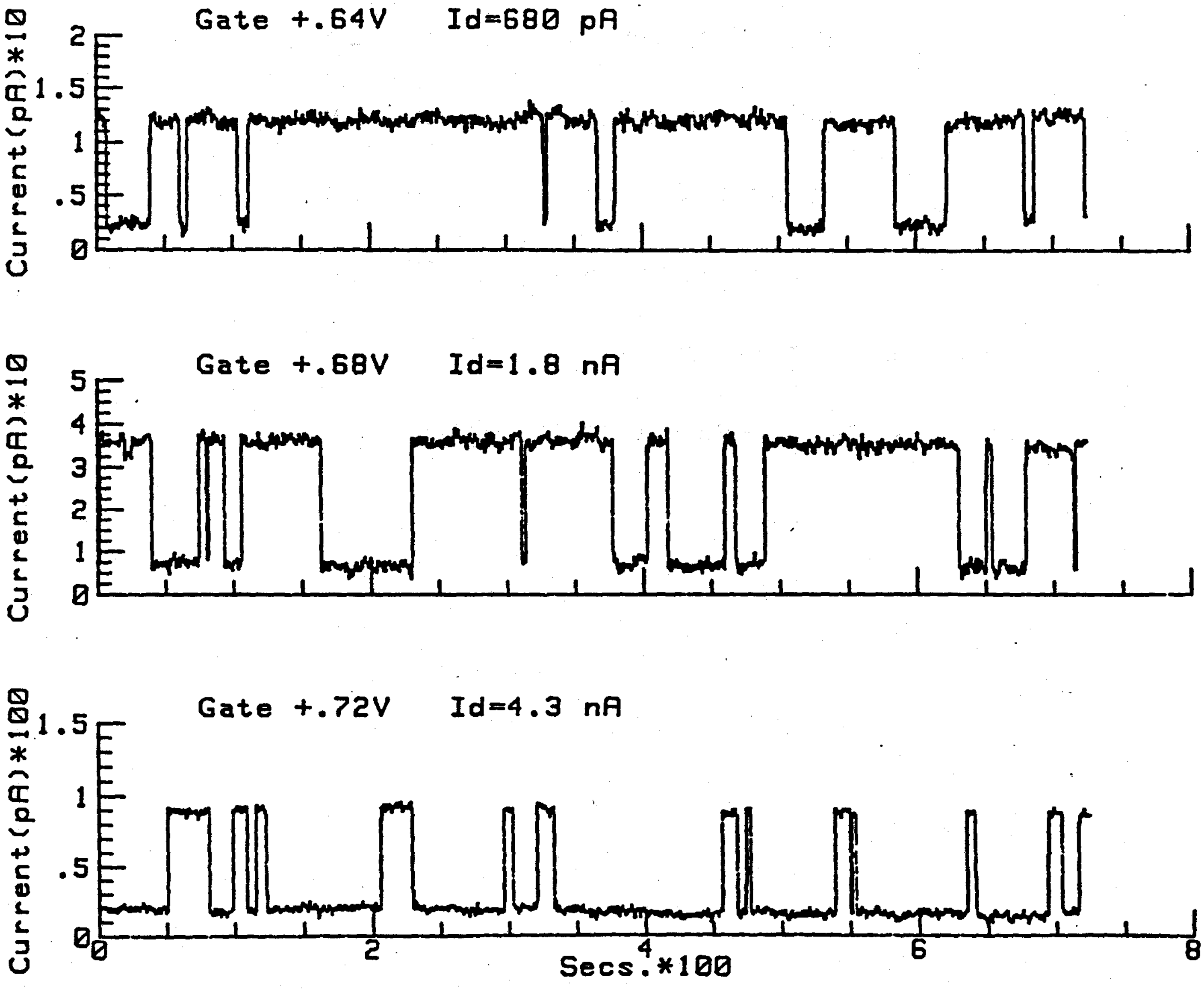


Fig.3 GATE VOLTAGE EFFECTS (Vd=85mV, T=260.8K)


Gate +.64V Id=680 pA

Gate +.68V Id=1.8 nA

Gate +.72V Id=4.3 nA

The noise model assumes that:-

All low frequency noise is generated by bulk Si and oxide traps.

Energy levels, cpature cross sections and densities of all traps are known.

Bulk Si trap density	<	10^{13} cm^{-3}
Bulk Oxide trap density		10^{17} cm^{-3}
Interface state density		10^{10} cm^{-2}
Capture cross section		10^{-15} cm^{2}

Gradual channel approximation.

Thermal velocity saturation of carriers at drain.

Ramo's Theorem

Current induced into an electrode by a moving charge

$$dI = q\,u\,E$$

q = charge

u = velocity in the direction of the field due to the electrode

E = Electric field per volt due to the electrode potential.

Approximation for FET channel

Low field gradual channel

$$dI = q\,u/L$$

L = channel length.

RTS CURRENTS IN FETS

Amplitudes

Extended Ramo's theorem gives drain current amplitude

$$dI= \frac{Gqu}{L}$$

← u has a strong position dependence

where

G=Charge coupling factor to channel — effect of position fudge?

q=Electronic charge

u= Mean local carrier drift velocity

L= Channel length

gate.

$(G=1)$

depletion region $G \simeq$ ~~[illegible]~~

in deBye $G \simeq 1$

in channel $G = 1$

RTS CURRENTS IN FETS

Characteristic times

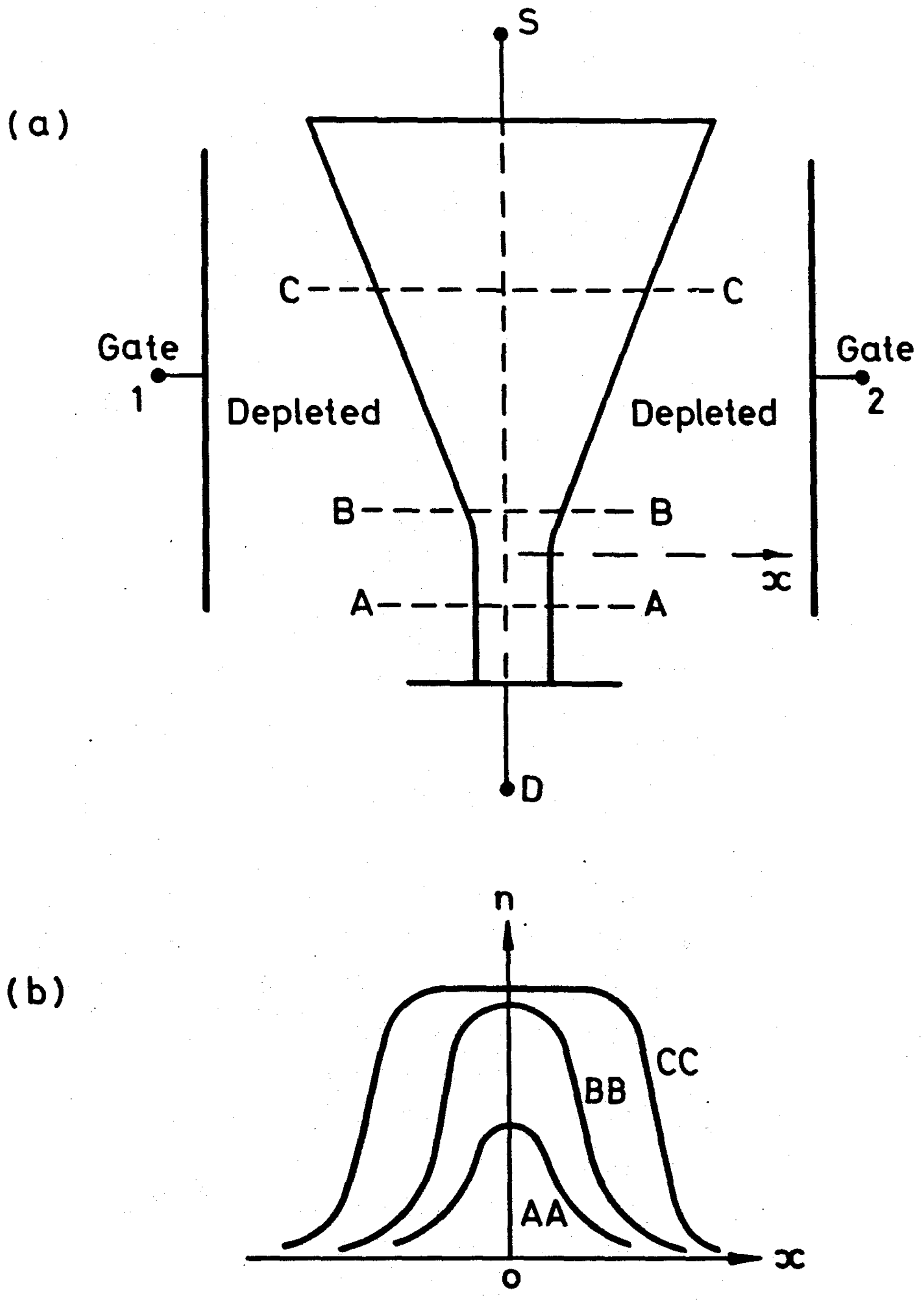
Capture	$\frac{1}{nvc}$
Emission	$\frac{\exp(E_t/kT)}{Nvc}$
Tunnelling	$\frac{\exp(2Ky)}{4nvc}$

time depends a lot on local carrier density

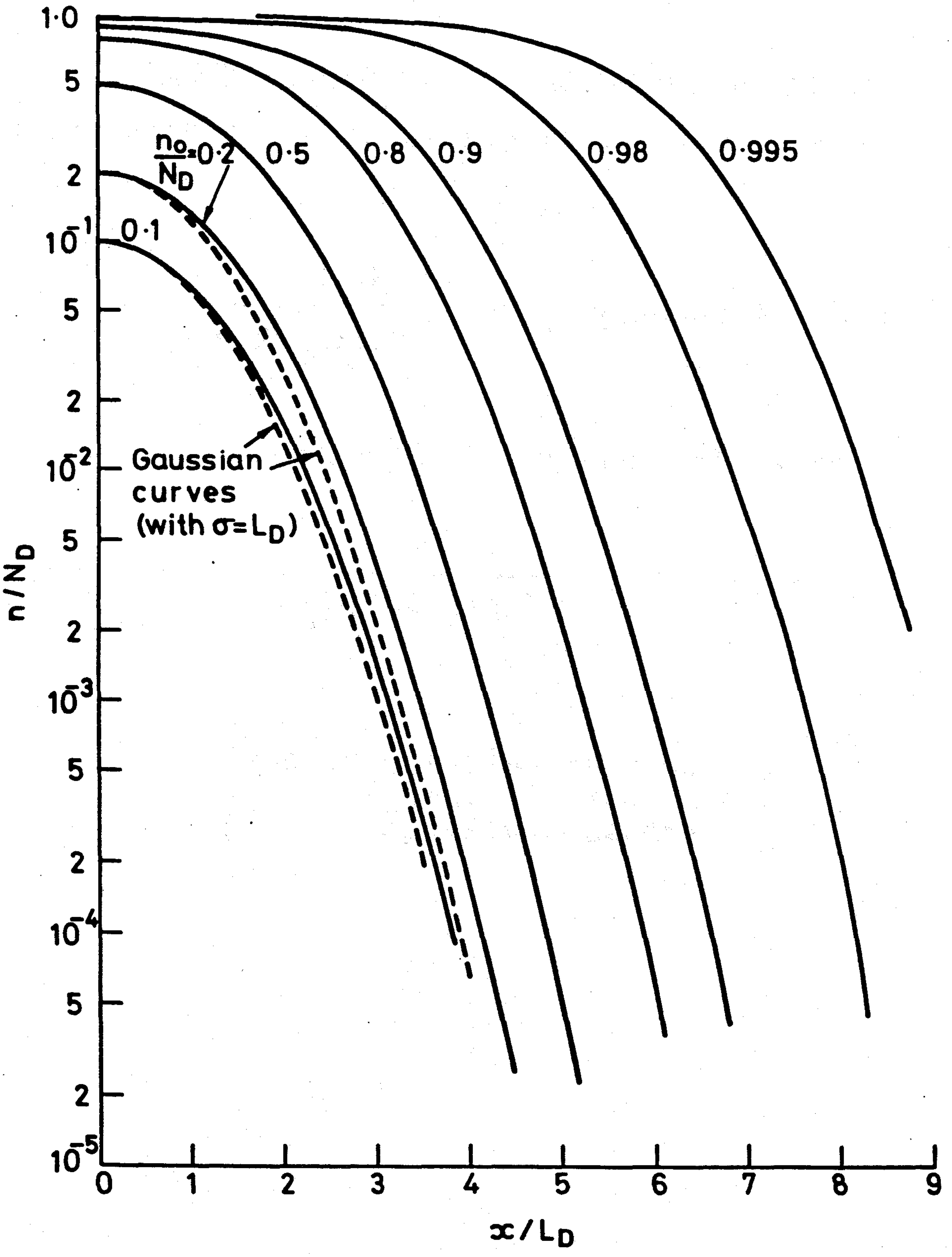
where

$$K = \frac{\sqrt{2mE_o}}{h}$$

n=local carrier density
v=thermal carrier velocity
c=capture cross section of trap
E_t=energy level of trap
k=Boltzmann's constant
T=temperature
N=density of states at band edge
y=depth of trap in oxide
m=electron mass
E_o=oxide barrier height
h=reduced Planck's constant



AERE R11410. FIG. 1. (a) DUAL-REGION MODEL OF A JFET CHANNEL. (b) TYPICAL ELECTRON DENSITY DISTRIBUTIONS ACROSS SECTIONS AA, BB AND CC OF AN n-CHANNEL DEVICE.



AERE R11410. FIG. 4. EXACT 1D ELECTRON DENSITY PROFILES FOR VARIOUS MID-CHANNEL DENSITIES (n_o).

GATE REFERRED NOISE DUE TO SINGLE BULK TRAP

Maximum value assuming trap at drain pinchoff point

Corner frequency $f_c = \dfrac{N v_s c}{\exp(E_t / kT)}$

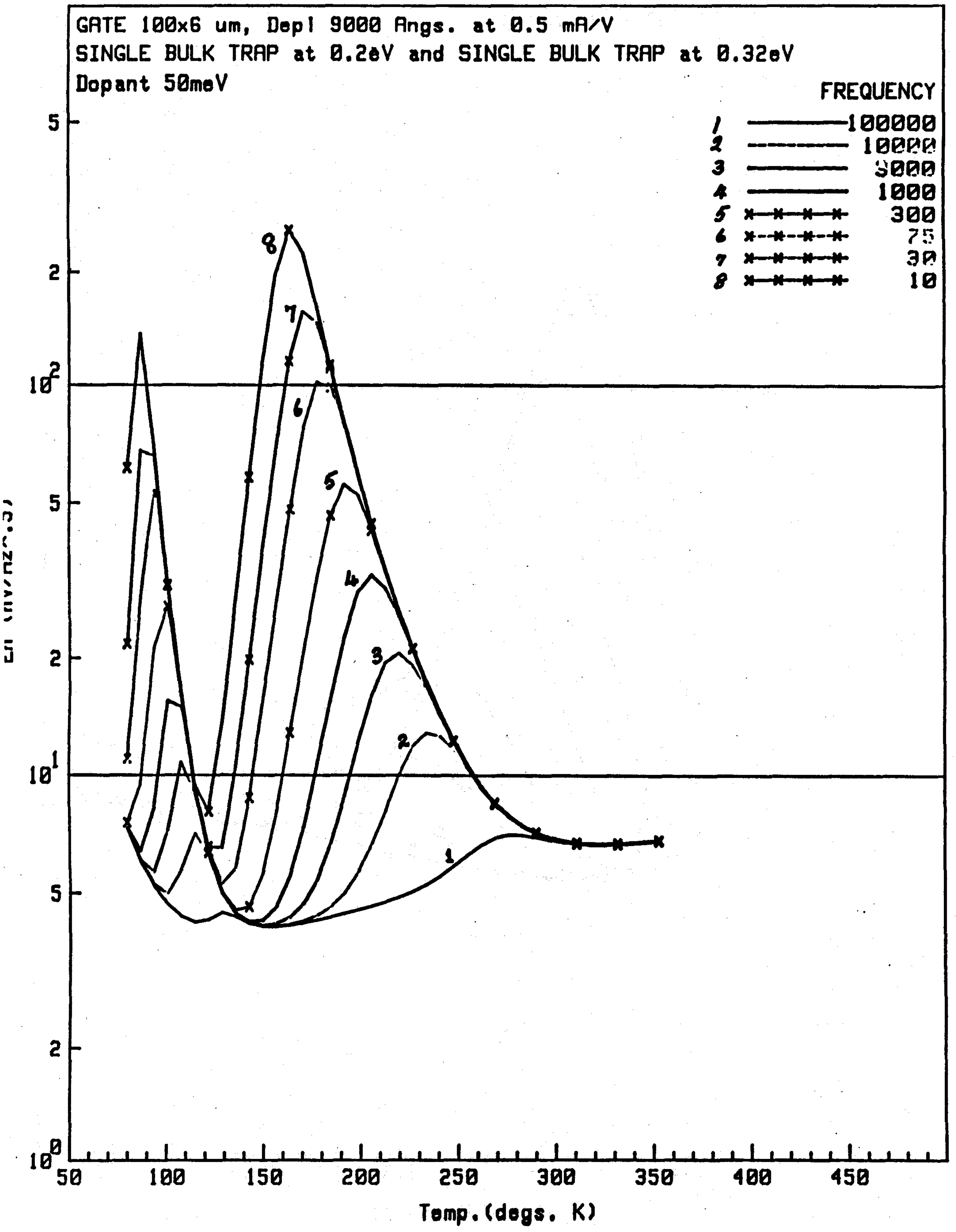
Noise at frequency f is given by

$$E_n^2 = \frac{q^2 v_s^2 f_c}{2L^2 \pi (f_c^2 + f^2) g_m^2}$$

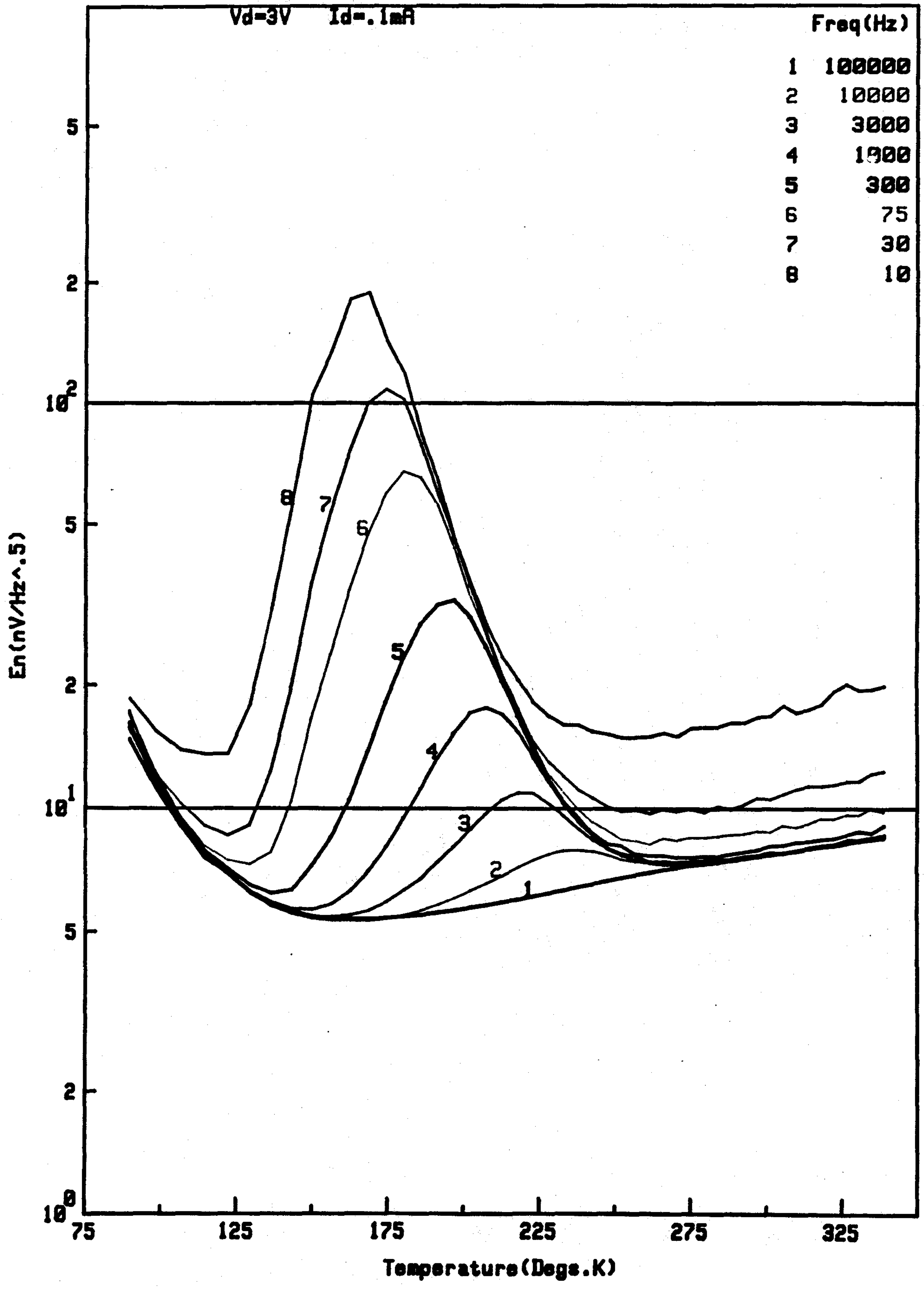
where

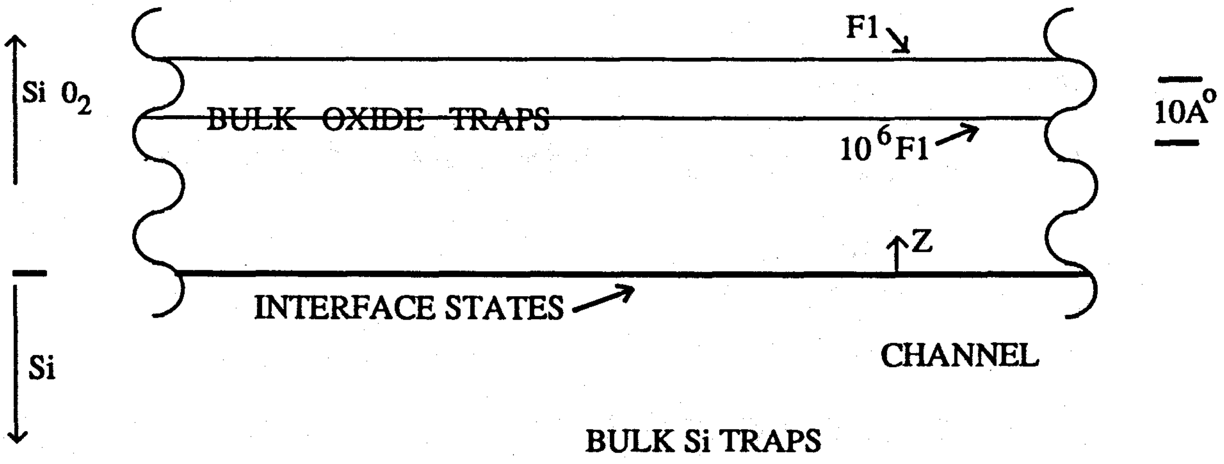
v_s = carrier velocity at drain
q = electronic charge
g_m = transconductance

IMULATED NOISE: NORMAL JFET; NO OXIDE TRAPS



CHARACTERISTICS OF NOISE GENERATED BY A SINGLE TRAP IN JFET VX5165A





ACTIVE TRAPS IN A MOSFET

GATE REFERRED NOISE DUE TO OXIDE TRAPS

MOSFET in strong inversion

Noise at frequency f is given by

$$E = \frac{N_t q^2}{24KWLc_{ox}^2 f}$$

where

N_t = volumetric oxide trap density

$$K = \frac{(2mE_0)}{h}$$

m = electron mass

E_0 = oxide barrier height

h = reduced Planck's constant

W = gate width

L = gate length

c = oxide capacitance per unit area

GATE REFERRED NOISE DUE TO OXIDE TRAPS

Ideal depletion mode MOSFET

Corner frequency $f_c = \dfrac{N v_s c}{\exp(E_g/2kT)}$

Noise at frequency f is given by

$$E_n^2 = \frac{4N_{ss}\, kTq f_c}{6\pi W L c_{ox}^2 (f_c^2 + f^2)}$$

where

N_{ss} =areal interface state density

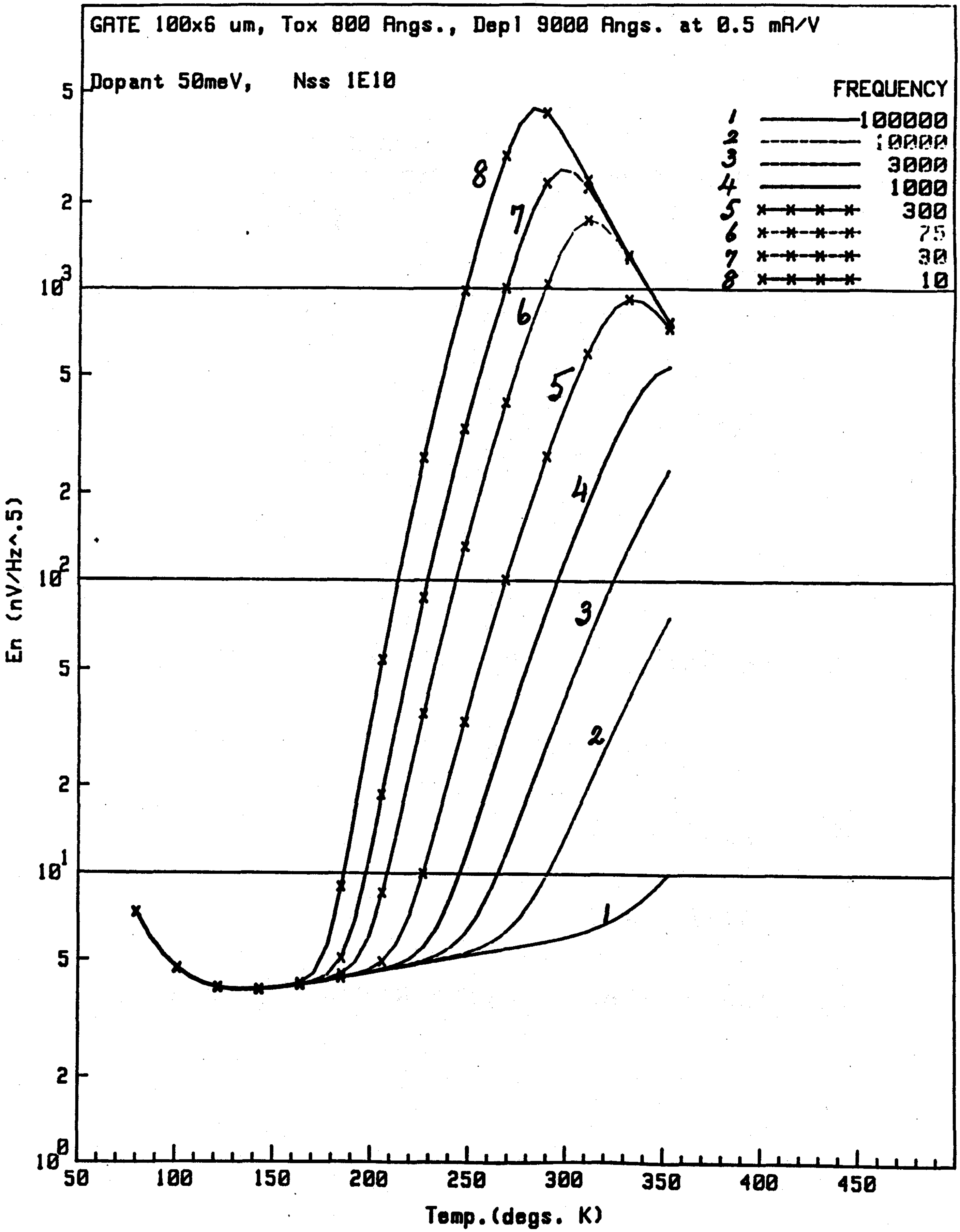
E_g =silicon bandgap

W =gate width

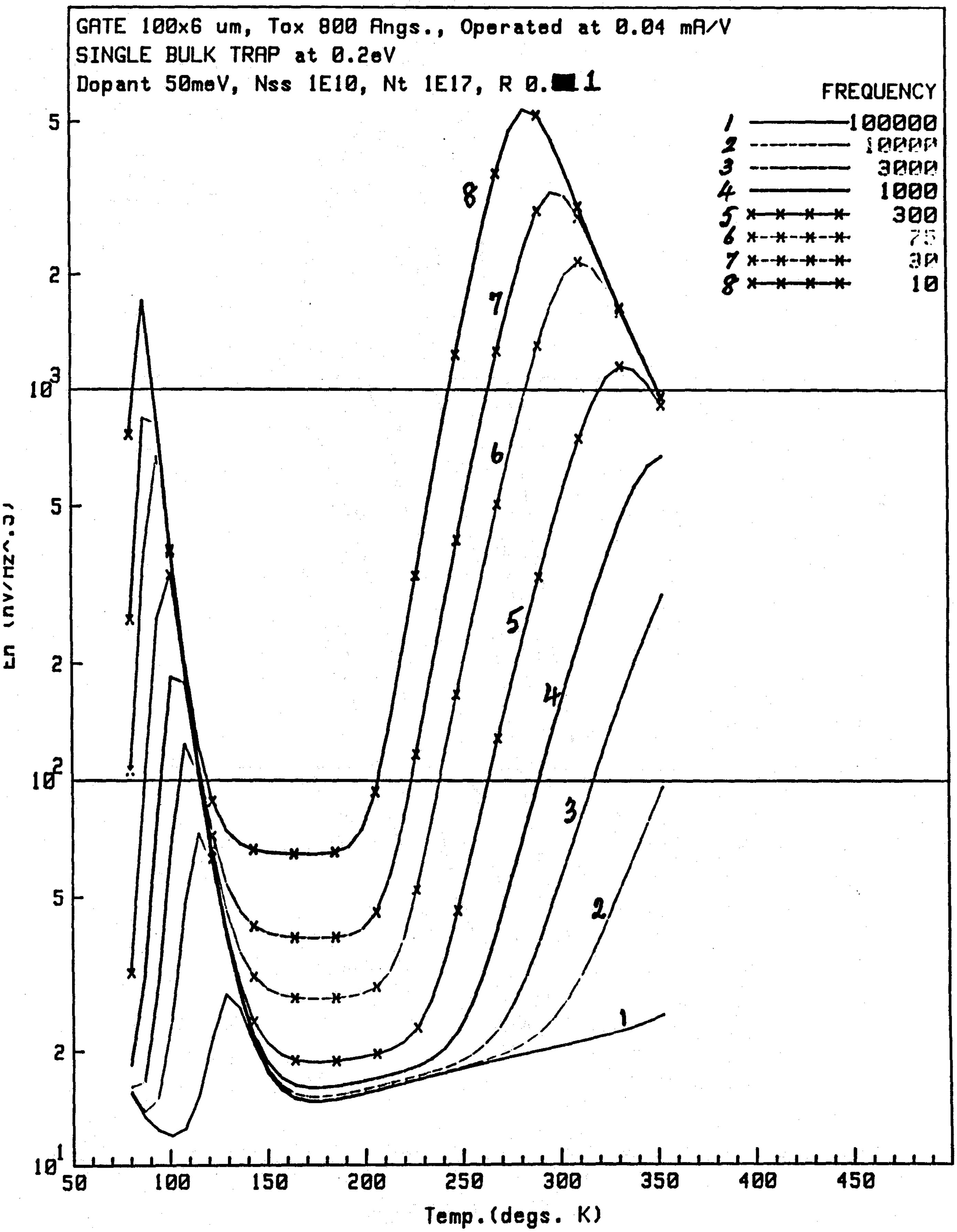
L =gate length

c_{ox} =oxide capacitance per unit area

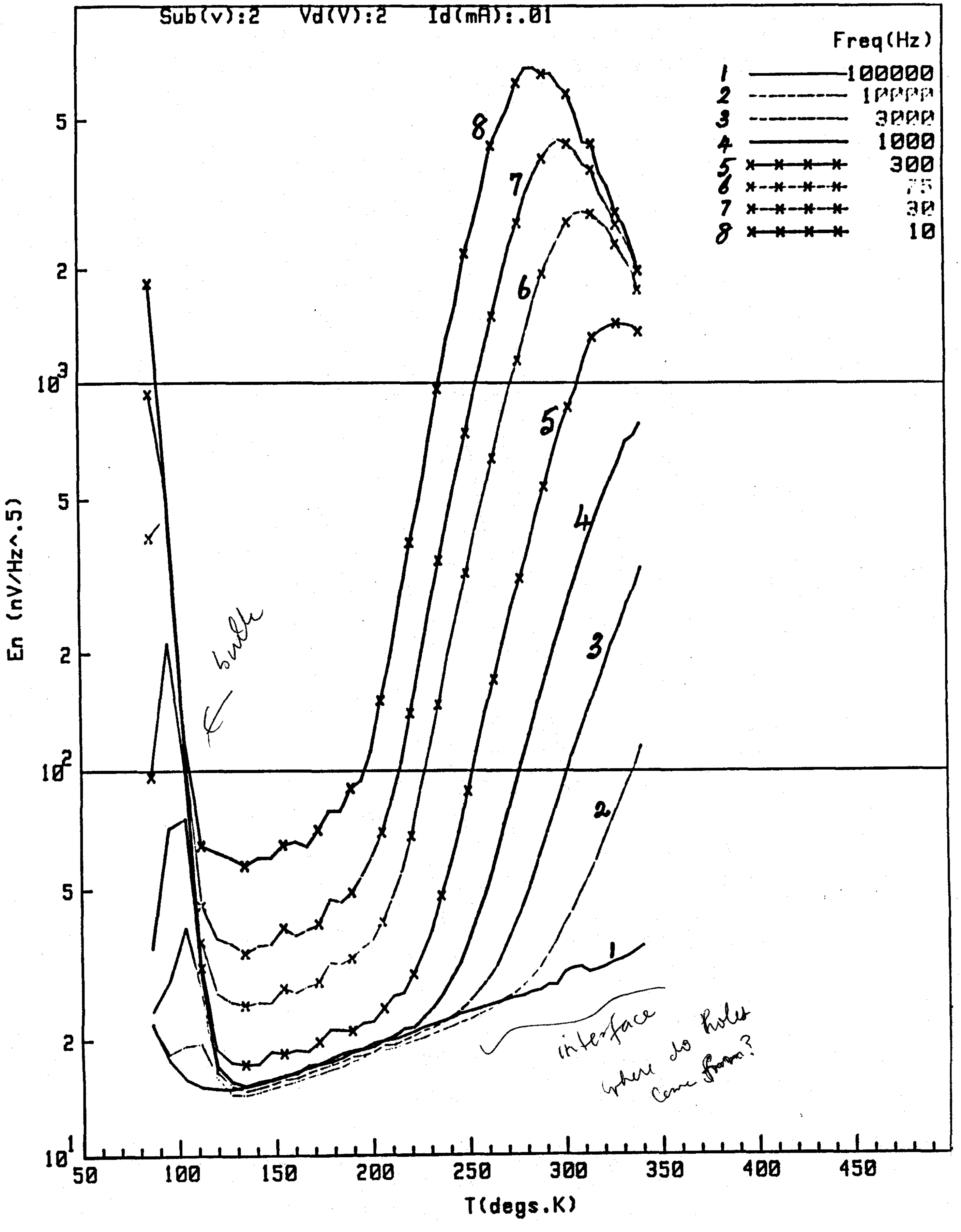
SIMULATED NOISE: DEPLETION MODE MOSFET,CCD PROCESS; NO BULK TRAPS or 1/f NOI



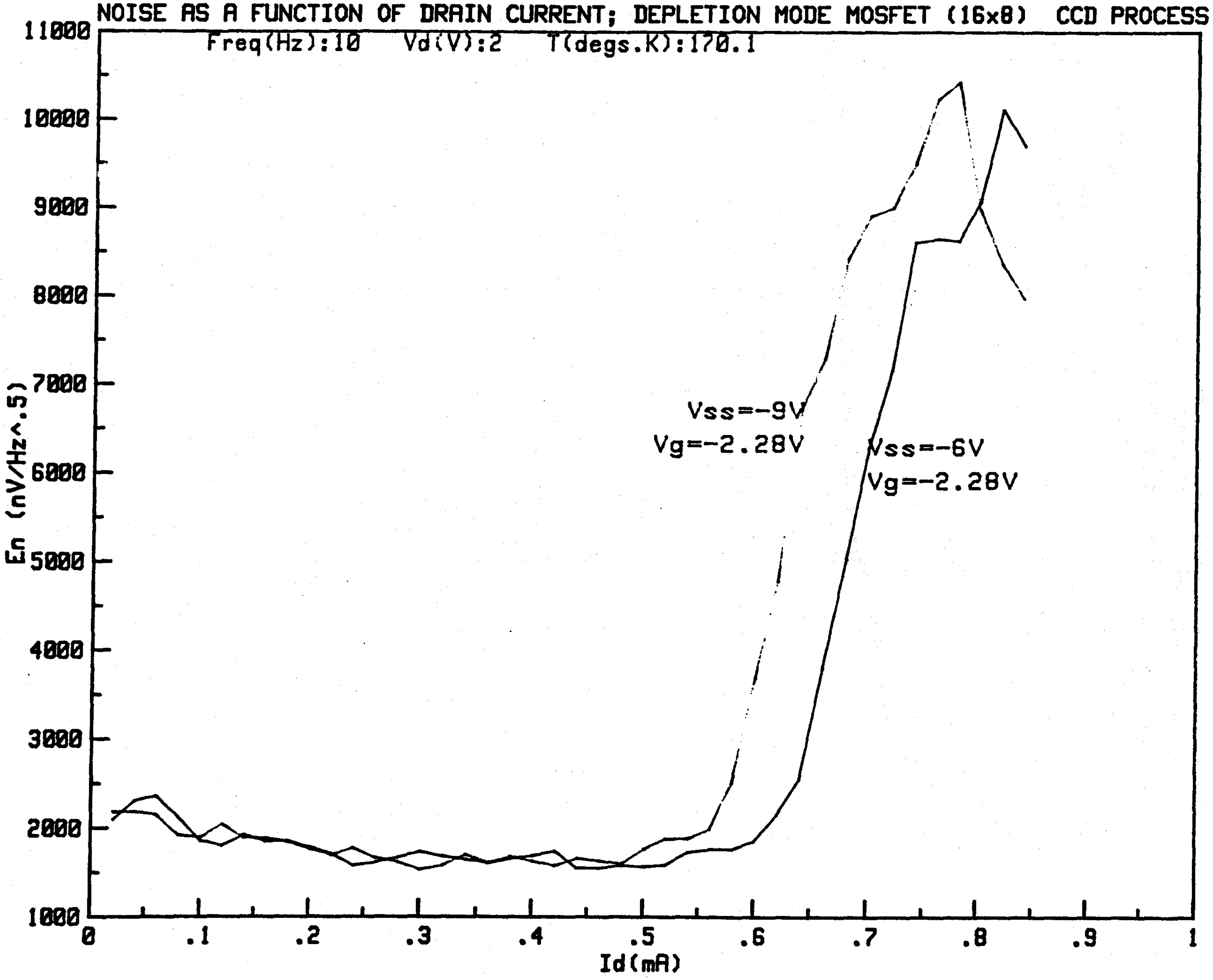
IMULATED NOISE: DEPLETION MODE MOSFET, EFFICIENT HOLE COLLECTION; 1 BULK TRAF



MEASURED NOISE: DEPLETION MODE MOSFET;GATE 100x6 um



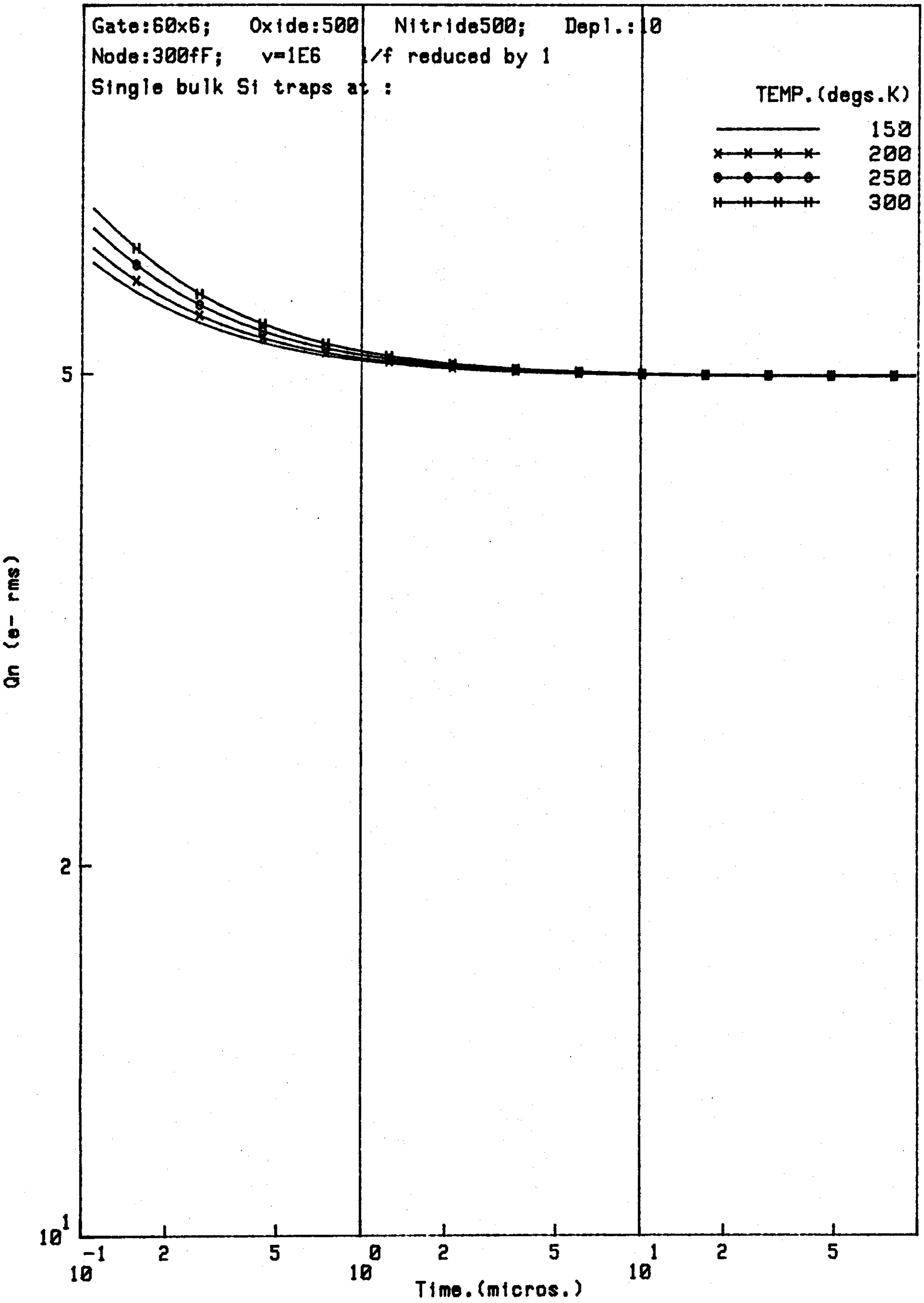
UT103-11 -T27 16×8



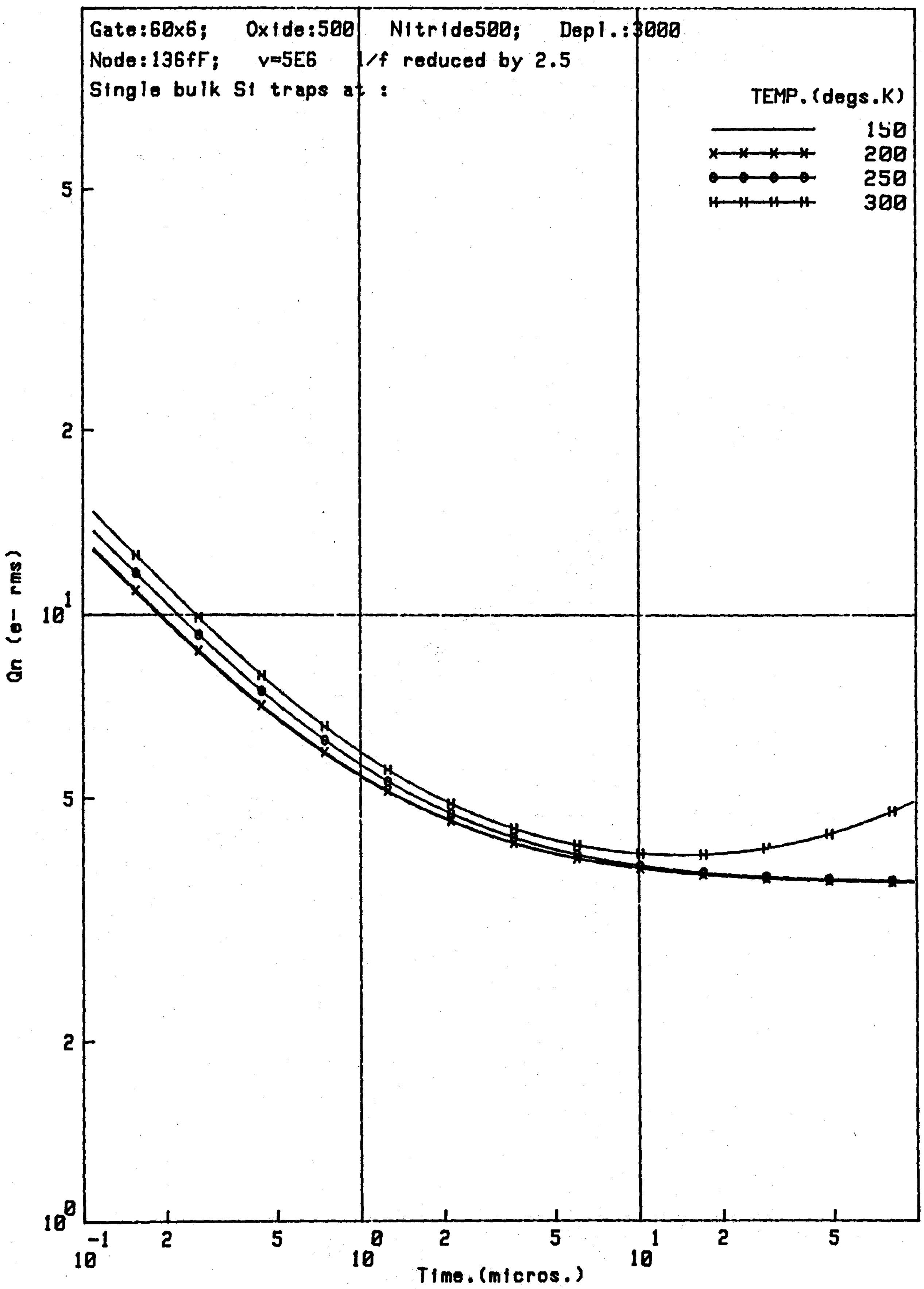
NOISE AS A FUNCTION OF DRAIN CURRENT; DEPLETION MODE MOSFET (16x8) CCD PROCESS

Freq(Hz):10 Vd(V):2 T(degs.K):170.1

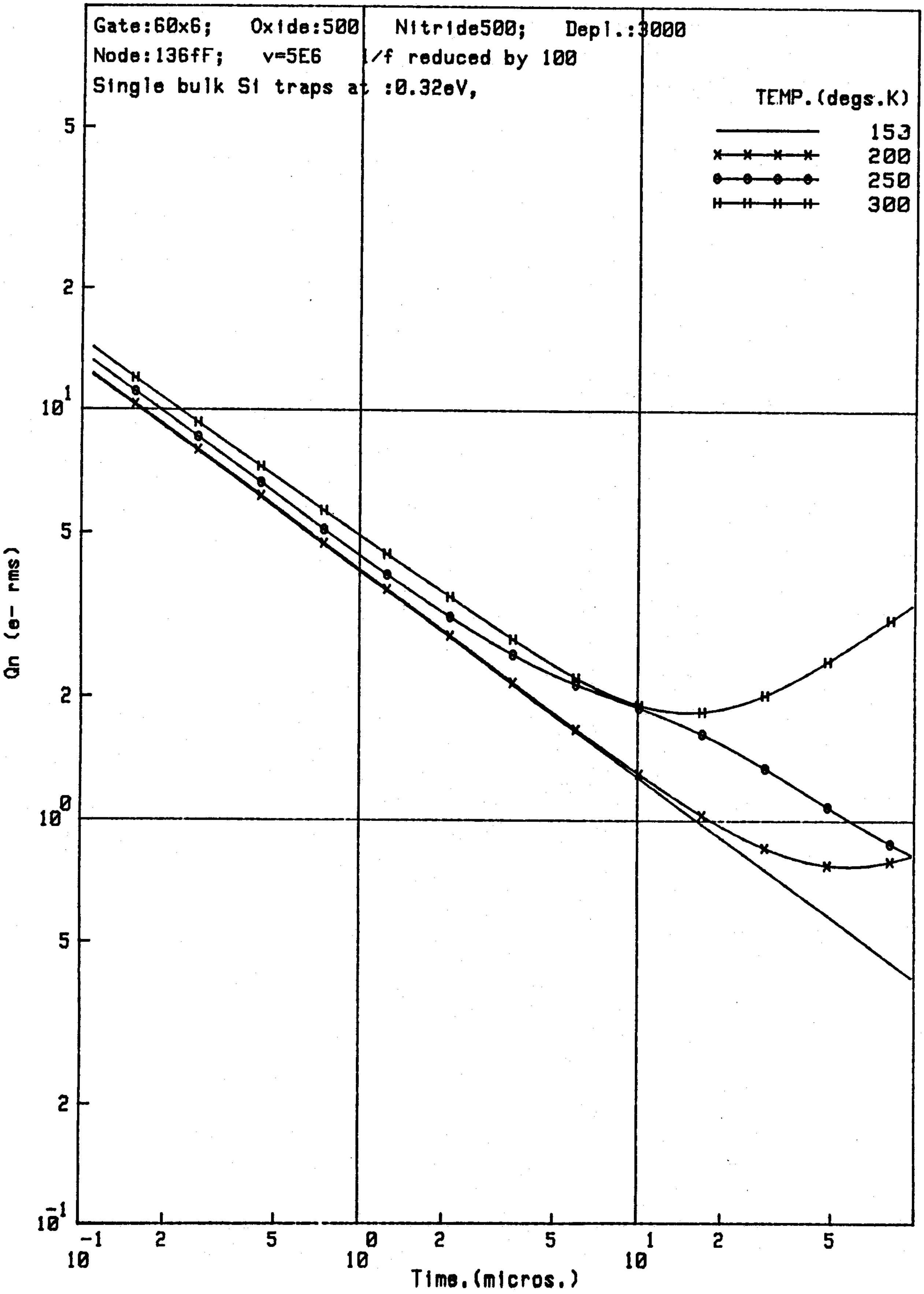
INVERSION MODE MOSFET ; Node Cap. = 2*Cgs

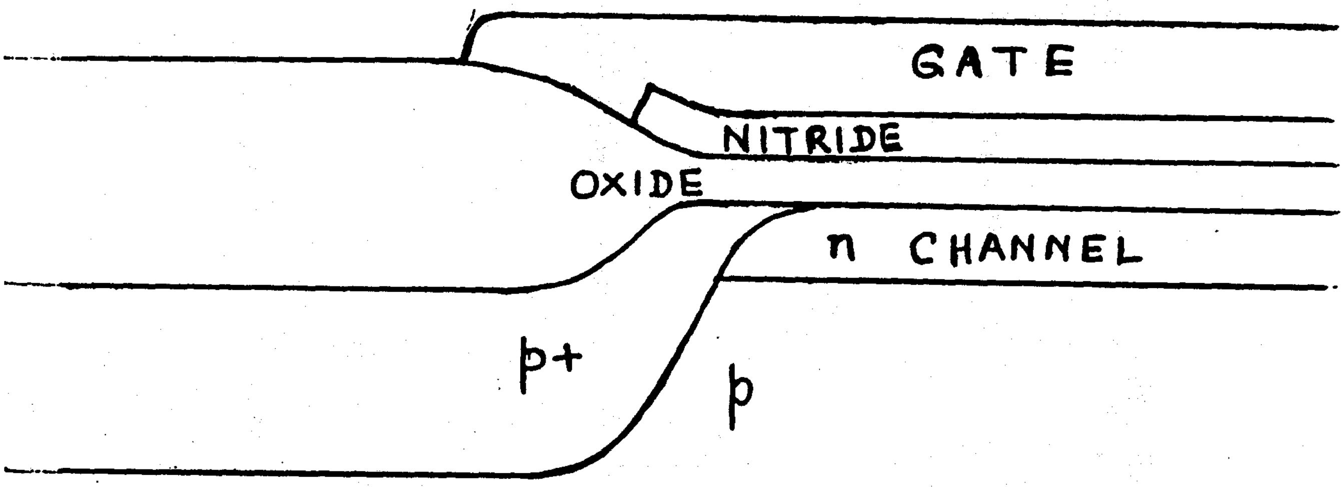


UNIT A1 ;   Node Cap. = 2*Cgs

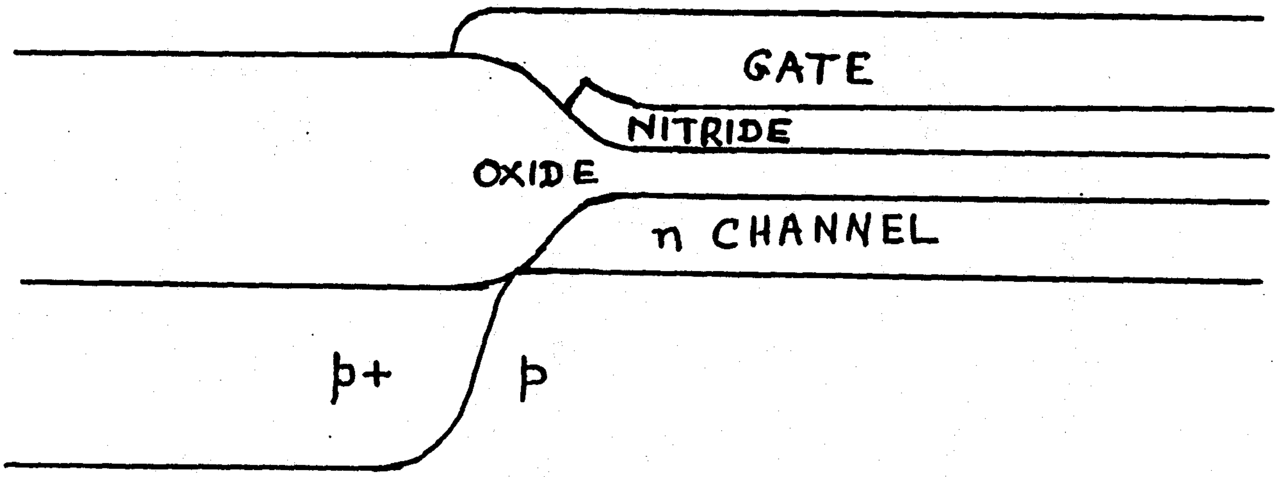


*UNIT A1 ;   Node Cap. = 2*Cgs





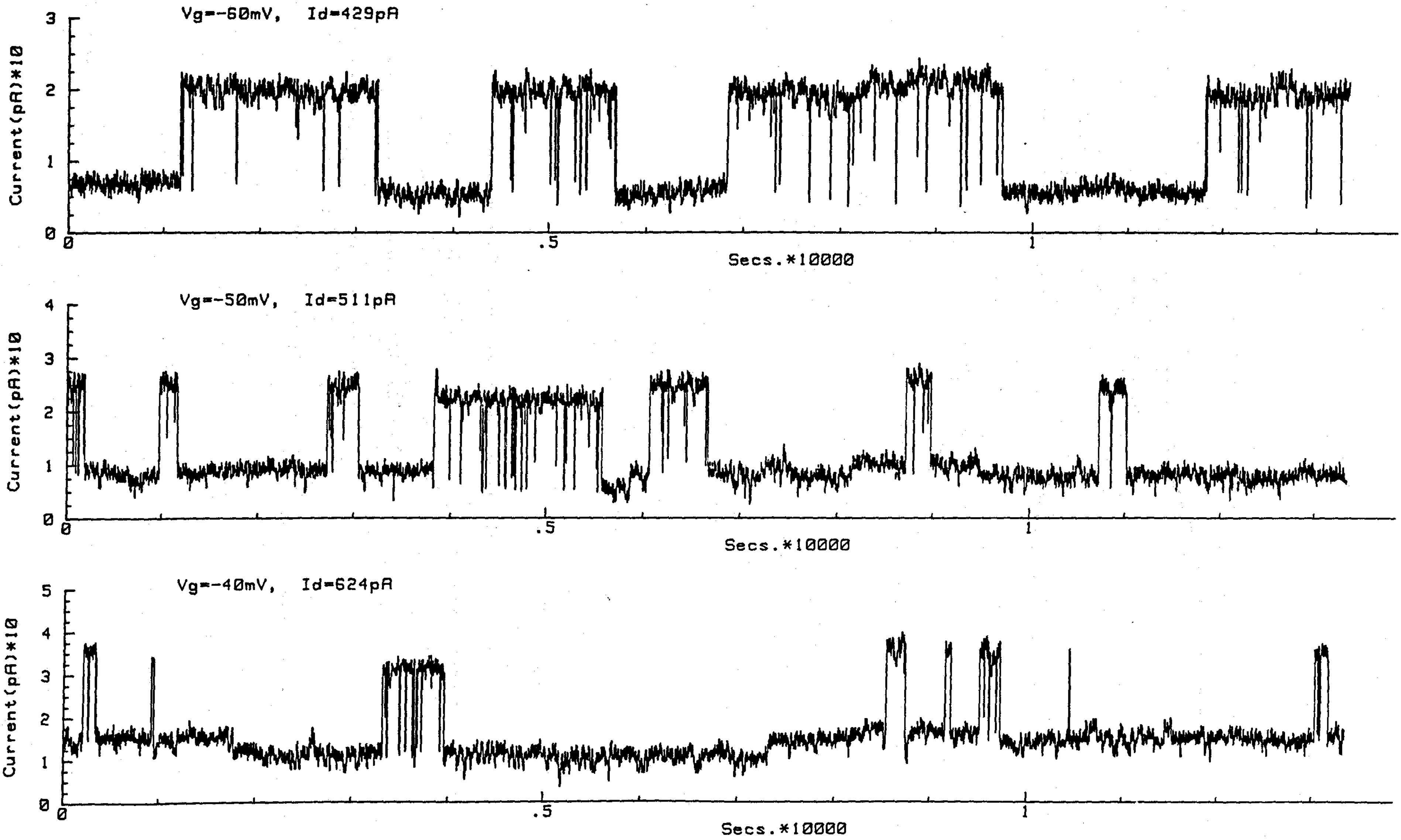
NEAR IDEAL



NOT IDEAL

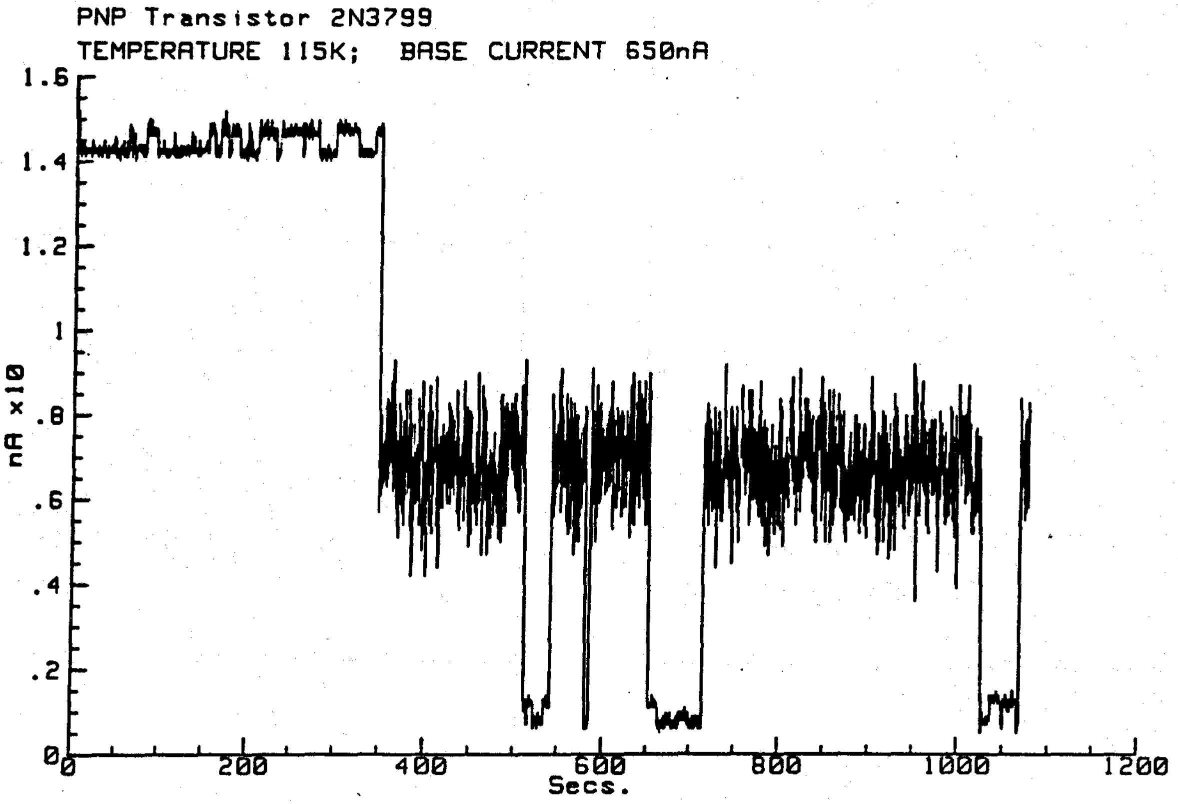
MOSFET-LOCOS ISOLATION

1.5x1.5um NMOS; Vs=-20mV, Vd=0V, Vss=+.2V, T=236.8K (WAVFRMS 023.1)

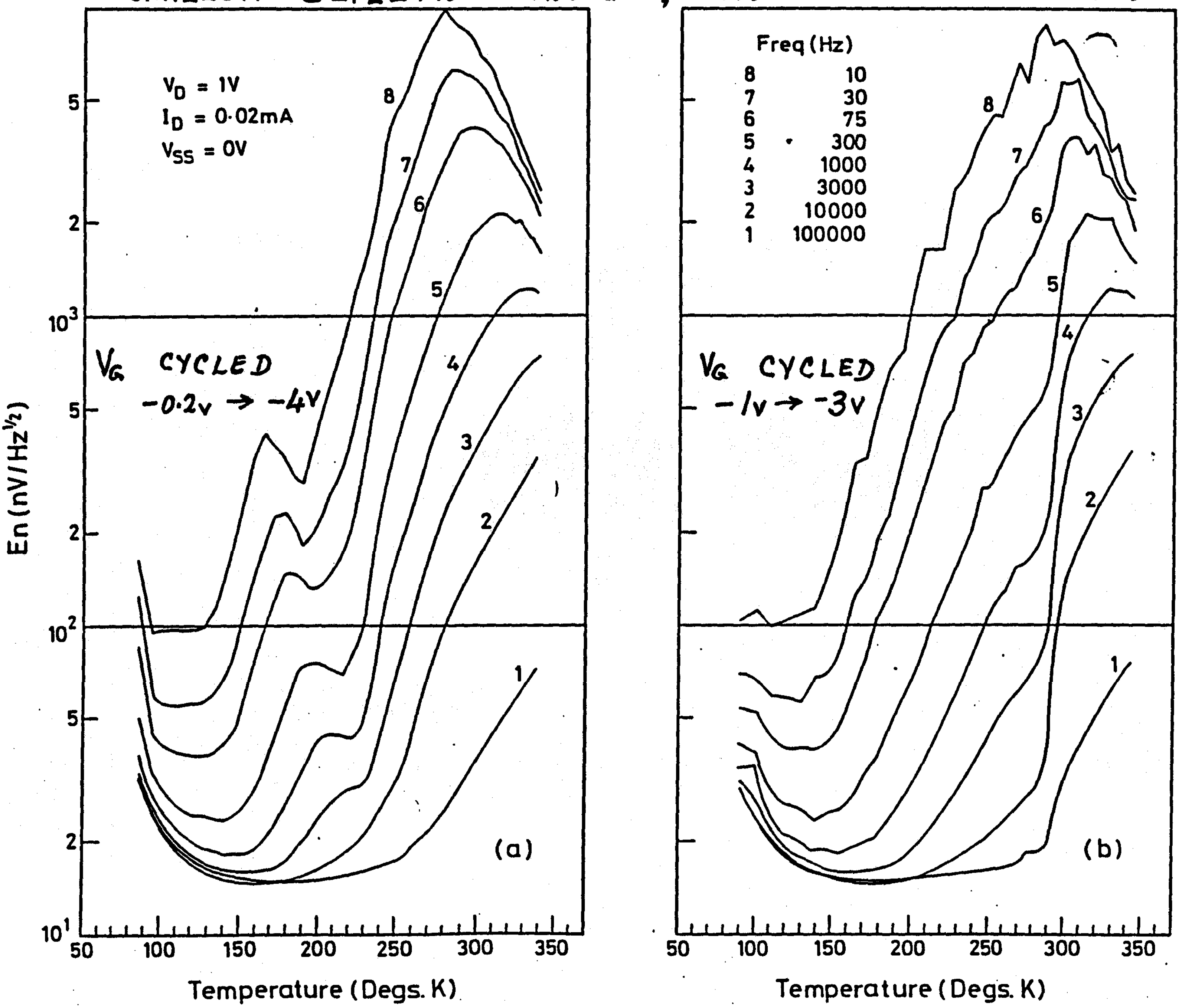

Vg=-60mV, Id=429pA

Vg=-50mV, Id=511pA

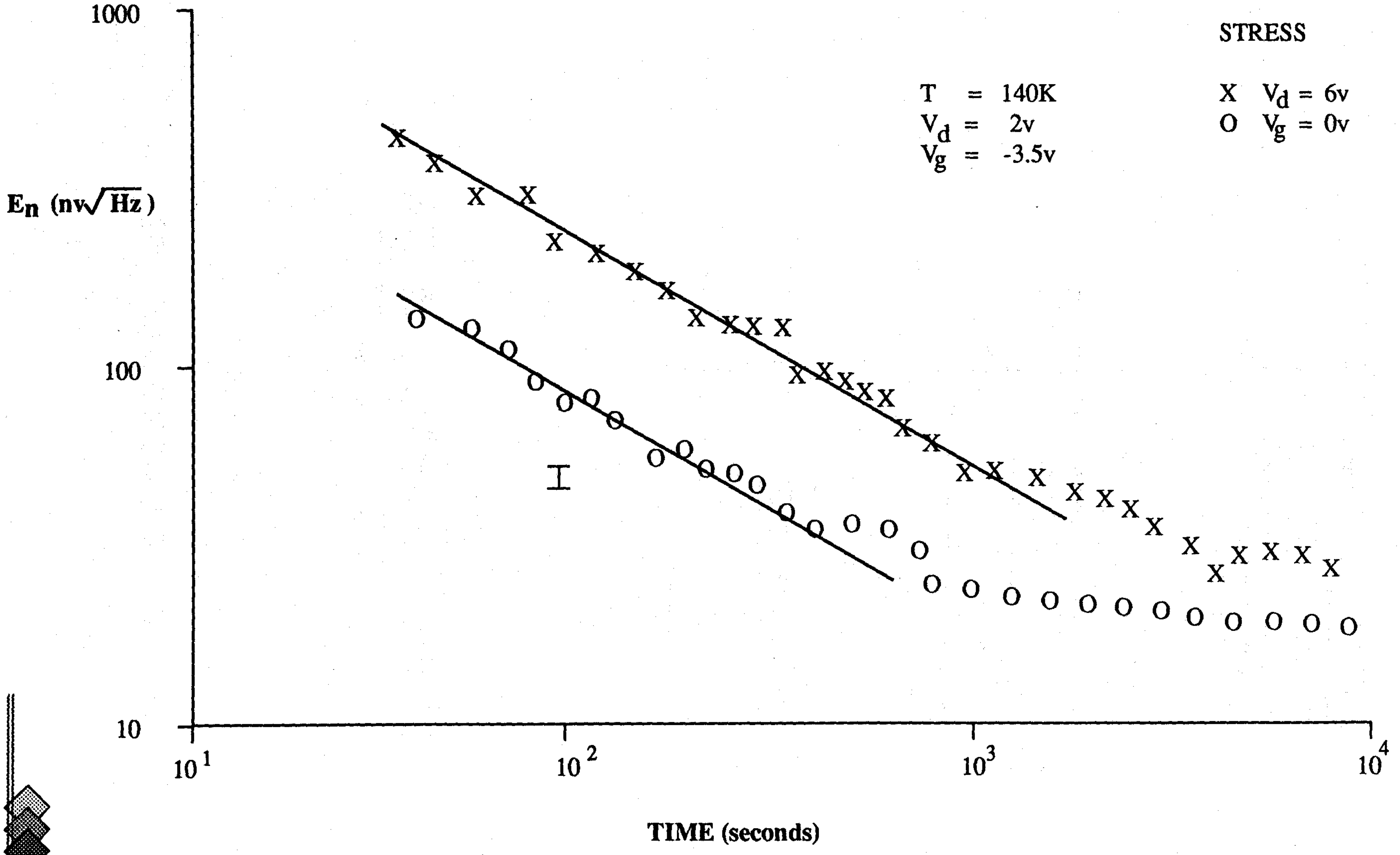
Vg=-40mV, Id=624pA

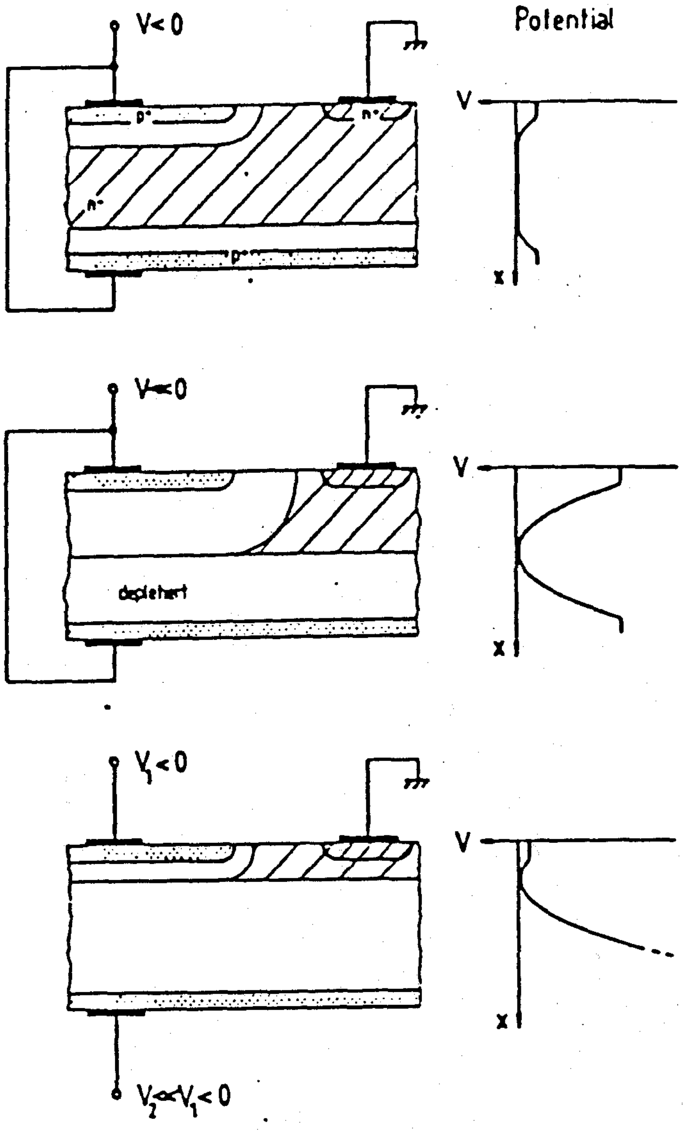

PNP Transistor 2N3799
TEMPERATURE 115K; BASE CURRENT 650nA
nA x10
1.6
1.4
1.2
1
.8
.6
.4
.2
0
0
200
400
600
800
1000
1200
Secs.

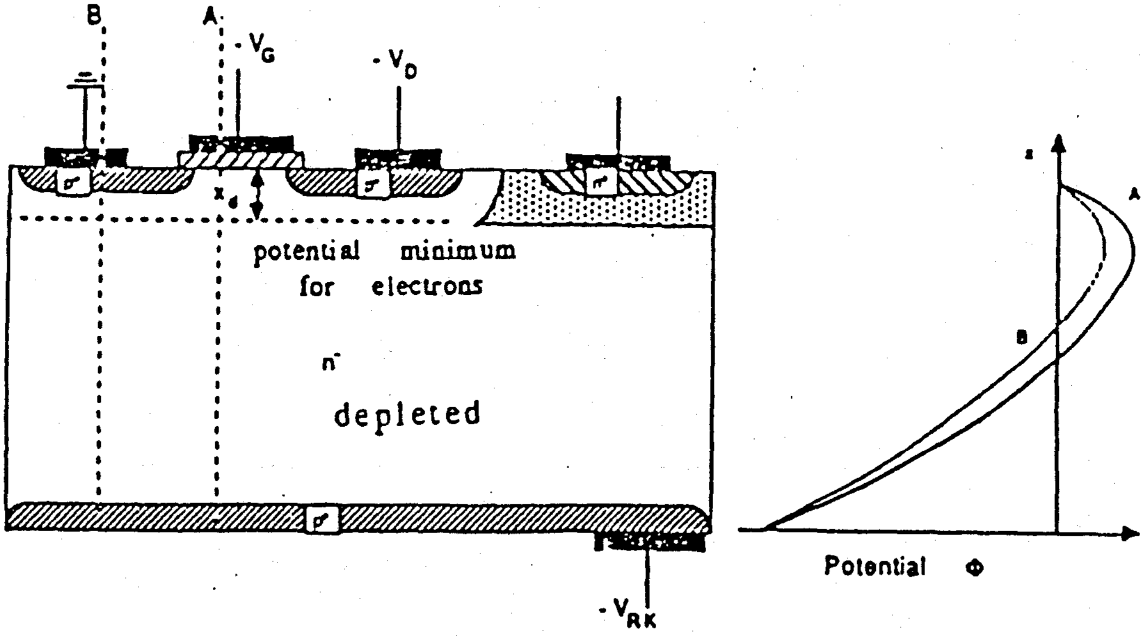
SHALLOW DEPLETION MOSFET; AGING AND ANNEALING



NOISE AT 10 Hz OF DEPLETION MODE MOSFET AFTER STRESS




Potential
V<0
p+
n+
n-
p+
V
x
V<<0
depleted
V
x
V1<0
V
x
V2<<V1<0


B
A
- VG
- VD
p+
p+
p+
n+
xd
potential minimum
for electrons
n-
depleted
p+
- VRK
z
A
B
Potential Φ

THERMAL NOISE ($\bar{e}$ rms)

CDFET

$$\bar{N}^2 = \frac{2\,kT\,WL^2 C_{gso}}{t_p v\; q^2}$$

FET + CHARGE SENSING ELECTRODE

$$\bar{N}^2 = \frac{2\,kT\,C^2}{W\,C_{gso}\;t_p v\; q^2}$$

(a) FLOATING DIFFUSION

$$C = WLC_{gso} + Co$$

(b) FLOATING GATE

$$C = \frac{C_g\,(WLC_{gso} + C_o) + C_d\,(WLC_{gso} + C_o + C_g)}{C_g}$$

k = Boltzmann's constant
T = Temperature
W,L = Gate width, lenth
C_{gso} = Gate to channel capacitance per unit area
v = Carrier velocity at drain
q = Electronic charge
C_o = Total capacitance added to gate of FET
C_g = Capacitance between charge and floating gate
C_d = Capacitance between charge and all other electrodes
t_p = Signal processing time