A 512-STAGE ANALOG-BINARY PROGRAMMABLE TRANSVERSAL FILTER[Δ]

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ABSTRACT

Characterization of a new, 512 stage CCD correlator is reported. The device is a programmable, analog-binary correlator, i.e., it stores binary reference codes and compares them to signals which are essentially analog in character. Performance of the new device (designated TC1235) is compared to that of an earlier design (TC1221, a 128 stage correlator).

The results presented summarize measurements on many samples of each device type. The measurements attest to the improved operational utility of the new device. Of particular note are the expanded on-chip support circuitry and the improved floating gate tap structure which solves the code-dependent bias problem.

I. INTRODUCTION

This paper describes the continuing development of the programmable CCD analog-binary correlator,[1,2,3,4] an important class of devices expected to have broad utility in spread spectrum communications and radar systems.[5] The results presented here indicate that the CCD correlator is reaching a state of maturity in design and implementation. The 512-stage correlator described here (TC1235) is superior to earlier designs in several important respects including: 1) a solution of the code-dependent-bias problem, 2) reduced power dissipation per stage, 3) improved dynamic range, 4) voltage averaging rather than current summing, which simplifies the off-chip differential amplifier requirement, and 5) fewer biases and generally simpler device operation. These advantages of the TC1235 are highlighted by comparison of this device with its predecessor, the 128 stage correlator TC1221.

II. DEVICE ARCHITECTURE

The basic architecture of both programmable CCD correlators is discussed in Ref. 1 and a detailed description of the 512 stage device is given in Ref. 2. A description of the basic correlation circuits is summarized here, and a representative block diagram appears in Fig. 1.

The circuits and their functions are as follows:

1) Program Register: A binary, serial-in/parallel-out shift register through which the binary reference code is loaded. Both correlators employ dynamic, two phase registers.

2) Binary Latches: Flip-flops constituting a static memory where the reference code is stored. The latches may be activated in groups. For the TC1235 it is possible to correlate 64-, 128-, and 256-bit codes in addition to 512-bit codes.

3) Isolation Switches: Transmission gates connecting the program register to the binary latches. They control the parallel shift of data from the program register to the binary latches and thus permit the introduction of a new reference code into the program register while the correlator is still acting on the code previously stored.

4) Routing Switches: Two FET's per CCD stage which steer the output of a given tap to the appropriate summing bus. The switches are controlled by the reference code stored in the binary latches.

5) Tap Source Followers: FET source followers which convert charge-induced voltage fluctuations at the CCD floating gate to signals which are routed to the summation buses. For the new, 512-stage device each source follower FET works with an active load to produce a voltage signal that is coupled, via an enabled routing switch, to one of the summation buses. For the 128 stage device, each source follower has the enabled routing switch as its load, and the floating gate fluctuations are converted to a current contribution to one of the summation buses.

6) CCD Tapped Delay Line: Shallow, buried n-channel, double-polysilicon gate, CCD shift register with one floating gate per CCD stage. The 512 correlator employs uniphase clocking, with barrier implants under the second polysilicon gates and a reset FET attached to each floating gate. The 128 correlator employs two phase clocking, with no barrier implant and a coupling capacitor attached to each floating gate.

In addition to the circuits required for comparison of input signals to reference codes, the analog-binary correlators contain many on-chip support circuits which simplify the interface between the correlator and the surrounding system.

The TC1235 contains circuits to operate the CCD register and circuits to control the entry of the reference code into the binary latches. The CCD requires clock logic and a transport clock pre-driver, an input sampling circuit, and a floating gate reset driver. The clock-logic circuit accepts an input from the master oscillator (via a TTL-to-MOS translator), and amplifies it for input to the CCD predriver. It also provides timing pulses for the input sampling circuit. The CCD transport clock predriver further amplifies the waveform to a level sufficient to drive the off-chip buffer. The off-chip buffer provides a transport clock waveform capable of driving the capacitive load of the CCD register gates. The buffer permits a significant reduction in on-chip power dissipation at the cost of a slight increase in off-chip complexity. The floating-gate reset driver controls the FET's which couple the floating gates to the bias bus. (The bias is required to establish the CCD channel

Δ This work was supported in part by Air Force Contract F19628-77-C-0263, "Analog-Binary Programmable Transversal Filter," RADC/ET, Hanscom AFB, MA, F. D. Shepherd and L. D. Skolnik, contract monitors.
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potential profile but must be removed so that the gate will be floating when the signal charge arrives.)

The input sampling circuit controls the low-noise fill-and-spill inputting of the signal charge into the CCD register. It generates the input sampling pulse (strobe) in synchronism with the CCD register transport clock.

To control the entry of the reference code into the binary latches the 512 correlator also contains a program register clock driver, load logic, and load logic drivers. These circuits accept TTL level signals, via TTL-to-MOS translators, and generate the signals necessary to serially shift and load the reference code. A photomicrograph of the TC1235 appears in Fig. 2.

The 128 stage device also contains a considerable degree of on-chip support circuitry, including CCD clock drivers, CCD input sampling circuit, and program register drivers. A photomicrograph of the TC1221 appears in Fig. 3.

III. ADVANTAGES OF THE 512 STAGE CORRELATOR DESIGN

The earlier process (TC1221) was a buried channel CCD/non-self-aligned NMOS process without provision for a barrier implant. The TC1235 was fabricated by a buried channel CCD/self-aligned NMOS process with barrier implants. The latter enables clocking with a minimum of bias potentials for the CCD gates. In addition, the self-aligned NMOS process inherently provides a significant decrease in parasitic FET gate capacitance.

The use of uniphase clocking combined with a new tap structure[6,7] has proved to be a major design improvement. The new tap structure and clocking scheme provide lower power dissipation, greater output linearity, and perhaps most importantly, a solution to the code-dependent bias problem.

The code dependent bias problem manifests itself as a correlator output baseline offset which changes as the balance of ones and zeroes in the reference code is changed. This effect exists in any correlator in which the signals to be summed are superimposed on DC offsets. An imbalance in the total offset components on the sum buses occurs whenever the code is unbalanced, i.e., the number of ones does not equal the number of zeroes. When the two buses are differenced, the differential offset component may overwhelm the differential signal component. This is the case with the TC1221 correlator, which employs a floating gate capacitively coupled to a large transfer clock. The transfer clock provides tap bias potential as well as charge transfer. In practice, the 128 stage correlator is forced to use balanced codes or accept a sizable reduction in dynamic range. A schematic of the TC1221 tap structure appears in Fig. 4.

The new tapping structure solves the code-dependent bias problem by eliminating the offset bias components. The 512 correlator is designed in such a way that all taps provide the same bias component, which is averaged, not summed, onto the summation buses. Thus, an imbalance in the number of ones and zeroes in the reference causes no change in the averaged bias potential appearing on the summation buses. The TC1235 tap circuitry is shown in Fig. 5.

An additional benefit of the new tapping and summing circuitry is reduced sensitivity to device nonuniformity. In the 128 stage device the DC offset (bias) is much larger than the maximum signal amplitude. Consequently, nonuniformities can produce differences in the DC offset which are of the same order of magnitude as the signals themselves. The elimination of the offsets clearly minimizes the deleterious effects of device nonuniformity.

The final advantage of the new tapping and summing scheme is its inherent voltage output. Both the summing buses are voltage lines, which need to be differentially added to provide the correlation signal. The output impedance of each line is approximately 40 Ω. Thus, widely available devices such as the μA733 and SE/NE592 may be employed to achieve the differential output. This type of voltage output is much easier to process than the current output of the earlier device.

IV. DEVICE OPERATING CHARACTERISTICS

The operating characteristics of the TC1221 and the TC1235 are given in Table 1. All the measurements were done at a 10 MHz CCD clock rate.

The input dynamic range is defined as the ratio of the maximum peak-to-peak CCD input signal to the minimum input signal. The maximum signal being defined as the point beyond which gain compression appears in the correlation output. The minimum signal is the point where the output correlation signal-plus-noise is equal to twice the noise.

The output dynamic range is currently limited by clock feedthrough, rather than fixed pattern noise or other noise sources. The output dynamic range is defined as the ratio of the maximum correlation peak amplitude to the peak-to-peak CCD clock feedthrough. The signal to noise ratio is defined as the ratio of the correlation peak amplitude to the peak-to-peak temporal noise on a single sample.

The charge transfer inefficiency is measured at the output of the CCD register at the floating diffusion amplifier. The $n\epsilon$ product is determined from a square wave CCD input signal, sampled at a 10 MHz rate. The transfer loss per transfer is deduced from the difference in amplitude between the first "one" and subsequent " "ones".

The autocorrelation responses are for aperiodic maximal length sequences. An additional bit is added to the 511 or 127 bit sequences to arrive at 512 or 128 bit codes. Photographs of the autocorrelation response for the correlators are given in Figs. 6 and 7. For these photographs the code was loaded into the program registers at a 5 MHz clock rate and correlated at a 10 MHz CCD clock rate.

The performance of the TC1235 with respect to code dependent bias is demonstrated in Fig. 8. The autocorrelation response of the TC1235 for different codes may be compared to that of the TC1221. For each device, no adjustment was made after the initial optimization for the square-wave response (10 MHz). It may be seen that the TC1221 displays the code-dependent base line shift when the code is changed from the square wave (Fig. 8a) to a PRN sequence (Fig. 8b). By contrast, the TC1235 performance (Fig. 8c) shows essentially no code-dependent base line change as the autocorrelation response changes with the code change (256-bit square wave, 32-bit square wave, 512-bit PRN code).

The power dissipation of the correlators is summarized in Table 2. The TC1221 data are for 5 MHz program register operation and 10 MHz CCD operation with both registers continuously operating. The total measured dissipation is approximately 1.2 watts. The estimated power dissipation for the TC1235 is based on circuit simulation results for 5 MHz program register operation and 10 MHz CCD operation, again for the case of

TABLE 1. CORRELATOR PERFORMANCE SUMMARY

Parameter	TC1221	TC1235
Number of Points Correlated	128, 64, 32, 16	512, 256, 128, 64
CCD Clock Rate	10 MHz	10 MHz
Reference Code Load Rate	5 MHz	8 MHz
Input Dynamic Range	35 dB	37 dB
Output Dynamic Range	32 dB	34 dB
Linearity (Ratio of Fundamental to 2nd, 3rd Harmonics)	>40 dB	>40 dB
Signal to Noise	>60 dB	>60 dB
Charge Transfer Inefficiency	0.8×10^{-4}	1.6×10^{-4}
Autocorrelation Peak-to-Sidelobe Ratio	20.1 dB*	25.4 dB**

* 128 bit sequence, theoretical value is 21.3 dB.
** 512 bit sequence, theoretical value is 26.5 dB.

TABLE 2. POWER DISSIPATION

Device Section	TC1221* 128 Stage Correlator (mw)	TC1235** 512 Stage Correlator (mw)
Program Register	125	219
Program Register Driver	204	190
CCD Register Drivers	238	538
Binary Latches	348	250
Tap Structure	215	502
CCD Output Amplifier	61	53
Load Logic Drivers	---	362
	1,191	2,114

* Measured
** Simulation

continuous operation of all circuitry. The total estimated power dissipation is 2.1 watts. The total power dissipation (measured without separating the power supplies for sectional detail) was 1.96 watts, in good agreement with the simulation.

A semi-quantitative estimate of thermal performance was made by means of a thermocouple attached to the case near the pellet mounting location. The TC1221 is packaged in a 48 pin dual-in-line ceramic package with silver epoxy mounting. The TC1235 is packaged in a 64 pin dual-in-line Kyocera ceramic package, again employing silver epoxy mounting. The TC1221 when dissipating nominally 1 watt in an ambient temperature of 23°C reaches a case temperature of 36°C with a small fan directing air flow over the package. When the fan is removed, the case temperature rises to 46°C at thermal equilibrium after several hours. At this elevated temperature (with no bias readjustment) the autocorrelation peak amplitude drops to about 90% of its lower temperature value. When the device is heated to a case temperature of 55°C (by a heat gun) the correlation peak is lost completely. While a complete analysis has not been done, it is believed that degradation of on-chip driver performance causes the loss of performance and that the basic correlation circuits are capable of operating at considerably higher temperatures.

The thermal performance of the TC1235 is significantly better. When dissipating nominally 2 watts in an ambient of 23°C, the 512 correlator reaches a case temperature of 39°C with a small fan cooling the package. When the fan is removed the case temperature rises to 50°C upon acquiring thermal equilibrium. At the elevated temperature, the unadjusted correlation peak amplitude drops to about 95% of its initial, lower temperature value. Further heating to raise the case temperature to 69°C reduces the peak to 80%.

The reported performance of the TC1235 is poorer than expected because of two design defects. These defects cause the high level uniphase transfer clock to be coupled more strongly than anticipated onto the summation buses. The first defect is an inadequate substrate contact, which allows substrate modulation by the uniphase clock. The second defect is a larger than expected overlap capacitance between the second polysilicon transfer clock gate and the first polysilicon floating gate. Both defects are being corrected.

The excess clock coupling to the floating gates impairs device performance in several ways. First, modulation of the floating gate by the transfer clock results in modulation of the charge storage well depth. This effect causes reduced charge capacity and reduced transfer efficiency. Second, the excess overlap capacitance increases the total capacitance at the floating gate node, thereby reducing its sensitivity to signal charge packets. Finally, a larger clock feedthrough signal is fed to the summation buses and the off-chip video differential amplifier.

The reduced charge capacity and transfer efficiency, reduced charge sensitivity, and increased common-mode signal all result in a reduced dynamic range. It is an indication of the ultimate performance capability of the TC1235, that, in spite of the excess clock coupling, an input dynamic range of 37 dB has been measured.

The performance limitations caused by clock feedthrough will be remedied by a minor mask change and special treatment of the wafer back surface. The mask change entails a decrease in the second polysilicon CCD transfer gates in order to reduce overlap capacitance. The back surface treatment involves removal of the N+ layer (which occurs naturally in this process) and replacing it with an annealed P+ layer and chrome-gold metallization. The back surface treatment has been attempted, and it has resulted in improved ohmic contact to the substrate.

V. FUTURE WORK

The success achieved thus far in the development of large analog-binary correlators has shown that the CCD correlator has great potential as an alternative to other correlator technologies (i.e., digital CMOS, SAW devices). In a drive toward increasing the attractiveness of the analog-binary correlator, plans have been made to add additional on-chip circuitry in order to improve the ease of operation of the device. A particularly attractive addition to the correlator would be a CCD automatic input biasing circuit to make the CCD register self-biasing. A preliminary design for this circuit has been completed, and a similar circuit has been demonstrated in other CCDs. Furthermore, automatic tap bias adjustment circuitry may be added so that the tap structure bias current is automatically adjusted to the optimum operating point. Other candidates for inclusion on the chip are summation bus sample and hold circuitry and a differential amplifier. These additions would make the correlator a complete, self-biasing signal processing device.

VI. CONCLUSIONS

The operation of a 512-stage, programmable CCD correlator with on-chip driver circuits has been demonstrated. Peak-to-sidelobe ratio of 25.4 dB (within about 1 dB of the theoretical autocorrelation response) was realized with 10 MHz CCD clocks. Ability to change codes without requiring adjustment of the output was likewise demonstrated. Direction of future efforts leading to improved performance was indicated. Anticipated improvements include reduction of clock feedthrough, with attendant increased dynamic range, and further-simplified operation by means of automatic, on-chip biasing circuits.

ACKNOWLEDGMENT

The authors are grateful to many colleagues: at RCA, to J. I. Pridgen, D. J. Sauer and R. L. Angle for design and processing assistance and design review, to D. S. Kent for assistance in device characterization, to R. A. Geshner for MEBES photomask fabrication, to F. S. Shashoua and R. F. Kenville who encouraged the work; at MIT Lincoln Laboratory, to J. Laynor and R. Bush for discussions on a wide variety of correlator topics. Special thanks are due F. D. Shepherd of RADC/ET for support, encouragement and guidance throughout the development of the TC1235.

The work of S. C. Munroe was done at MIT Lincoln Laboratory, Lexington, MA. This work was sponsored in part by the Department of the Air Force. The views and conclusions contained in this document are those of the contractor and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the United States Government.

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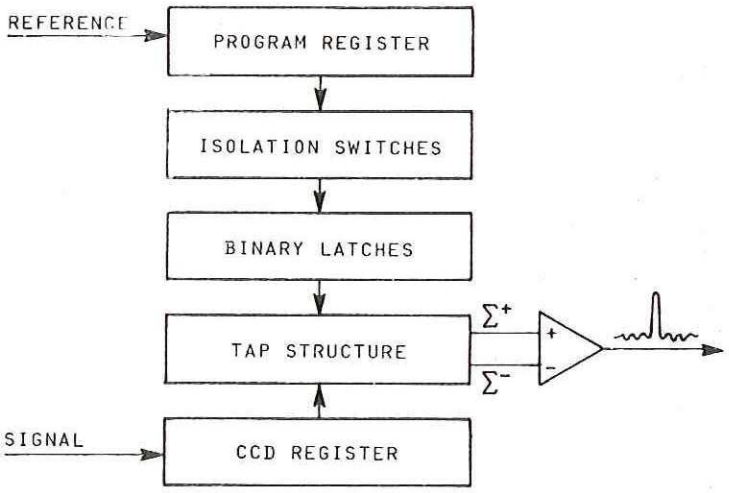


Fig. 1. Basic architecture of programmable, analog-binary CCD correlator. Analog signal in CCD tapped delay line is compared to binary reference entered via program register and stored in latches.

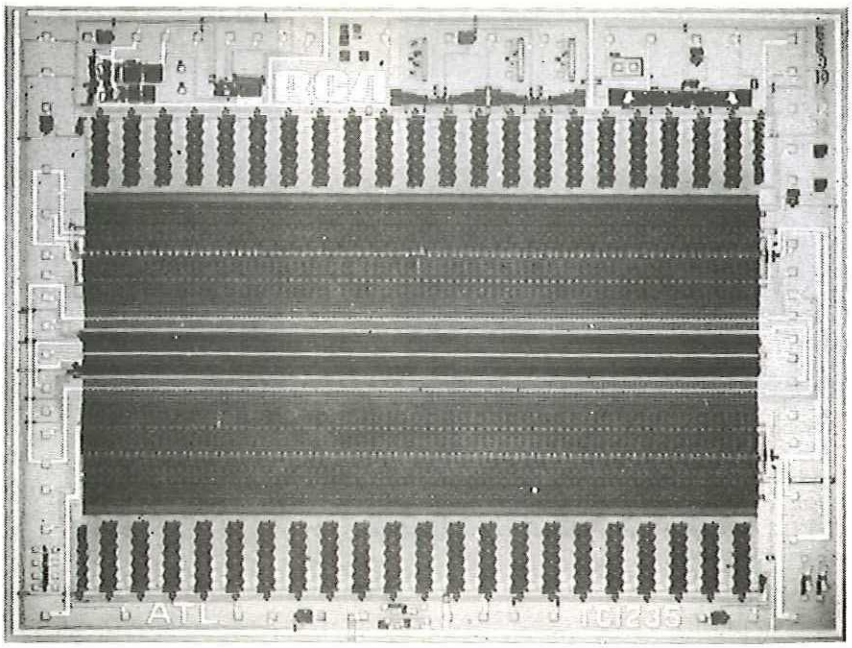


Fig. 2. Photomicrograph of TC1235, a 512-stage correlator with on-chip clock drivers. Chip dimensions are 385 x 290 mils.

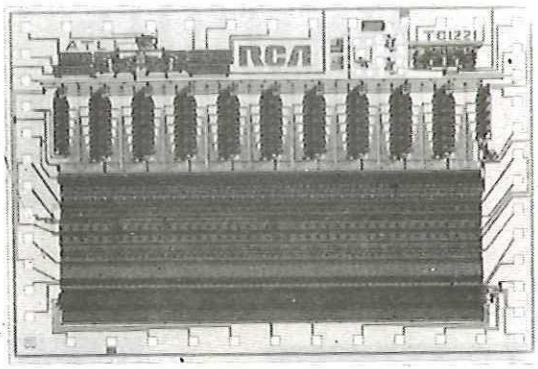


Fig. 3. Photomicrograph of TC1221, a 128-stage correlator with on-chip clock drivers. Chip dimensions are 240 x 160 mils.

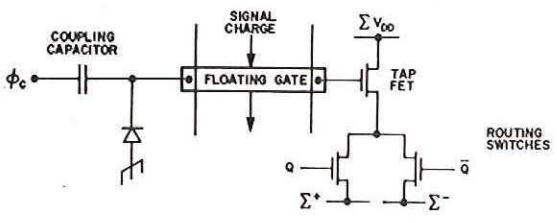


Fig. 4. Tap structure employed in TC1221. Floating gate voltage change is converted to a current change. Routing switches steer tap current to appropriate summation bus. Summation buses sum tap currents.

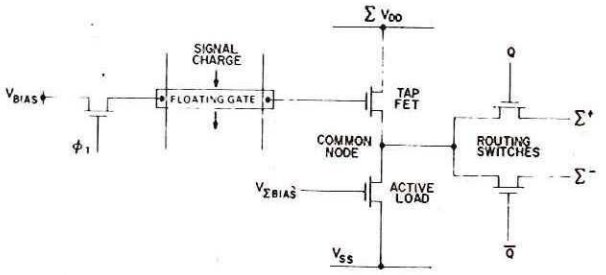


Fig. 5. Tap structure employed in TC1235. Floating gate voltage change causes change in common node voltage. Routing switches couple these changes to appropriate summation bus. Summation buses average tap common node voltages.

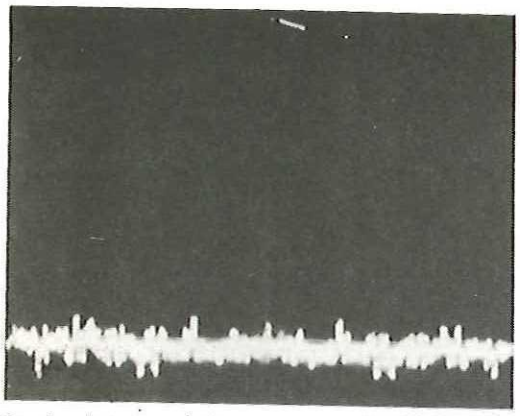


Fig. 6. Autocorrelation response of TC1221 with on-chip CCD clocks at 10 MHz. Input signal is a 128-bit aperiodic maximal length sequence. Peak to sidelobe ratio is 20.1 dB, compared to 21.3 dB theoretical. (Small arrow indicates correlation peak.)

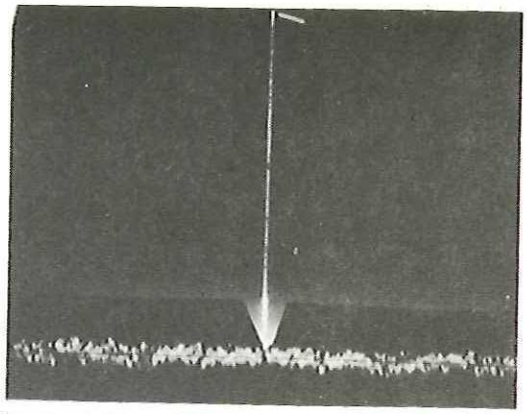
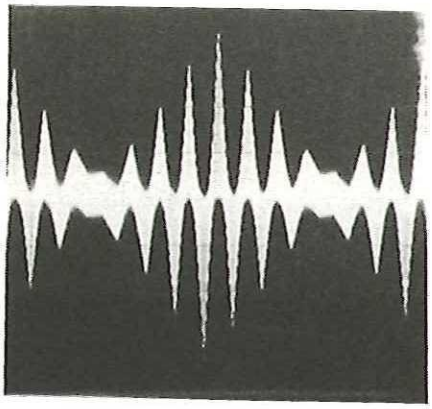
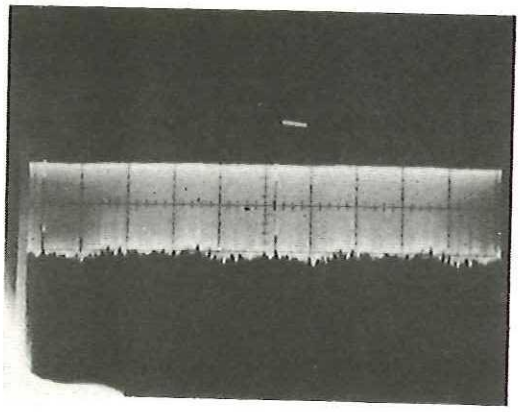


Fig. 7. Autocorrelator response of TC1235 with on-chip CCD clocks at 10 MHz. Input signal is a 512-bit aperiodic maximal length sequence. Peak to sidelobe ratio is 25.4 dB, compared to 26.5 dB theoretical.



a)



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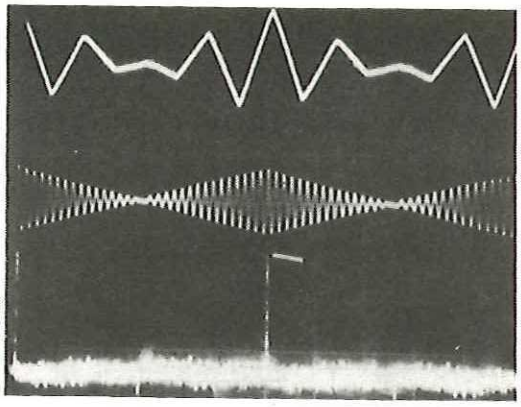

c)

Fig. 8. Code-dependent bias. a) and b) illustrate the effect in TC1221. a) shows square-wave correlation: b) shows PRN sequence correlation with output unadjusted from a). Note large common mode signal on base-line. c) shows response of TC1235 to square waves (top traces) and PRN sequence (bottom trace) with no adjustment of output after code change.