27.4 A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor

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In recent years, cellphone cameras have come to require much more diversification and increased functionalities, due to the strong growth of the smartphone market. In addition to the image quality, speed, and pixel counts that conventional image sensors require, there is high demand for new functions that can respond to various photo-taking scenes. We developed a stacked CMOS image sensor (CIS), composed of conventional back-illuminated (BI) image-sensor technology and 65nm standard logic technology.

Figure 27.4.1 shows the structure of a stacked BI-CIS, and that of a conventional BI-CIS [1-3]. The stacked BI-CIS uses a logic process substrate instead of the supporting substrate of a conventional BI-CIS, and thus forms advanced logic circuits using an exclusive logic process technology that is independent of the CIS process.

The cross-sectional view of the stacked BI-CIS is shown in Fig. 27.4.2. The top half of the chip (top part of figure) is formed with conventional 1P4M BI-CIS process technology; it is laid upside down. The bottom half of the chip (bottom part of figure) is formed with 65nm 1P7M logic process technology. The on-chip color filter and micro-lens are formed on the top surface of the chip, and the photodiode is constituted in the Si (CIS) area. The connection between the interconnect layers of the top and bottom parts is realized by through-silicon vias (TSV), which are a type of vertical via-type contact.

Figure 27.4.3 shows a block diagram of the chip. A pixel array, load transistors, row drivers, and comparators are located in the top part. The signals between the top and bottom parts are connected by TSVs, and the number of TSVs approximately equals the number of row and column signals (this number is in the order of thousands per chip, including power supply and GND wiring). The column TSVs are placed in between comparators and counters, connecting column-signal lines, power supply and GND lines. The row TSVs also become like column TSVs, placed in between row decoders and row drivers, connecting row-signal lines, power supply and GND lines. The circuits for the comparators are composed of high voltage (HV) transistors at 2.7V. These compare the pixel signal and the referenced ramp signals, and the result of this comparison is an output of 1.05V CMOS signal that passes along a TSV and is inputted into the counter. The comparator and counter constitute the digital correlated double-sampling scheme [4,5], thus the variation of parasitic resistance and capacitor of TSVs are compensated, and the TSV has no influence on the image quality. Since the row drivers and load transistors are also composed of HV transistors, the low-voltage transistors, which were included in the conventional CIS process, are excluded from the top part, thereby reducing the number of process steps. In this chip, the circuit configuration is determined in consideration of the device and noise characteristics of each process, as well as to maximize the area efficiency. As a typical example, because generally there is more noise in a logic process than a CIS process, the comparators that are sensitive to noise are located in the top part; this avoids degradation in image quality due to aggravation of 1/f noise or RTS noise, thus maintaining the good image quality of a conventional BI-CIS. On the other hand, the use of a 65nm logic process enables the equivalent of 2400k gates in the bottom part, which are mainly used for the image-processing circuit.

The chip micrograph is shown in Fig. 27.4.7. TSVs are located beside row drivers and comparators, surrounding the pixel array of the top part; they are arranged in the same position in the bottom part. In spite of additional functionalities, the chip size is about 70% that of conventional 1/4-inch BI CMOS image sensors with the equivalent of 500k gates.

There are two new functions on the chip: (1) RGBW coding adds a clear filter to the color filter of the pixel, and realizes higher sensitivity, and (2) binning-SVE [6] for a high-dynamic-range high-definition (HD) movie. The block diagram of an image data-processing block in high-dynamic-range (HDR) mode is shown in Fig. 27.4.4. It switches short exposure and long exposure every two lines, and compares those two perpendicular different-exposure pixels in the synthesize block. It selects one suitable pixel, or blends those two pixels into one single pixel. Thus, the vertical resolution becomes one half, and following that the horizontal resolution is also set to one half by digital processing. As mentioned above, binning-SVE is used for HDR and digital binning. To obtain a 720p movie, the binning-SVE processing is performed in the 3280×1848 picture, which is the maximum 16:9 picture size clipped out from the pixel array, and the picture is processed and reduced to a quarter size (1640×924); it is then further downsized to 1280×720 by a scalar that is not shown in a figure. Moreover, the exposure ratio of short exposure and long exposure is 16× at the maximum, and the output data of the synthesize block is extended to 14b from 10b at the input. After the synthesize block, adaptive tone reproduction (ATR), which is a tone-conversion process optimized for every scene, is performed by the ATR block (14b data is converted to 10b and is forwarded into a Remosaic block). Within the Remosaic block, the high-sensitivity (high SNR) and texture image information of white pixels (clear filter) is transcribed to RGB pixels by the signal-processing block. Since the RGB code level is maintained so that a spectral sensitivity characteristic may not change, it compresses the noise. Moreover, the RGBW coding is changed into Bayer coding, thus post-processing in the conventional ISP is possible.

Figure 27.4.5 shows the comparison of HDR movie pictures; the background sky portion is over-exposed in the long exposure, the portion of the umbrella is under-exposed in the short exposure, but proper exposure is obtained for both portions in the HDR mode.

The rise in temperature of the chip is investigated to confirm the influence it has on image quality, due to stacking the CIS and the logic substrate. The simulation result shows the temperature distribution in pixel area is suppressed to <1°C. Also the local heat generation in the bottom part under the pixel does not spread to the pixel directly or locally, thus there is no degradation in image quality due to stacking.

Characteristics of the 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor are summarized in Fig. 27.4.6. The pixel size is 1.12×1.12μm^2, sensitivity of the white pixel is 6700e$^-$/lx-s and green pixel is 4800e-/lx-s, and a saturation signal of 5000e$^-$ at 60°C is achieved. The dynamic range is 60dB (10b), +24dB with HDR mode. The measured power consumption is typically 200mW in the 720p HDR movie mode.

In conclusion, the stacked BI CMOS image sensor achieves advanced functionality in a compact chip size. The separation of the top part (Pixel) and bottom part (Logic) accelerates the individual evolution of each technology.

Acknowledgements:
The authors would like to thank the members of Sony Semiconductor Corporation, Sony LSI Design Inc. and Sony Corporation for their support of this work.

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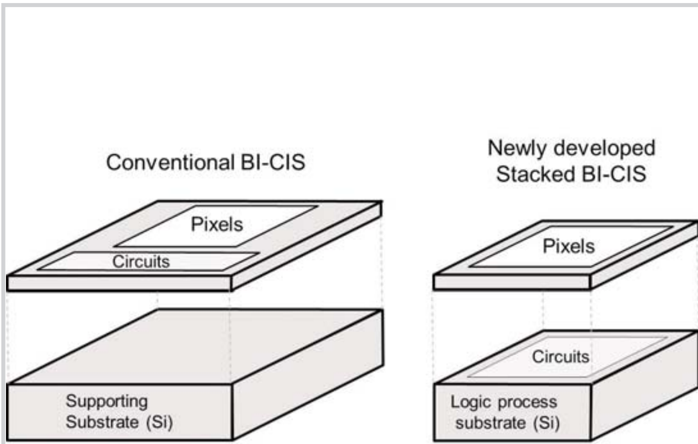

Figure 27.4.1: Structure of stacked CMOS image sensor.

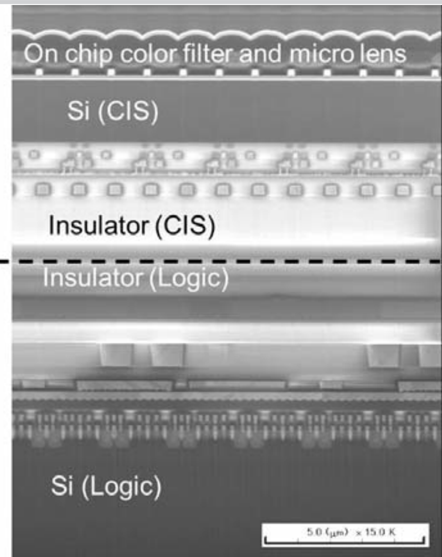

Figure 27.4.2: Sectional view of stacked CMOS image sensor.

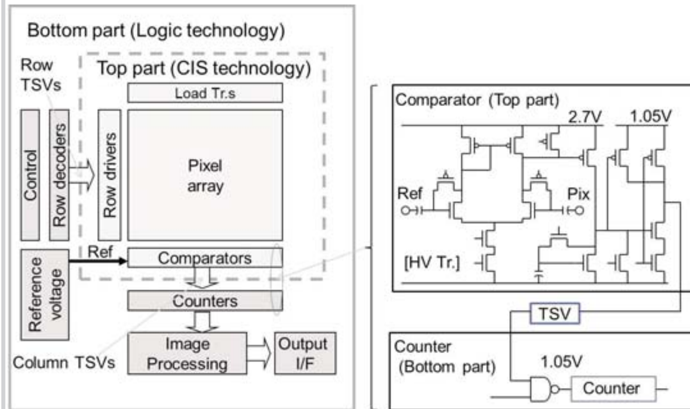

Figure 27.4.3: Block diagram of 8Mpixel stacked CMOS image sensor.

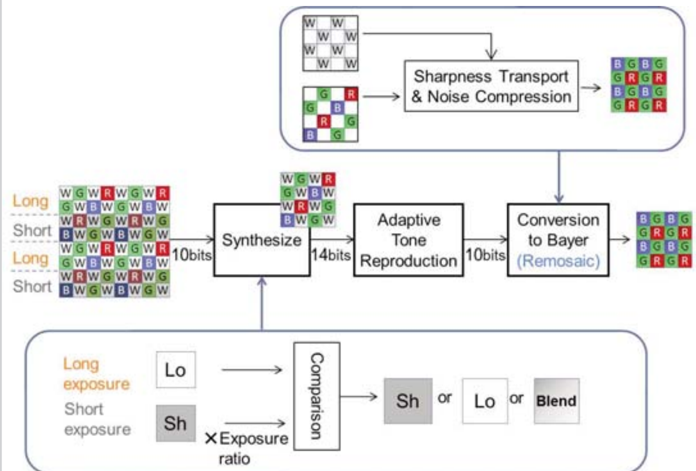

Figure 27.4.4: Block diagram of image-processing block (@HDR mode).

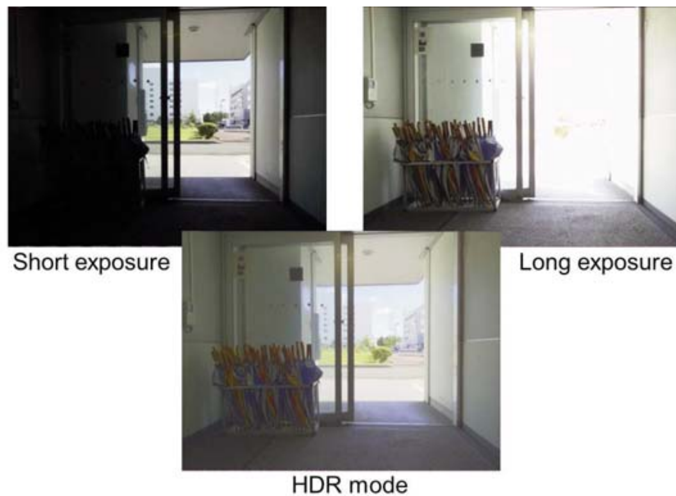

Figure 27.4.5: HDR movie pictures (4:3).

Process		90nm1P4M CIS / 65nm 1P7M Logic Stacked Back Illumination
Number of effective pixels		3280(H) X 2464(V) 8.08M pixels
Image size		Diagonal 4.595mm (Type 1/4)
Pixel size		1.12um(H) X 1.12um(V)
Frame rate	Full	30 fps
	1/2 sub sampling	60 fps
	HD format	1080p 30fps
		720p 30fps (HDR mode)
		720p 60fps
Supply voltages		2.7V / 1.8V / 1.05V
Input clock frequency		6 ~ 27MHz
Image output format		Bayer RAW
Outputs		MIPI (CSI2) [4lane 750Mbps, 2lane 1Gbps]
Saturation Signal		5000e- at 60C
Sensitivity (typical value F5.6)		4800e-/lx-s (Green pixel) 6700e-/lx-s (White pixel) At 3200k light source with IR cut filter of 650nm cut-off
RMS random noise		2.2e- (Analog gain :18dB)
Conversion gain		63.2uV/e-
Dynamic range		60dB (10bits)+ 24dB(HDR mode)
Power consumption		200mW @typ. 720p HDR movie mode 185mW @typ. Full 30fps

Figure 27.4.6: Characteristics of 1/4-inch 8Mpixel stacked BI CIS.

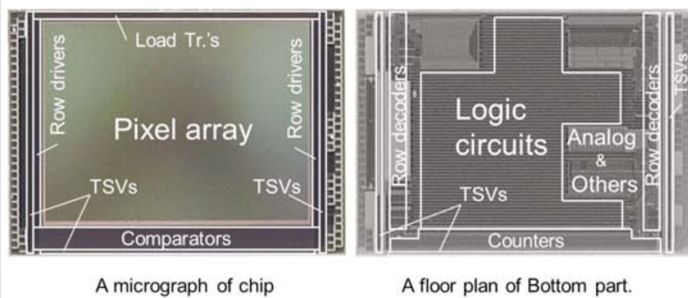

Figure 27.4.7: Micrograph of 1/4 inch 8M pixel stacked BI CIS.

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