22.9 A 1/2.3-inch 10.3Mpixel 50frame/s Back-Illuminated CMOS Image Sensor

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This paper presents a 1/2.3-inch 10.3Mpixel Back-Illuminated (BI) CMOS image sensor that targets both digital still camera (DSC) and high-definition camcorder applications. These applications require high-pixel-count, high-sensitivity, high saturation signal, low noise and high-speed imaging for image quality [1]. The sensor is scaled down to get a higher resolution due to higher pixel count. Several approaches such as a Cu process to reduce the pixel height and inner micro-lenses to gather rays of incident light have been proposed to overcome electro-optical challenges [2-4]. The BI process has been reported as one of the most promising technologies to improve optical performance [5,9]. This BI image sensor includes a 10b/12b analog-to-digital converter (ADC), an internal phase-locked loop (PLL) and a 10b serial LVDS interface to enable a data-rate up to 576MHz.

Pixel sharing increases the sense-node capacitances because of: floating-diffusion (FD) regions linked in series, and interconnect capacitance. The FD capacitance causes a trade-off between conversion gain and full well capacity [4,6]. The imager uses a 1.65×1.65μm² 4-shared-pixel FD boost-driving architecture with a view to optimize for high fill factor, high conversion gain and high full well capacity.

Figure 22.9.1 depicts the schematic diagram and basic timing of a 4-shared-pixel FD boost-driving architecture. The pixel consists of transfer (TR), reset (RST) and amplifier (AMP) transistors, and hole-accumulation diodes (HAD), and does not include a select transistor. The upper 2 pixels and RST source region share the first FD. The lower 2 pixels share a second FD. The first and the second FD regions are connected by wiring in a vertical manner to reduce node capacitance. The high conversion gain caused by a reduction of node capacitance widens the amplitude of the vertical signal line and enables a reduction of random noise. Pixel selection is executed by controlling the FD potential through the RST transistor by driving the reset drain electrode (DRN). Whereas the FDs of unselected pixels are set low, that of the selected pixel is set high. The winner-take-all characteristic of the source follower leads the selected pixel's signal to the vertical signal line. A conventional FD driving image sensor achieves the FD potential not only using the coupling between the amplifier transistor's gate and the vertical signal line, but also using the coupling between the amplifier transistor's gate and drain line. These sensors are limited to a horizontal scanning time because the DRN electrodes have to be connected among all pixels or alternating from the left and right columns [4,7,8]. In this sensor, the DRN is separated from the amplifier drain electrode (VDD) because of the freedom in placing the metal wiring layer when using the BI process. By electrode separation, the pixel selection and horizontal scanning time at 10b resolution are executed in less than 0.2μs and 5.5μs, respectively. The DRN node is supplied by 2.9V (boost) or 0.7V (low) using embedded bias circuits to increase the FD potential and to execute the pixel selection. A conversion gain of 75μV/e⁻, random noise of 1.7e^-_{rms} and a saturation signal of 9130e⁻ are achieved by the 4-shared-pixel FD boost driving architecture.

Figure 22.9.2 is the cross-sectional view of the pixel with on-chip color filter and micro-lens. The sensor is fabricated using a 0.14μm 1P4M CMOS process with specialized add-on steps for BI technology. The pixel size reduction results in a quantum efficiency decrease for the image sensor. BI technology solves this issue caused by a narrow metal aperture and amount of optical stack over a photodiode in a conventional front-side image sensor. Above the illuminated side, a metal light shield formed among the photodiodes to reduce crosstalk in the pixel array achieves good color separation.

Figure 22.9.3 displays the spectral response of the sensor. A sensitivity of 9890e⁻/lux*s is achieved. The BI image sensor is not only advantageous in terms of its optical characteristics but also offers flexibility in terms of metal wiring on a pixel area. This flexible layout improves crosstalk noise by wire coupling [9]. With regards to the bulk crosstalk, a deep p-implant is implemented as an isolation barrier to prevent the photo-generated electron from diffusing across to the adjacent pixel. The low dark current of 3e⁻/s is achieved by the pinning and thermal treatment process on both the front-side and the back-side.

For BI, the degradation of the sensitivity is only slightly dependent on the angle at which the light enters. Figure 22.9.4 shows the degradation of the R, G and B light. The degradation of Green (550nm) light is 24% at a 15°angle of incidence. An F-number dependence of 0.99 (F2.8/F5.6) is achieved.

The chip specification is summarized in Figure 22.9.5. An input clock of 72MHz is required to obtain a 576MHz data rate with the column-parallel ADC architecture. The sensor performance is 10.3Mpixel 22fps at 12b, 50fps at 10b resolution for still mode, and 6.3Mpixel 60fps for HD video mode. The measured power consumption in HD mode is 375mW. One of the challenges of high-speed imaging is to compensate for skew introduced in printed circuit board (PCB) design and to increase the setup or hold time at the receiver. The sensor has several variable channels of serial LVDS interfaces. Each channel has a delay line buffer in order to compensate for the differences of each data lane. The delay line circuit consists of 2 kinds of circuits: (1) a phase-locked loop (PLL) generates the delay control signal, and (2) delay-line buffers are used in each data line. The delay control signal generated by a voltage-controlled oscillator in the PLL is delivered to delay-line buffers having the same configuration as the oscillator, and each delay buffer can easily generate a stable delay substantially identical to the delay generated in the oscillator. The control signal is delivered to a delay buffer as a current, and the delay step adjusted by current value can be controlled in the delay buffer. A delay step of 47ps is achieved in each data line.

Characteristics of the 1/2.3-inch 10.3Mpixel Back-Illuminated CMOS image sensor are summarized in Figure 22.9.5. The low light luma-S/N performance is measured at an 18% gray patch from a 5500K light source through a F/2.8 lens. A low-light luma-S/N performance after AWB and CCM of 14.5dB is achieved at 10lux. The dynamic range is 71dB. Figure 22.9.6 is a reproduced image at 10.3Mpixel taken by the sensor at 25lux. Figure 22.9.7 shows a chip micrograph.

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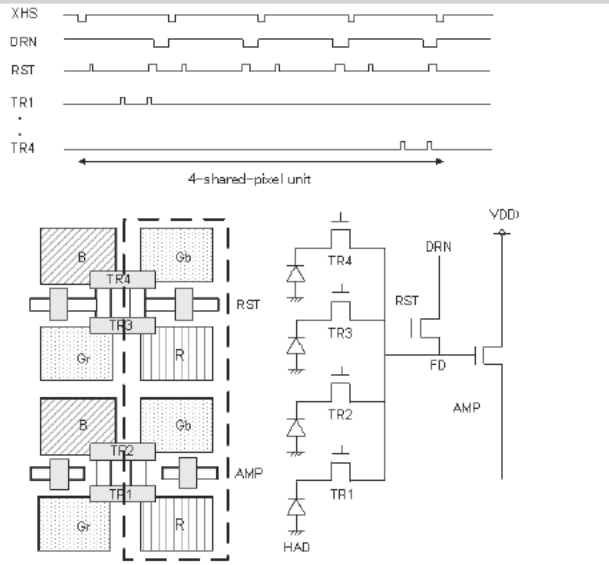

Figure 22.9.1: Schematic diagram and basic timing.

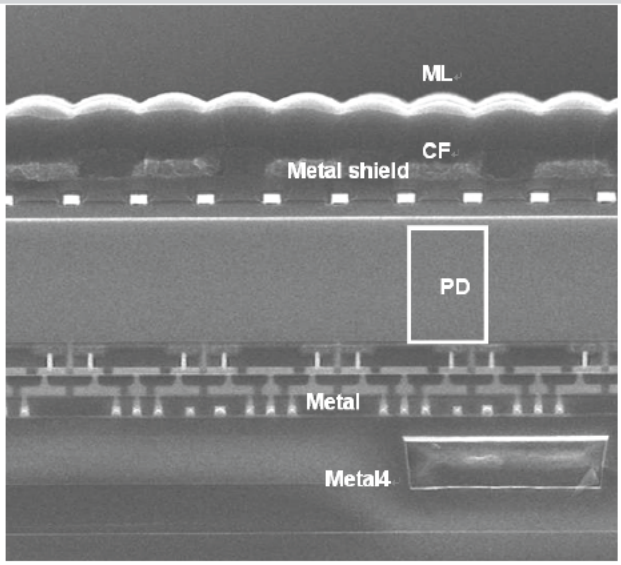

Figure 22.9.2: 1.65μm pixel cross-section.

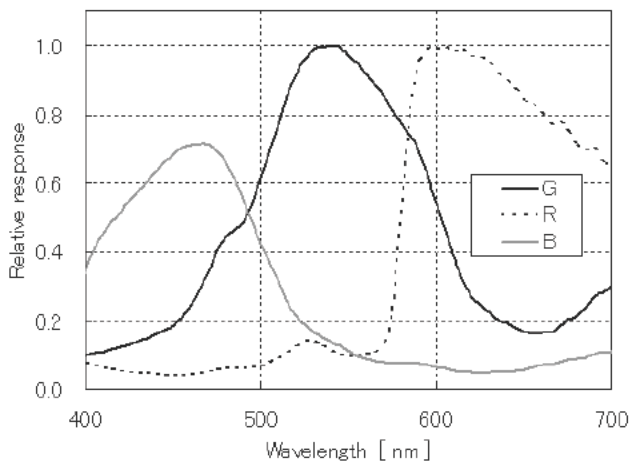

Figure 22.9.3: Measured spectrum.

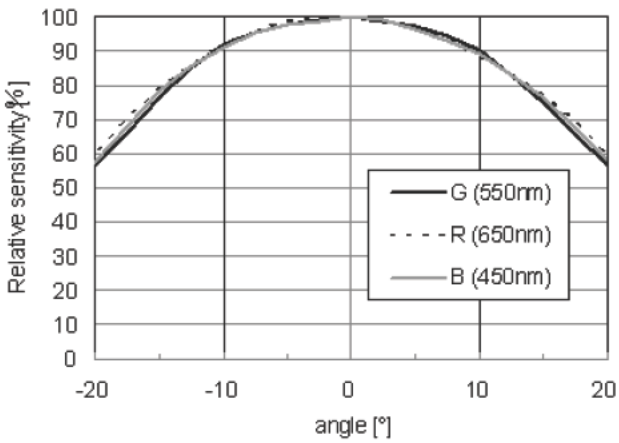

Figure 22.9.4: Optical angle response.

Item	Specification	Item	Characteristics
Process	0.14um 1 Poly 4 Metal Back Illumination	Saturation Signal	9130e- (60°C)
Pixel size	1.65um(H)×1.65um(V)	Conversion gain	75uV/e-
Number of effective pixels	3720(H)×2760(V)	Sensitivity	9890 e-/lux·s 3200K light source with IR cut filter of 650nm cut-off
Supply voltage	2.7V/1.8V	F-number dependence (F2.8/F5.6)	0.99
Input clock frequency	72MHz	Lag	Below measurement threshold
Max. data-rate	576MHz	Dark current	3e-/sec (60°C)
Output	10b serial LVDS	RMS random noise	1.7e-rms (16x gain)
Mode	10.3Mpixel 12b 22frame/s	Dynamic range	71dB (1x gain)
	10.3Mpixel 10b 50frame/s	Data line delay	47ps/Step
	6.3Mpixel 10b 60frame/s (HD)	Power consumption	375mW HD video mode (Dark)
	3.2Mpixel 10b 120frame/s (HD)		

Figure 22.9.5: Specification and characteristics.

Figure 22.9.6: Reproduced image (F2.8, D55, 50fps, Tint20ms, Gain32x).

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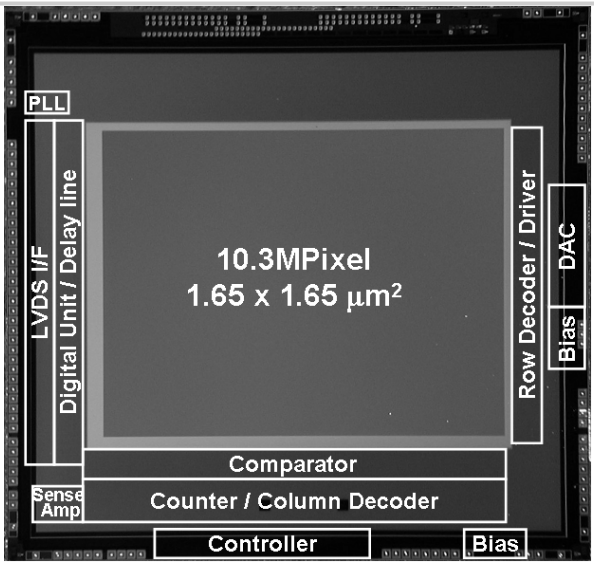

Figure 22.9.7: Chip micrograph.

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