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2.9 Low-Crosstalk and Low-Dark-Current CMOS Image-Sensor Technology Using a Hole-Based Detector

Eric Stevens[1], Hirofumi Komori[2], Hung Doan[1], Hiroaki Fujita[1], Jeffery Kyan[1], Christopher Parks[1], Gang Shi[1], Cristian Tivarus[1], Jian Wu[1]

[1]Eastman Kodak, Rochester, NY, [2]Eastman Kodak, Yokohama, Japan

As the pixel size of CMOS image sensors (CIS) shrink, problems associated with crosstalk become more severe for devices built using mainstream CMOS processing. This high crosstalk increases the amount of noise added to the final image (via an increase of the off-diagonal terms in the color correction matrix (CCM)) and degrades the modulation transfer function (MTF). Reducing dark current has also been challenging for such CIS imagers. At present, the solution to these problems has been to switch to n-type substrates [1, 2] since they have been used for interline charge-coupled devices (CCDs) for decades [3].

This technique is well known for reducing the lateral diffusion component of crosstalk. The downside of this approach for CIS devices is that it requires major modifications to the process and existing IP cannot necessarily be used [4]. Another tradeoff is that gettering of n-type substrates, which affects dark current, is more difficult.

We have recently built CIS imagers of various pixel sizes (from 4.3μm down to 1.4μm) using a new hole-based detector technology. This technology retains the existing p-epi substrates of typical mainstream CMOS processes so that all of the existing IP can be used. A deep n-well is formed in the image area using MeV P implantation so that the pixel becomes pMOS based and the signal-charge carriers are now holes instead of electrons. A cross section of a sample pixel built using this new structure is shown in Fig. 2.9.1. Unlike CCDs [5], which have thousands of transfers, a CIS device has only one transfer. Therefore, transfer efficiency is not such an issue for CIS and the lower mobility of holes is of little to no consequence.

As a result of the new structure, we have reduced the crosstalk from 25 to 7% on a 4.3μm pixel, from 46 to 10% on a 2.2μm pixel, and from 49 to 15% on a 1.75μm pixel. The residual crosstalk has been determined to be primarily the result of optical crosstalk as opposed to lateral diffusion of charge carriers within the silicon. Crosstalk is defined here as the ratio of green- to red-pixel quantum efficiency at 650nm. The quantum efficiency (QE) of the 1.4μm pixel is not reported because of the lack of scaled micro-optics on the test arrays. For the 2.2μm pixel, the reduction in crosstalk reduces the noise introduced from the CCM by 4dB for 7500K daylight (international commission on illumination, CIE, illuminant D75), and by 6dB for 2856K blackbody (CIE illuminant A).

A graph showing the measured QE of the new 2.2μm pMOS pixel compared to that of a 2.2μm standard nMOS CIS pixel is shown in Fig. 2.9.2. The reduced crosstalk in the green and red portions of the visible spectrum is clearly evident. It can also be seen that the blue pixel QE of the pMOS pixel is 10% higher than that of the standard nMOS device, which results from the incorporation of an antireflective UV-nitride film over the photodiode (PD) for the pMOS pixel [6]. This film was found to increase dark current on the nMOS device; hence it could not be used there. The red-pixel QE is 5% lower for the pMOS device because of the well structure. It is worth noting that these proof-of-concept devices were made using only a single microlens and a relatively thick optical stack. Therefore, improvements in quantum efficiency and reduction in optical crosstalk are expected for the smaller pixels with the use of an inner lens and/or thinner optical stack height, as is well known in the industry [7].

Charge capacities of 60kh+ for 4.3μm, 11kh+ for 1.75μm, and 4kh+ for 1.4μm pixels have been measured on these same test arrays. The charge capacities of the 2.2μm pixel devices were not measured because the signal amplitude saturated the output structures of these pixels.

The dark current of the new device is reduced for several reasons. First, with the pMOS-based pixel, the isolation regions and pinning implants are now n-type. Unlike the B typically used for these regions in nMOS-based pixels, As and P pile up at the silicon-silicon dioxide interface, which helps quench interface generation in the pMOS pixels. Additionally, any positive charge in dielectric layers above the structure tends to accumulate these interfaces (as opposed to depleting them as happens for nMOS pixels), which further helps to reduce interface generation. The well structure serves to reduce the bulk-diffusion dark-current component. We have measured as low as 6 pA/cm^2 on our test arrays at 60°C, which was found to be a factor of >30× less than that of the standard nMOS CIS pixels. For comparison, we have also built nMOS pixels in p-epi on n-type substrates, where it was found that the dark current was only cut in half. Therefore, we conclude that the pMOS structure offers a dark current advantage over traditional nMOS devices because of better interface passivation. Dark-current spectroscopy indicates that the average dark current is presently limited by metallic contamination. By reducing these contaminants from the process, dark current can be further reduced. Measured dark-current density (normalized to the PD area) versus temperature for some sample pixels is shown in Fig. 2.9.3.

The 4.3μm pixel was built using TSMC's 0.18μm process and the smaller pixels were built using their 0.11μm process. The 2×2 shared pixel designs were fairly conservative; conversion gains of around 60μV/h+ were measured for most of the 1.75μm pixel designs and about 70μV/h+ were measured for the 1.4μm pixels. Although some pixel designs achieved ~80μV/h+, they were found to suffer from higher lag. The conversion gain of the 2×1 shared, 4.3μm pixel was intentionally low (~19μV/h) due to the expected high charge capacity. Standard 2.7V power supplies were used for the smaller pixels, and lag was measured at only 3 holes for the 1.75μm pixels, and <1 hole for the 1.4μm pixels. A graph showing lag versus the transfer gate low-level clock voltage (TGlo) for the 1.75μm and 1.4μm pixels is shown in Fig. 2.9.4.

Another advantage of the pMOS-based pixel is reduced amplifier noise due to the lower 1/*f* and random-telegraph signal noise characteristics of a pMOS FET [8]. We have measured the pixel noise of our pMOS device to be 40% lower than that of an equivalent nMOS device, ($3h+_{rms}$ versus $5e-_{rms}$).

A comparison of pixel noise is shown in Fig. 2.9.5. A complete summary of the measured device performance characteristics is given in Fig. 2.9.6 and a micrograph of the test arrays is shown in Fig. 2.9.7.

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References:
[1] S. Inoue, I. Ueno, T. Koizumi et al., "3.25 M-Pixel APS-C Size CMOS Image Sensor," Eijogakugiho, vol. 25, no. 28, March, 2001.
[2] G. Agranov, R. Mauritzson, S. Barna et al., "Super Small, Sub 2μm Pixels for Novel CMOS Image Sensors," *IEEE Int'l Image Sensor Workshop*, pp. 307–310, June 2007.
[3] Y. Ishihara, E. Oda, H. Tanigawa et al., "Interline CCD Image Sensor with an Anti Blooming Structure," *ISSCC Dig. Tech. Papers*, pp. 168–169, 1982.
[4] J. Nakamura Ed., *Image Sensors and Signal Processing for Digital Still Cameras*, CRC Press, pp.159–160, 2006.
[5] M. Tompsett, B. Kosicki, and D. Kahng, "Measurements of Transfer Efficiency of 250-Element Undercut-Isolated Charge Coupled Devices," *Bell Syst. Tech. J.*, p.5, Jan. 1973.
[6] C-W. Chang, S-G Wuu, D-N Yaung et al., "High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology," *IEEE Int'l Image Sensor Workshop*, pp. 207–210, June 2007.
[7] H. Takahashi, T. Noda, T. matsuda et al., "A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders," *ISSCC Dig. Tech. Papers*, pp. 510–511, 2007.
[8] K. Abe, S. Sugawa, R. Kuroda et al., "Analysis of Source Follower Random Telegraph Signal using nMOS and pMOS Array TEG," *IEEE Int'l Image Sensor Workshop*, pp. 62–65, June 2007.

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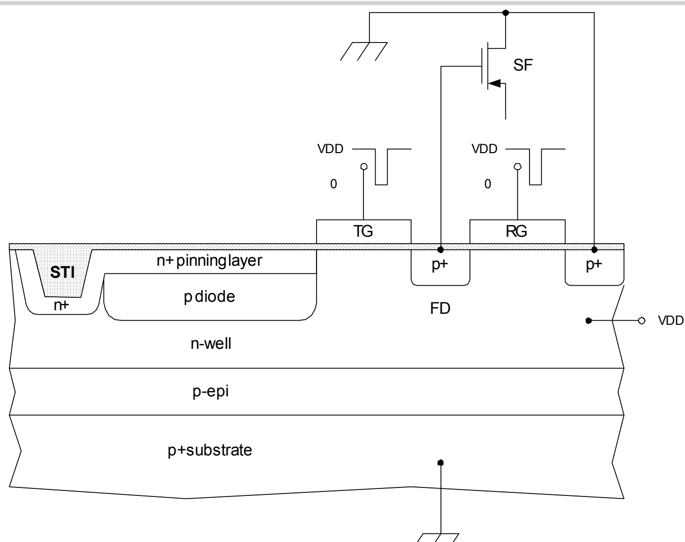

Figure 2.9.1: Cross section of pMOS-based CIS pixel structure. The n-well is formed only in the image area.

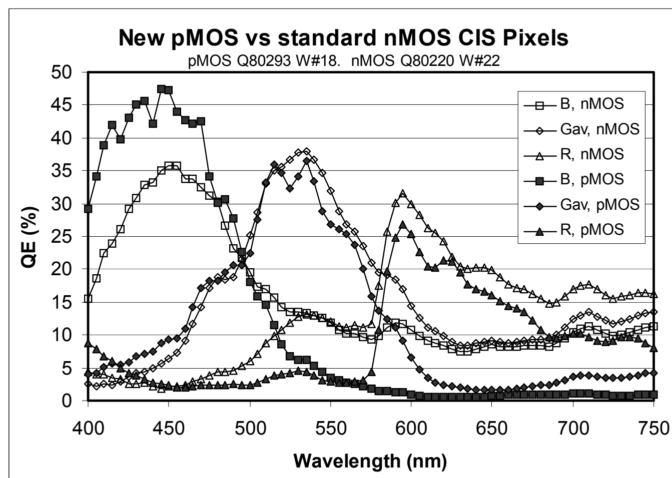

Figure 2.9.2: Absolute quantum efficiency for the new pMOS CIS pixel versus standard nMOS pixel. The pixel size is 2.2µm.

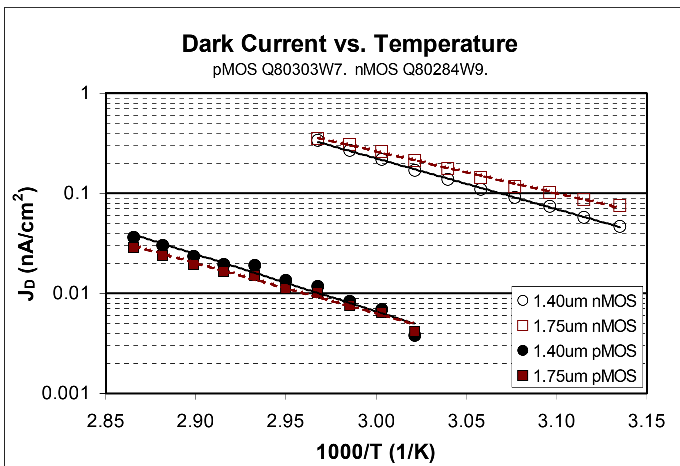

Figure 2.9.3: Dark-current density versus temperature for sample nMOS and pMOS pixels.

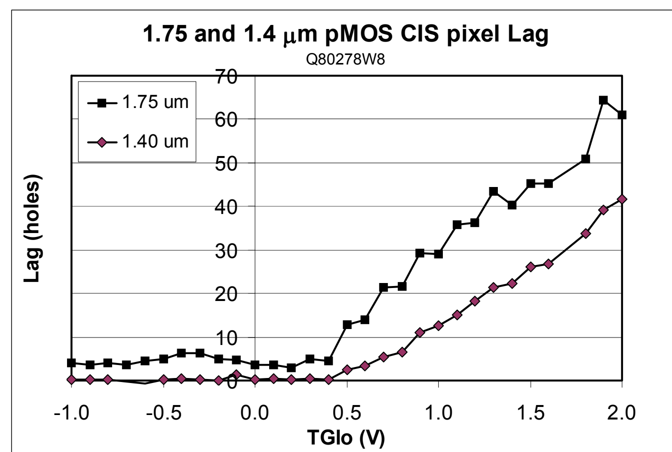

Figure 2.9.4: First-field decay lag as a function of transfer gate low clock voltage, TGlo.

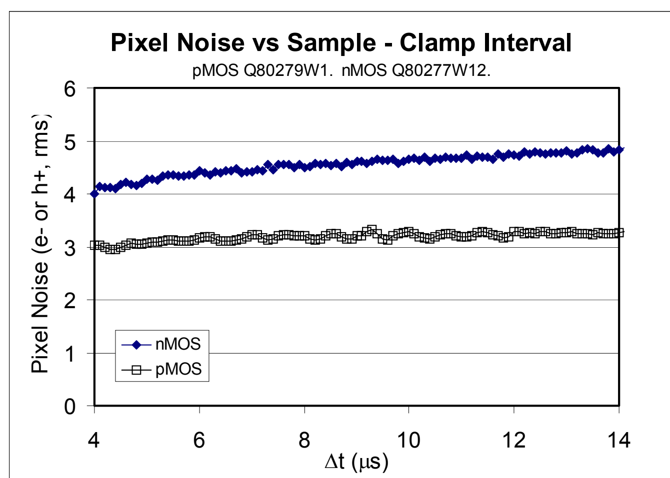

Figure 2.9.5: Comparison of nMOS and pMOS pixel noise as a function of sample-to-clamp interval, $\Delta t = t_{SAMPLE} - t_{CLAMP}$.

Pixel Size	4.3 µm	2.2 µm	1.75 µm	1.4 µm
Process	0.18 µm 1P 4M	0.11 µm 1P 4M	0.11 µm 1P 4M	0.11 µm 1P 4M
Sharing (FDs)	2 × 1	2 × 1	2 × 2	2 × 2
PD fill factor	36%	41%	35%	29%
Conversion gain	19 µV/h+	85 µV/h+	60 µV/h+	70 µV/h+
Charge capacity	60 kh+	-	11 kh+	4 kh+
Peak QE (B,G,R)	46, 38, 28	47, 36, 27	46, 36, 24	-
Crosstalk (G/R)	7%	10%	15%	-
Lag (TGlo = 0V)	<1 h+	3 h+	3 h+	<1 h+
Dark signal (at 60 ºC)	10.4 h+/s	1.2 h+/s	0.42 h+/s	0.22 h+/s

Figure 2.9.6: Performance characteristics of various pMOS CIS pixels. The crosstalk values are at an incident wavelength of 650nm.

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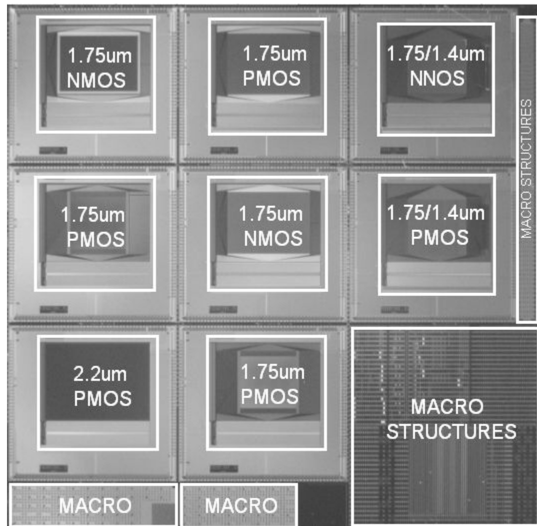

Figure 2.9.7: Chip micrograph showing test arrays for new hole-based CIS technology.