A 2/3" 2-M pixel progressive scan FT-CCD for digital still camera applications.

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ABSTRACT

The first 2M-pixel CCD image sensor especially developed for digital still camera applications is presented. The sensor can be operated in various modes, to best suit the camera requirements. High-quality full resolution images are obtained using the camera's mechanical shutter. A variety of subsampled color images of reduced vertical resolution can be generated by simply changing the pulse pattern, allowing e.g. real-time preview mode on the camera's LCD display, or fast auto-focus mode. The sensor output amplifier combines low noise and excellent linearity with a high conversion factor.

CCDS FOR DIGITAL STILL CAMERAS

Consumer digital still cameras (DSCs) are an important market for CCD imagers. Both the annual production of cameras increases, as well as the average resolution. 1M- and 1.3M-pixel cameras are now common, and a number of 2M-pixel cameras will soon be introduced. We present the first 2M pixel CCD for consumer DSCs.
A CCD used in a DSC has to fulfil the following requirements [2],[3]: (1) the best quality full-resolution still image; (2) an ISO-100-like camera sensitivity; (3) a real-time preview mode of operation for the camera LCD viewfinder, auto-focus, auto-exposure system, etc. (4) a flexible low-cost, low-power system solution.

ARCHITECTURE AND BASIC OPERATION

The new 2M-pixel 2/3-inch progressive scan 1600(H)x 1280(V) FT-CCD imager with 5.1x5.1 μm^2 pixels optimised for digital still camera applications, is shown schematically in Fig. 1. Fig. 2 shows a top view and cross-section of the image pixel, optimised for high charge capacity, good highlight handling and high light sensitivity [1]. In full-resolution mode, up to 6 images/s can be generated. A mechanical shutter then shields the sensor from light during readout. The shutter requirements are compatible with the requirements for mechanical shutters for interline-transfer CCDs with interlaced readout, which are frequently used in high-resolution DSC cameras. In preview mode, subsampling is performed at the image-storage transition during frame-shift by dumping

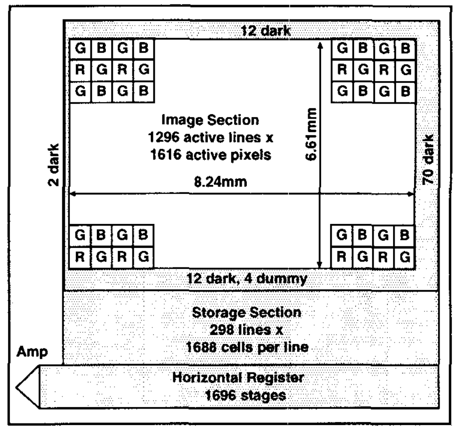

Figure 1: Block diagram of the 2M-pixel 2/3" FT-CCD

the electron charge packets to the n-substrate using the electronic shutter locally. The resulting images can be used for the electronic (LCD) preview and for camera functions such as auto-focus. The mechanical shutter remains open in preview mode. Compared to the 1/3-inch 1.3M CCD imager presented last year [2], several basic improvements in operation and performance are presented below.

IMAGE FORMAT AND PIXEL SIZE

The aspect ratio of CCDs for DSCs is not fixed. A 4:3 aspect ratio is common for VGA- and 1M-cameras. A 5:4 format is compatible with XSGA monitors and with full-size $8\frac{1}{2}$"x11" prints. A 3:2 aspect ratio is compatible with the classical silver-halide 36 x 24 mm format. The 1600x1280 image format was chosen because it allows easy generation of 5:4, 4:3 and 3:2 aspect ratio images with constant horizontal resolution, see Table 1. The 5.1 μm pixel size combines a sufficiently high sensitivity and dynamic range to obtain an ISO-100 sensitivity and 10-bit dynamic range, with a small chip size of only 90 mm^2.

STORAGE SIZE AND METHOD OF SUBSAMPLING

In [2], a simple 1:4 subsample scheme to reduce the vertical resolution was presented. We now add to this an

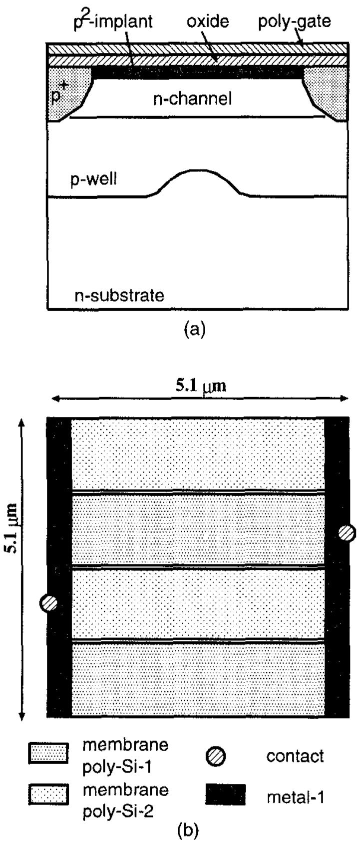

Figure 2: Pixel structure: (a) cross-section; (b) top view of electrode structure

electronic optical low-pass filtering and optimised and flexible subsample schemes.

Table 1 shows some possible subsample ratios and the resulting vertical resolution for the 3 image formats. Up to 40 subsampled images at 280-line images/s can be generated with 25MHz readout. The simple 1:4 subsampling

full resolution modes			
aspect ratio	5:4	4:3	3:2
active pixels	1600×1280	1600×1200	1602×1068
subsampled modes			
subsample ratio	1:5	1:5	1:4
active pixels	1600×256	1600×240	1602×267

Table 1: Overview of some possible modes of operation

(actually 2:8 to maintain a RGB pattern) is shown in Fig.3. This method has two drawbacks: (1) high aliasing because of the small resulting vertical fill factor, and (2) the unbalance between the original lines and an interlaced display. The aliasing can be reduced by an *electronic* on-chip low-pass filter in preview mode, as shown in Fig.4 for a 2:8 subsample scheme: after *each quarter*

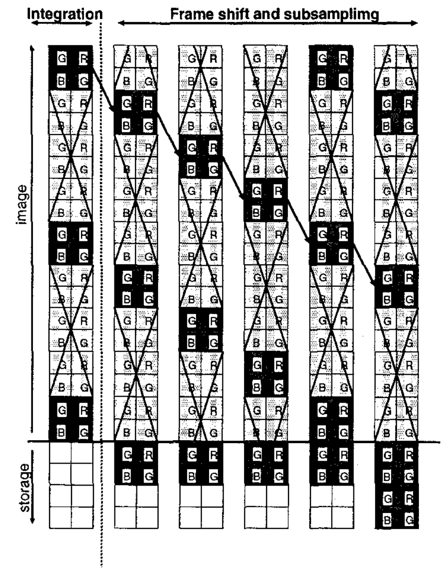

Figure 3: Simplest method of 2:8 subsampling: the charge of the crossed-out pixels is dumped at the image-storage transition

of the exposure time (Q1, Q2, ...), the image is shifted 2 lines towards the storage section. Correct interlacing

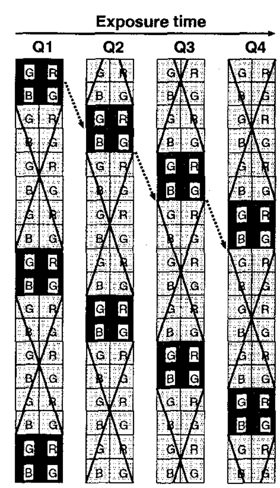

Figure 4: 'Electronic' optical low-pass filtering over four time steps (Q1...Q4) during exposure to reduce vertical aliasing in subsampled images

in subsampled images can be obtained by improving the simple 2:8 interlacing as shown in Fig.5. Both improvements can be combined. A variety of application-tailored subsample schemes is possible simply by changing the timing generator; an example for a camera with optical viewfinder (i.e. not needing the preview mode) is 'fast auto-focus' on the center of the image (Fig.6): only the center 280 lines are read out at 40 images/s.

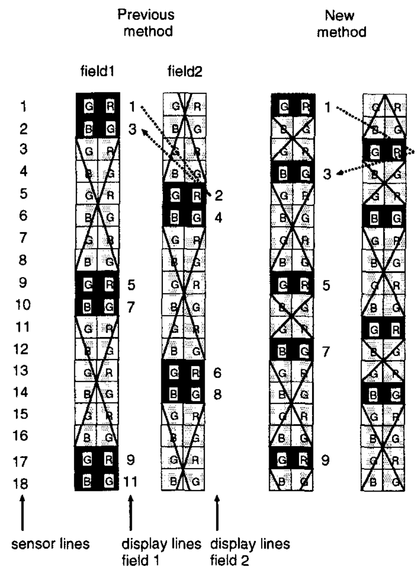

Figure 5: Subsample scheme compatible with interlaced displays

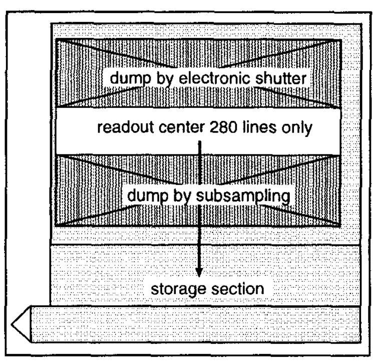

Figure 6: Subsample scheme for fast auto-focus on center of image

SENSITIVITY

Consumer CCDs require a sufficiently high mV/lux number to assure good sensitivity. A high quantum efficiency must be combined with a high output responsivity ($\mu V/e^-$). Another requirement is the compatibility with front-end ICs that typically can handle 600 to 1000 mV saturation input. A maximum charge capacity of 30k..40k e^- is sufficient to obtain high-quality 10-bit images required for DSC applications. This implies an output amplifier with 20 $\mu V/e^-$ responsivity to be competitive. Based on the results from test structures reported in [4], two versions of the first source follower were designed, one with a surface and one with a buried MOS transistor (Fig.7). To achieve a *high, matched and predictable* conversion factor, the gain of the first source-follower stage and input capacitance (the effective capacitance of the floating diffusion (FD) detection node) have to be known at the time of design. As the input capacitance becomes

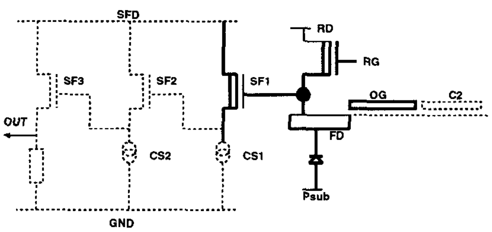

Figure 7: Elements forming the input capacitance (solid lines, effective floating diffusion capacitance) of the three-stage source follower amplifier (dashed lines). SF1 can be buried or surface MOST

very small, 1-D or 2-D approximations are no longer sufficient. We used a combination of 3-D off-state and 2-D on-state device simulations to effectively model the input capacitance, including the capacitance of the first source follower.

The conversion factor was improved from 10 to 19$\mu V/e^-$ (buried MOST) and 23 $\mu V/e^-$ (surface MOST), without additional process steps, by minimising the FD capacitances while maintaining the gain, noise and bandwidth performance of the first source follower.

SENSOR EVALUATION AND PERFORMANCE

The gain and linearity of both the surface- and buried-type output amplifier are shown in Fig. 8. Fig. 9 shows

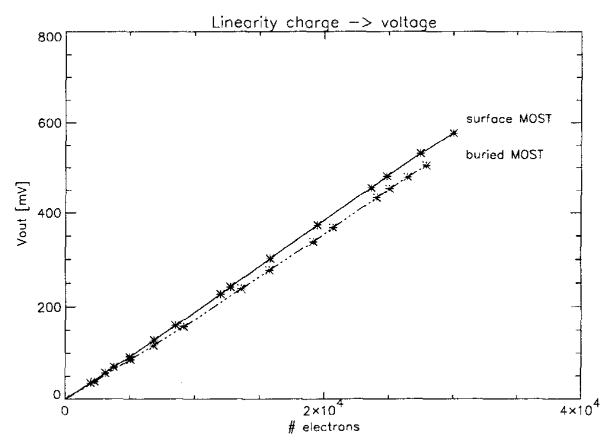

Figure 8: Outamp responsivity and linearity for surface and buried first source follower

the color response after optimization of pixel design and color filter technology. Table 2 summarizes the device architecture and performance. Fig. 10 is a die photograph. Fig. 11 shows a 2:10 subsampled image and Fig. 12 a full-resolution image.

CONCLUSIONS

A 2-M pixel 2/3" FT-CCD optimised for consumer DSC applications is presented. Compared to a previously reported 1.3M pixel FT-CCD for DSC applications [2], the

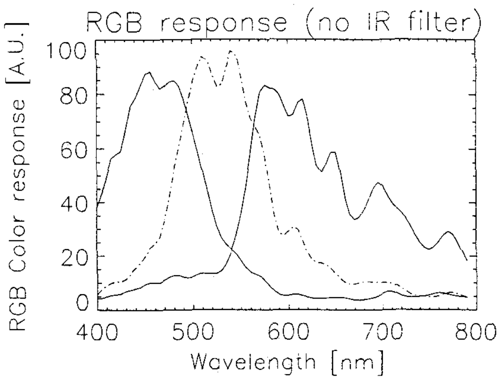

Figure 9: Optimized pixel response

CCD type	Frame Transfer with reduced storage
Optical format	2/3"
Operation modes	full resolution typ. 6 im/s monitor preview 8... 40 im/s LCD preview 5... 15 im/s
Number of active lines	1280
Number of active pixels per line	1600
Pixel size	5.1μm × 5.1μm
Minimum features	0.5 μm
Chip size	90 mm^2
V clock frequency & swing	3.125 MHz @12V
H clock frequency & swing	25 MHz @3.3V
Maximum charge capacity	40 000 electrons
Sensitivity (green)	390 mV/lux.s
Color filters	Bayer RGB
Outamp type	triple source-follower
Outamp responsivity	
surface MOST	23 μV/electron
buried MOST	19 μV/electron
Saturation output voltage	900 mV typ.
Outamp noise (5 MHz BW)	10 electrons RMS

Table 2: Summary of 2-M pixel 2/3" FT-CCD

subsampling is optimised, the pixel color response is improved, and a high, predictable responsivity of the output amplifier is obtained.

REFERENCES

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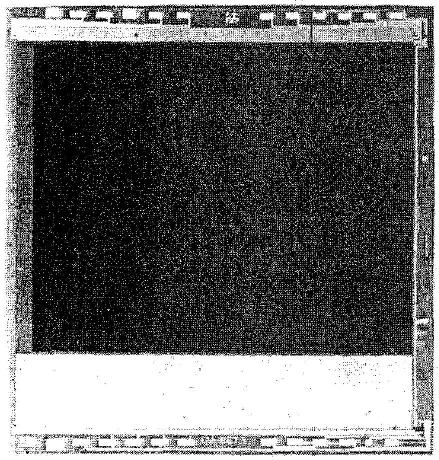

Figure 10: Die photograph (before color filters)

Figure 11: Image obtained in monitor mode, 256 lines

Figure 12: Full-resolution image, 1280 lines